# Energy- and Area-Efficient Memristor-based Ternary Content Addressable Memory for High-Speed and Low-Power Application

by

Md. Hasan Maruf

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Department of Electrical and Electronic Engineering
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The Organization of the Islamic Cooperation (OIC)
Board Bazar, Gazipur-1704, Bangladesh

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# CERTIFICATE OF APPROVAL

The thesis titled '**Energy- and Area-Efficient Memristor-based Ternary Content Addressable Memory for Low-Power Application'** submitted by Md. Hasan Maruf, St. No. 152701 of Academic Year 2015-16 has been found as satisfactory and accepted as partial fulfillment of the requirement for the Degree DOCTOR OF PHILOSOPHY IN ELECTRICAL AND ELECTRONIC ENGINEERING on 09 May 2024.

**Board of Examiners:**

_____ Chairman

**Dr. Syed Iftekhar Ali** (Supervisor)
Professor, Department of Electrical and Electronic Engineering,
Islamic University of Technology (IUT), Gazipur.

_____ Member

**Dr. Mohammad Rakibul Islam** (Ex-Officio)
Professor and Head, Department of Electrical and Electronic Engineering,
Islamic University of Technology (IUT), Gazipur.

_____

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Islamic University of Technology (IUT), Gazipur.

_____

**Dr. Md. Ruhul Amin** Member
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Islamic University of Technology (IUT), Gazipur.

_____ Member

**Dr. A. B. M. Harun-Ur-Rashid** (External)
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Bangladesh University of Engineering and Technology (BUET),
Dhaka.

_____ Member

**Dr. Md. Anwarul Abedin** (External)
Professor, Department of Electrical and Electronic Engineering,
Dhaka University of Engineering and Technology (DUET), Gazipur.

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**Dr. Syed Iftekhar Ali**
Professor,
Department of Electrical and Electronic Engineering,
Islamic University of Technology (IUT), Gazipur.
Date: 09 May 2024

**Md. Hasan Maruf**
Student No: 152701,
Academic Year: 2015-16
Date: 09 May 2024

*Dedicated to my parents, sisters, wife and adorable son.*

# ABSTRACT

The shrinking feature sizes in CMOS-based technologies pose challenges, prompting a need for more efficient computing architectures. Memristor-based ternary content addressable (MTCAM) offers a promising alternative to conventional MOSFET-based TCAM by offering a promising avenue for high-speed data searching and matching with reduced power consumption. TCAM's ternary format enables flexible data searching, vital for networking, pattern recognition, and security applications. However, conventional TCAM suffers from high costs, chip size, and power consumption. MTCAM presents a solution, offering scalability and efficiency to meet modern computing demands. The work presents a novel MTCAM design aimed at high-speed and low-power applications. This MTCAM structure, comprising of five transistors and four memristors, offers a unique approach to data preservation. By integrating WRITE and SEARCH operations on the same lines, the design addresses potential data overwrite issues during SEARCH operations through a dedicated data recall unit. Moreover, the architecture employs a consistent voltage level for both WRITE and SEARCH operations, thereby enhancing efficiency. The study conducted using HSpice simulations for a 32-word array, each containing 144 MTCAM cells, using 32nm 0.9V strained Si technology models. Employing a precharge-low current race (CR) match-line scheme, the simulations yielded impressive results: a search time of 215ps and search energy of 0.556fJ/digit/search for worst-case mismatches at a supply voltage of 1.2V, along with a substantial voltage margin of 343mV. Comparative analysis with conventional MOSFET-based TCAM and other existing designs signifies the superiority of the proposed MTCAM. It exhibits remarkable reductions in search delay (83%), search energy consumption (61%), voltage margin (14%), peak power consumption (65%), and estimated area (53%) compared to conventional MOSFET-based TCAM. Furthermore, it boasts improvements in search delay (55%), search energy efficiency (18%), voltage margin (7%), and peak power consumption (10%) compared to the latest existing MTCAM design. Notably, the area footprint of the proposed MTCAM cell is significantly smaller than that of other designs, making it a viable option for integrated circuit applications.

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# List of Abbreviations of Technical Terms

| | |
|---|---|
| TCAM | Ternary Content Addressable Memory |
| MTCAM | Memristor-based TCAM |
| CR | Current Race |
| AI | Artificial Intelligence |
| IoT | Internet of Things |
| CMOS | Complementary Metal-Oxide Semiconductor |
| MOSFET | Metal-Oxide Semiconductor Field Effect Transistors |
| SCA | Short Channel Effect |
| NCA | Narrow Channel Effect |
| MRAM | Magnetic Random Access Memory |
| STT-RAM | Spin-Transfer Torque RAM |
| MTJ | Magnetic Tunnel Junction |
| DWM | Domain Wall Memory |
| RRAM | Resistive Random Access Memory |
| NVM | Non-volatile Memory |
| IRDS | International Roadmap for Device and Systems |
| MEMS | Micro-electromechanical Systems |
| PMUs | Power Management Units |
| ML | Match-line |
| TTL | Transistor-Transistor Logic |
| ECL | Emitter-Coupled Logic |
| SRAM | Static Random Access Memory |
| HRS | High Resistance State |
| LRS | Low Resistance State |
| MIM | Metal-Insulator-Metal |
| PCM | Phase Change Memory |
| TEAM | Threshold Adaptive Memristor |
| VTEAM | Voltage Threshold Adaptive Memristor |

| | |
|---|---|
| MD | Mismatch Dependent |
| AF | Active Feedback |
| RF | Resistive Feedback |
| DRAM | Dynamic Random Access Memory |
| BSER | Bit Search Error Rate |
| MLSA | Match-line Sense Amplifier |
| EDA | Electronic Design Automation |
| IC | Integrated Circuit |

# Chapter 1

# Introduction

## 1.1 Introduction

Currently, the semiconductor sector maintains a significant influence on defining the contemporary technological environment. Semiconductors are fundamental components in a wide range of devices, from smartphones and laptops to cars and industrial machinery. The industry is currently undergoing significant innovation, characterized by advancements in miniaturization and performance enhancement, alongside the incorporation of emerging technologies such as artificial intelligence (AI) and Internet of Things (IoT) functionalities [1]. The advancement of semiconductor materials and manufacturing techniques has resulted in the production of more efficient and high-performing chips. This progress has facilitated the proliferation of applications in various domains, including autonomous vehicles, renewable energy systems, and healthcare equipment. Nevertheless, the industry faces numerous hurdles and uncertainties in its future trajectory. When considering the future, it is evident that the semiconductor business is positioned to encounter both favorable circumstances and challenges. The anticipated expansion in the market is attributed to the increasing need for high-performance computing and the widespread adoption of smart devices. This growth is further fueled by the emergence of advanced technologies such as 5G, quantum computing, and edge computing, which necessitate more sophisticated semiconductor solutions. Nevertheless, the sector is currently facing challenges related to disruptions in the supply chain, geopolitical conflicts, and the growing intricacy of chip design and production processes [2]. The continuous endeavor to uphold Moore's Law, which denotes the historical trend of doubling the transistor count on a chip roughly every two years, has encountered diminishing returns owing to physical constraints [3]. The aforementioned circumstances have resulted in a transition towards novel packaging methodologies, including 3D stacking and heterogeneous integration. In addition, the issue of sustainability is brought to light by environmental considerations and the energy-intensive processes involved in semiconductor manufacturing.

The semiconductor industry encounters numerous significant concerns in terms of limitations and challenges. To begin with, the complexity of designing and manufacturing advanced chips has led to escalating costs and longer development cycles, hindering smaller players from entering the market. Additionally, geopolitical tensions and trade restrictions can disrupt the global supply chain, impacting the availability of essential components. The industry's heavy reliance on a few key manufacturers also makes it vulnerable to disruptions caused by natural disasters, pandemics, and other unforeseen events. Furthermore, as transistors approach atomic sizes, quantum effects and power leakage become significant challenges, affecting chip performance and energy efficiency. The increasing demand for semiconductors in various sectors strains the capacity of fabrication facilities, leading to periodic shortages. Finally, addressing environmental concerns, such as the substantial energy consumption and electronic waste generated during production, poses a moral and regulatory challenge for the industry. In brief, the semiconductor industry holds immense promise for technological advancement, but it also faces formidable challenges that require innovative solutions in design, manufacturing, supply chain management, and sustainability to ensure its continued growth and relevance in the ever-evolving landscape of modern technology.

## 1.2 More Moore, More than Moore and Beyond CMOS

The semiconductor industry has been on a continuous journey to develop smaller and more efficient transistors. This trend, often referred to as Moore's Law, was slowing down due to physical limitations. Researchers were exploring alternatives such as new materials, 3D stacking, and novel transistor designs to keep pushing the boundaries of miniaturization. The term "More Moore" refers to one of the trends in the International Roadmap for Devices and Systems (IRDS), which is a roadmap that outlines the future trends and challenges in the semiconductor industry. The other trends are known as "More than Moore" and "Beyond CMOS". Figure 1.1 presents the conceptual view of these trends.

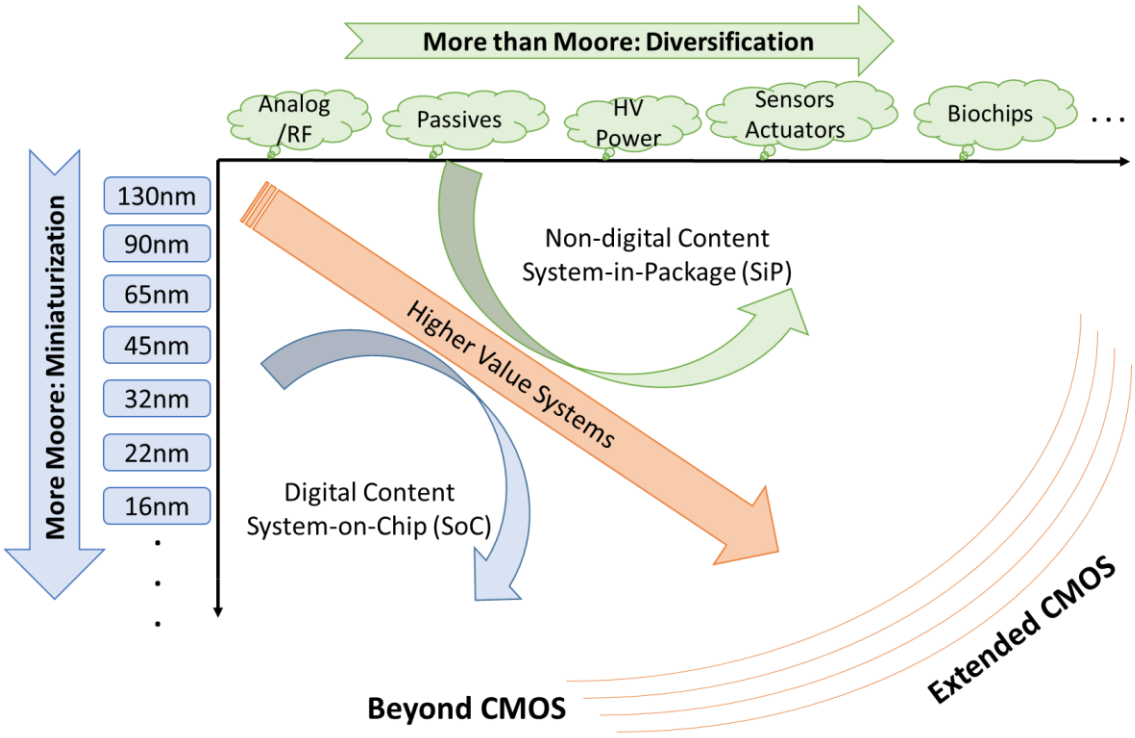



Figure 1.1: Conceptual view of three different trends (More Moore, More than Moore and Beyond CMOS) which can mitigate Moore's law slowdown [4]

"More Moore" is an example of continuous dimensional scaling. Using the already enormous number of foundries that use the common Complementary Metal-Oxide Semiconductor (CMOS) manufacturing techniques, new device topologies will enable at least another ten years of miniaturization. This will support the growth of component types including microprocessors, volatile and non-volatile memory, and digital logic that gain from downsizing [5].

"More than Moore" refers to the idea that the continued progress of technology will depend not only on the shrinking of transistors, but also on the integration of other components, such as sensors, micro-electromechanical systems (MEMS), and power management units (PMUs), into the same chip. In summary, "More than Moore" and "More Moore" are two concepts that describe different approaches to the continued progress of computer technology. "More than Moore" emphasizes the integration of other components into computer chips, while "More Moore" focuses on the doubling of the number of transistors on a chip every two years. [6].

"Beyond CMOS" refers to the exploration of alternative computing paradigms and device technologies that go beyond the limitations of conventional CMOS technology. CMOS has been the dominant technology for semiconductor devices for several decades, but as transistor sizes approach atomic scales, challenges related to power consumption, heat dissipation, and leakage currents have arisen. Beyond CMOS technologies explore novel materials, device architectures, and computing concepts such as quantum computing, neuromorphic computing, spintronics, and various other emerging technologies that could potentially offer more energy-efficient and higher-performance computing solutions [7, 8].

## 1.3 CMOS Technology and its Design Challenges

CMOS technology is a fundamental and widely-used integrated circuit manufacturing process in the field of electronics. It involves the creation of digital logic circuits and microprocessors on silicon wafers. CMOS technology is known for its low power consumption, making it highly efficient for portable devices and battery-operated applications. It utilizes a combination of P-type and N-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to create complementary logic functions, allowing for low power dissipation and reduced heat generation. CMOS technology has enabled the development of increasingly complex and powerful electronic devices, contributing significantly to the advancement of modern computing, communication systems, and consumer electronics [9, 10].

Designing integrated circuits using CMOS technology presents several significant challenges. One primary challenge lies in minimizing power consumption while maintaining performance, as CMOS devices consume power even in standby mode due to sub threshold leakage currents. Ensuring robustness against process variations, which can lead to parameter mismatches between transistors, is another challenge. As feature sizes continue to shrink, quantum mechanical effects like tunneling become more pronounced, causing increased leakage and performance degradation. Furthermore, mitigating the impact of electromagnetic interference and noise in densely packed CMOS circuits is essential for reliable operation. Lastly, addressing the thermal challenges associated with high transistor densities and increased power dissipation is crucial to prevent overheating and ensure long-term reliability [11, 12].

## 1.4 Emerging Technologies - Beyond CMOS for Memory and Computing

Emerging memory technologies are poised to revolutionize data storage and processing. In recent years, the field of memory and computing technologies has witnessed significant advancements driven by emerging devices. Emerging NVM technologies like Phase-Change Memory (PCM), Resistive RAM (ReRAM), Spin-Transfer Torque RAM (STT-MRAM), Ferroelectric RAM (FeRAM), and Memristor have been gaining attention. These technologies offer faster access times, higher endurance, and lower power consumption compared to traditional NAND Flash memory [13]. PCM is a type of non-volatile memory that stores data by changing the physical state of a material, typically a chalcogenide glass. It can be switched between amorphous and crystalline states to represent binary data, offering fast read and write speeds and high endurance [14]. ReRAM is based on the principle of resistance change in a material due to the movement of ions. It has the potential to provide higher speed, lower power consumption, and better scalability compared to traditional memory technologies [15, 16]. STT-MRAM uses the spin of electrons to store data in magnetic tunnel junctions. It combines the non-volatility of flash memory with the speed and endurance of DRAM, making it suitable for both cache and main memory applications [17]. FeRAM uses the polarization of ferroelectric materials to store data. It offers low power consumption, high read and write speeds, and endurance comparable to DRAM [18]. Memristors are two-terminal non-volatile memory devices that change resistance based on the flow of electric charge. They are considered a potential candidate for neuromorphic computing and memory design [19]. These innovations, along with others like Hybrid Memory Cube (HMC), High Bandwidth Memory (HBM), and quantum memory, are pushing the boundaries of traditional memory technologies and paving the way for more efficient and powerful computing systems.

The idea of memristor was proposed in 1971 [20]. It is regarded as a fourth essential circuit component that combines memory with a resistor. The history of the voltage placed across a memristor's terminals determines the device's resistance. Since its invention by HP lab in 2008 [21] memristor-based stateful logic, Boolean logic, and implicative circuits have been proposed [22, 23].There have been suggestions for memristor-based cross-bar

array circuits, non-volatile processors, neuron circuits, multi-state registers, and neuromorphic computing [24, 25]. Cross-bar memory array computing using memristor-only logic has been presented in [26] and [27]. These logics, which are based only on memristors and cross-bar arrays, do not include XOR/XNOR gates or input sharing among several gate-limiting fanouts. XOR logic gates are implemented by memristors-as-drivers gates (MAD) [28], which can share inputs between multiple gates.

## 1.5 Conventional MOSFET-based TCAM

Conventional MOSFET-based ternary content addressable memory (TCAM) is a type of memory that allows for fast searching and retrieval of data based on its content. In contrast to traditional binary counterpart, TCAM is capable of storing and retrieving information in three states: 0, 1, and "don't care" (X). This additional state allows for more flexible matching operations, making TCAM particularly useful for applications that involve complex matching and pattern recognition. TCAM is commonly used in network routers and switches to perform high-speed packet forwarding and filtering. It enables the hardware to quickly identify and route packets based on specific criteria, such as source/destination IP addresses, port numbers, or protocol types. The "don't care" state allows for wildcard matching, which is useful for implementing access control lists (ACLs) or routing table lookups.

The basic building block of a conventional MOSFET-based TCAM is the "ternary cell," which stores a ternary value (0, 1, or X) and can perform a parallel comparison with a given input. The memory is organized into a matrix of these cells, and the search operation involves applying the search key to all cells simultaneously. The cells that match the search key produce a match signal, indicating the presence of the desired data. While TCAM provides fast search capabilities, it typically has limitations in terms of density, power consumption, and cost compared to binary memories like random-access memory (RAM). This is due to the additional complexity required to implement the ternary functionality. As a result, TCAM is often used in combination with other memory technologies to balance the trade-offs between speed and cost-effectiveness in various applications.

## 1.6 Problem Statement

- Conventional MOSFET-based TCAM consumes significant power due to the presence of two static random access memory (SRAM) blocks in its design.
- The conventional TCAM has sixteen transistors in its cell which occupies a relatively large silicon area compared to other memory types. Improving the area efficiency of TCAMs without compromising performance is a significant research challenge.
- TCAMs require fast search operations to deliver high-speed packet processing in networking applications. Reducing search delay is a key research area.
- As the demand for higher memory capacity increases, it's essential to explore scalable TCAM architectures that can accommodate larger memory arrays without sacrificing performance or increasing power consumption disproportionately.
- Increasing the density and integration of memristor-based TCAM (MTCAM) arrays while minimizing area power consumption is a significant research challenge. Developing compact and scalable TCAM architectures compatible with memristor devices requires innovative circuit and system-level design approaches.
- Most of the MTCAMs use same input lines for WRITE and SEARCH operations which causes overwriting of stored data during search.
- The existing designs demand separate voltage levels to execute the WRITE and SEARCH functions for MTCAM, resulting in the requirement of two separate voltage sources.

## 1.7 Motivation

The motivation behind designing a MTCAM lies in the unique characteristics and advantages offered by memristor technology. Memristors, or memory resistors, are a type of electronic device that can remember the amount of charge that has previously flowed through them. They exhibit a resistance that depends on the history of the currents and voltages applied to them, allowing them to retain information even when the power supply is turned off.

There are several compelling points to overcome the challenges and research gaps associated with TCAMs/MTCAMs:

**Performance Enhancement**: Addressing the issues in TCAMs/MTCAMs can lead to significant improvements in memory performance, including faster search operations,

reduced latency, and enhanced data processing capabilities. This can enable more efficient and responsive computing systems across a wide range of applications, from data centers to edge devices.

**Energy Efficiency**: By improving the efficiency of TCAMs/MTCAMs, it is possible to reduce overall power consumption in computing systems, leading to lower operational costs, extended battery life in portable devices, and reduced environmental impact. Energy-efficient TCAMs/MTCAMs are crucial for sustainable computing solutions in the face of growing energy demands.

**Scalability and Integration**: Overcoming the design challenges in TCAM/MTCAM cell can facilitate the development of highly scalable memory architectures that can accommodate the increasing demand for storage and processing capabilities in modern computing environments. Scalable TCAMs enable the seamless integration of memory-intensive applications and support the growth of big data analytics, artificial intelligence, and machine learning workloads.

**Reliability and Robustness**: Enhancing the reliability and robustness of TCAMs/MTCAMs is essential for ensuring data integrity, system stability, and long-term operational reliability in mission-critical applications such as aerospace, healthcare, and finance. Reliable TCAMs help mitigate the risk of data corruption, system failures, and security breaches, thereby bolstering trust and confidence in computing technologies.

**Innovation and Technological Advancement**: Overcoming the design challenges in TCAMs/MTCMs require innovation, collaboration, and interdisciplinary research efforts across academia, industry, and government institutions. By pushing the boundaries of materials science, device engineering, circuit design, and computer architecture, we can unlock new opportunities for technological advancement and drive forward the frontiers of computing and information technology.

**Competitive Advantage and Market Leadership**: Organizations and countries that successfully address the design challenges in TCAM/MTCAM stand to gain a competitive advantage in the global marketplace. By investing in research and development, fostering innovation, and commercializing breakthrough technologies, they can establish market leadership positions and drive economic growth through technology-driven innovation and entrepreneurship.

**Social Impact and Human Well-being**: TCAMs/MTCAMs have the potential to revolutionize various aspects of society, including healthcare, education, transportation, and communication. By enabling faster medical diagnostics, smarter transportation systems, personalized learning experiences, and ubiquitous connectivity, TCAM technology can improve human well-being, enhance quality of life, and foster societal progress and inclusivity.

In summary, the motivation to overcome the design challenges in TCAMs/MTCMs are driven by the transformative potential of this technology to advance computing capabilities, improve energy efficiency, enhance reliability, foster innovation, drive economic growth, and benefit society as a whole. By addressing these challenges, it is possible to unlock new opportunities for scientific discovery, technological innovation, and sustainable development in the digital age.

## 1.8 Objective

The main objectives of this research work is specified as follows:

- To design a MTCAM cell which will be area-efficient compared to conventional MOSFET-based design.
- To maintain the high-speed and low-power operation of MTCAM.
- To perform the WRITE and SEARCH operation using single power supply.
- To provide the capability of restoring the data after completion of each search cycle.

## 1.9 Outline of Methodology

Step 1: Select the appropriate memristor model for TCAM cell design: There are various types of memristor models each with its own advantages and disadvantages. Therefore, it is important to select the appropriate memristor model for the TCAM design.

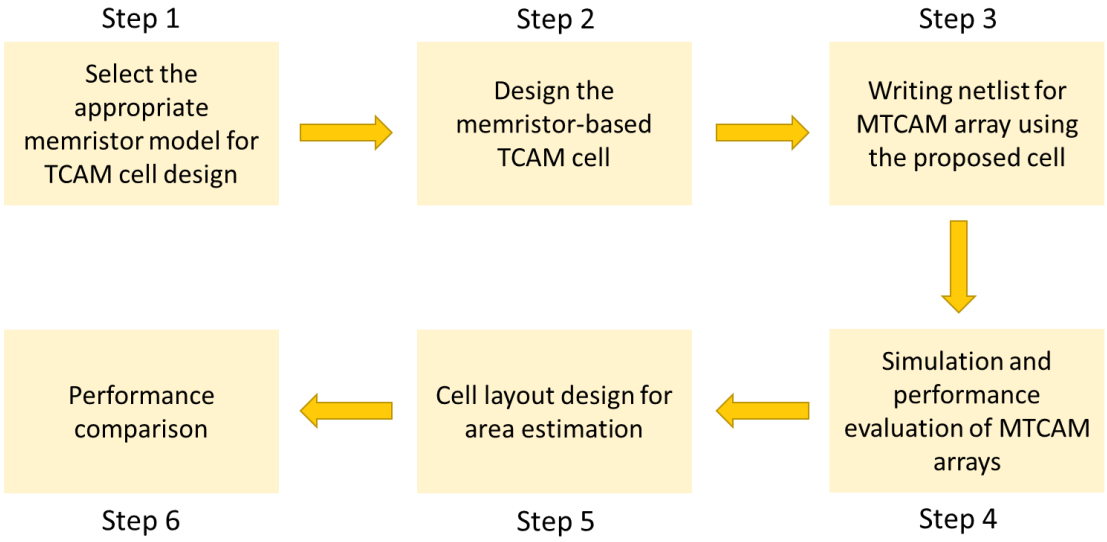
Step 2: Design the MTCAM cell: The second step is to design the circuit of the MTCAM cell, taking into account the number of cells, word length, and the number of rows and columns required to meet the specific requirements.

Step 3: Writing netlist: Once the memristor model is selected, designing circuits and preparing netlist for the MTCAM cell as well as array are to be done for simulation.

Step 4: Analyze the MTCAM: After designing the MTCAM, it must be analyzed to ensure that it performs as expected.

Step 5: Layout design: The layout will be designed to have an estimation of circuit area and for comparison with existing designs.

Step 6: Performance Comparison: The performance of the proposed MTCAM will be compared with the recent related works.




## 1.10 Thesis Organization

Chapter 2 delves into the fundamentals of memristors, providing a mathematical definition and elucidating their working principles. It proceeds to outline various standard memristor models along with their corresponding I-V characteristic curves. A comparative analysis of these models through statistical methods helps ascertain the most effective one.

In Chapter 3, the focus shifts to a comprehensive exploration of MOSFET-based TCAM systems. The discussion encompasses the architectural levels, match-line (ML) structures, and diverse bit cell topologies. Additionally, attention is given to the inherent tradeoffs between power consumption and processing speed, leading to the exploration of different match line sensing strategies, search line driving schemes, and power-efficient CAM designs.

Chapter 4 undertakes a detailed literature survey of MTCAM designs. Its objective is to review existing literature comprehensively, pinpointing potential research gaps.

Chapter 5 endeavors to introduce a novel compact MTCAM cell design. A hybrid compact MTCAM cell, comprising five transistors and four memristors, is proposed. The chapter delves into the structural aspects of the proposed cell, including its match-line configuration, WRITE and SEARCH operations, and array architecture.

Chapter 6 presents simulation results pertaining to both WRITE and SEARCH operations. These results are derived from simulations conducted in HSpice utilizing 32×144 MTCAM arrays. Metrics such as search time, search energy, and estimated area are computed to facilitate a comparative analysis against existing designs.

Lastly, Chapter 7 provides a conclusive summary of the thesis research work, along with suggestions for future endeavors.

# Chapter 2

# Basics of Memristor and its Models

## 2.1 Introduction

Within this chapter, an exposition of the foundational aspects of memristors is presented, encompassing mathematical delineations and operational principles. Various conventional models of memristors, each characterized by their unique I-V curves, are examined. Through a brief overview, a comparative analysis of different memristor models is conducted utilizing statistical methods, aiming to discern the most suitable model exhibiting optimal resemblance to experimental data.

## 2.2 Memristor Background

The memristor, short for "memory resistor," is a fundamental electronic component that exhibits a unique property known as memristance. It was first theorized by Dr. Leon Chua in 1971 as the fourth basic circuit element alongside the resistor, capacitor, and inductor. These four fundamental circuit variables have the potential to generate six distinct groupings: the characterization of current ($i$) emerges from the interplay between electric charge and temporal dynamics, as exemplified by the equation $dq = idt$; voltage ($v$) finds its definition in the interrelation connecting electromagnetic flux and temporal progression, expressed as $d\varphi = vdt$; resistor ($R$) obtains its definition within the linear association linking voltage and current, as portrayed by the equation $dv = Rdi$; capacitance ($C$) originates from the intrinsic connection between electric charge and voltage, represented by the equation $dq = Cdv$; inductance ($L$), conversely, is established within the linear connection between electromagnetic flux and electric current, as outlined by the equation $d\varphi = Ldi$; lastly, Chua postulated the existence of a relationship between electric charge (q) and electromagnetic flux (Φ), leading to the equation $d\varphi = Mdq$ [20]. Figure 2.1 presents a comprehensive overview of all the potential groupings proposed by Chua, including the missing memristor.

The memristor's distinctive characteristic lies in its ability to change its resistance based on the amount of charge that has flowed through it in the past, effectively

"remembering" its previous resistance states. This property makes memristors promising for non-volatile memory and neuromorphic computing applications. The first experimental demonstration of a memristor was achieved by a team of researchers at HP Labs led by Stan Williams in 2008, using thin films of titanium dioxide. This breakthrough sparked significant interest in the field of memristive devices, paving the way for developments in memory technologies and novel computing paradigms [21].

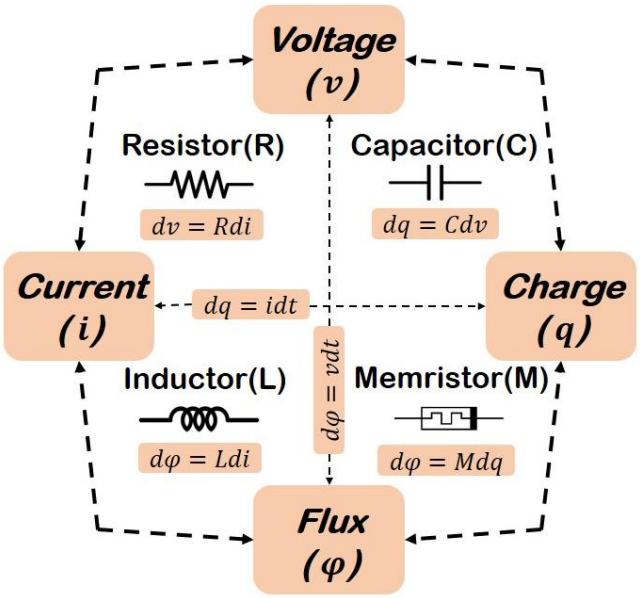



Figure 2.1: The four primary circuit parameters can be interconnected in six manners [29]

## 2.3 Memristor Fundamentals

A memristor can be understood as a resistor with memory capabilities, characterized by two terminals that alter their resistance based on the quantity and direction of electric charge passing through them. Its resistance goes up when a current flows in one direction, and decreases when the current moves in the opposite direction. The significant aspect is that the memristor conserves its latest resistance value even during periods of inactivity, and maintains this state upon being powered up again [30]. This memory attribute empowers the memristor to recollect previous resistance levels. A distinctive symbol, illustrated in Figure 2.2, represents the memristor. Its non-volatile memory property is primarily due to a unique behavior called a pinched hysteresis loop. This loop materializes when the relationship between current and voltage crosses the origin, and a memristor, driven by a bipolar periodic signal, displays a pinched hysteresis loop at the origin. The

presence of a non-zero region within this pinched hysteresis loop signifies memory functionality. Moreover, the extent of the hysteresis loop widens at lower frequencies of the input signal and contracts at higher frequencies [31, 32].

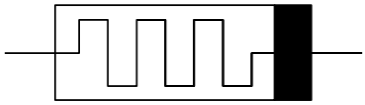


Figure 2.2: Symbol of memristor

If the representation of flux relies on charge as a variable, the memristor is referred to as a charge-controlled memristor [33]. For the scenario of a charge-controlled memristor:

Flux is function of charge, $\emptyset = f(q)$ (1)

Differentiating (1) in terms of time:

$$\frac{d\emptyset}{dt} = \frac{df(q)}{dt}$$

$$or, \frac{d\emptyset}{dt} = \frac{df(q)}{dq} . \frac{dq}{dt}$$

$$or, v(t) = M(q) . i(t) \quad (2)$$

here $M(q)$ represents the memristance, measured in ohms.

On the contrary, when charge is formulated as a function of flux, the memristor is known as a flux-controlled memristor [33]. For a flux-controlled memristor:

$$q = f(\emptyset) \quad (3)$$

Differentiating (3) in terms of time:

$$\frac{dq}{dt} = \frac{df(\emptyset)}{dt}$$

$$or, \frac{dq}{dt} = \frac{df(\emptyset)}{d\emptyset} . \frac{d\emptyset}{dt}$$

$$or, i(t) = W(\emptyset) . v(t) \quad (4)$$

here $W(\emptyset)$ denotes the memductance, measured in Siemens.

## 2.4 Memristive Structures

In 1976, Chua and one of his students introduced a memristive system, following five years of Chua's postulates [34]. Their concept introduced the memristive system as a two-terminal apparatus compatible with both direct current (DC) and alternating current (AC) power sources, capable of displaying both linear and nonlinear behavior contingent on the frequency value. They further asserted that the voltage-current correlation demonstrates a unique pinching effect within a hysteresis loop. This relationship between voltage and current is mathematically represented by equation (5), in which *M* is a function of two variables: *w* and *i*, both of which vary with time. The device's condition is characterized by the state variable *w*. It is given by the following equations:

$$v = M\big(w, i(t)\big)i(t) \tag{5}$$

$$dw/_{dt} = f(w, i(t)) \tag{6}$$

Initially, a prevailing notion suggested that the memristor's operation was limited to AC control. Nevertheless, subsequent investigations uncovered its distinct DC characteristics as well [35-38]. The memristor displays two discrete switching conditions, denoted as the high resistance state (HRS) and the low resistance state (LRS) [39]. The structure takes on a sandwich configuration known as metal-insulator-metal (MIM), where the insulator, commonly $TiO_2$, is chosen for its high intrinsic resistivity [40]. Previous studies have explored various metal electrodes, including copper (Cu), silver (Ag), platinum (Pt), gold (Au), and titanium/nitride (Ti/TiN). Furthermore, other insulators like $TaO_x$, ZnO, $HfO_2$, and $SnO_2$ have been proposed as alternatives to $TiO_2$ [41]. Hewlett-Packard (HP) laboratories classify $TiO_2$ as a doped region ($TiO_{2-x}$) with lower resistance and an undoped region ($TiO_2$) with higher resistance, as illustrated in Figure 2.3(a). The corresponding circuit model, proposed by the HP lab, is shown in Figure 2.3(b). Application of a positive threshold voltage to the $TiO_{2-x}$ layer causes the repulsion of positively charged oxygen vacancy ions, resulting in reduced $TiO_2$ layer thickness and increased conductivity. This change leads to the shift from HRS to LRS, referred to as the SET process [21, 42-44]. On the other hand, if a negative voltage is applied to the $TiO_{2-x}$ layer, positively charged oxygen vacancy ions are drawn to it, increasing the thickness of

the $TiO_2$ layer. This transition from low resistance state (LRS) to high resistance state (HRS) is commonly termed RESET [21, 44]. Figure 2.4 illustrates how the experimental I-V curve might be analyzed to ascertain the type of state variable at the boundary [21].

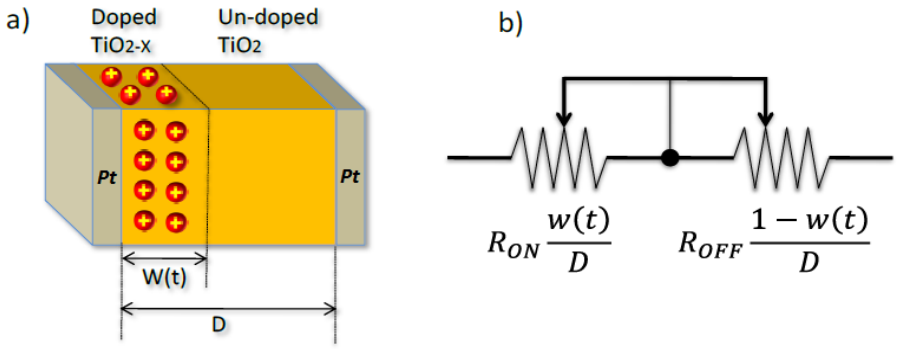



Figure 2.3: The HP research team's proposed physical structure for the memristor and its schematic model are shown in (a) and (b) respectively [21]

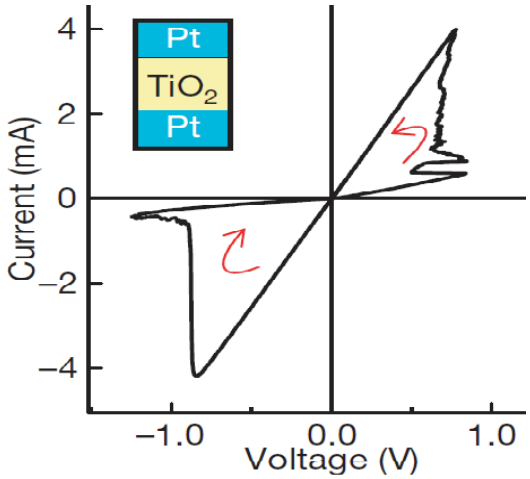



Figure 2.4: An experimental current-voltage (I-V) characteristic of the memristor. The initial width of the oxide layer, encompassing both non-conductive $TiO_2$ and oxygen-deficient $TiO_{2-x}$, measures 5nm [21]

## 2.5 Models of Memristor

This section has discussed several memristor models, each of which has its own distinct advantages and disadvantages.

### 2.5.1 HP Model (Linear Ion Drift Model)

The memristor's inherent behaviour was initially presented by HP in 2008 [21]. As per their explanation, the phenomenon of memristance is observed in nanoscale systems where a connection is established between semiconductor electronics and the motion of

ions when a voltage is applied [21, 45]. The insulator layer's dimension, as shown in Figure 2.4(a), is denoted as $D$. Within this layer, there is a doped section with a width represented by $w(t)$, which displays a lower resistance referred to as $R_{ON}$. Conversely, the undoped portion of the layer exhibits a higher resistance, as indicated by $R_{OFF}$. Furthermore, it is postulated that the memristor exhibits ohmic behaviour, characterised by a uniform electric field, linear ion migration, and equal average ion migration mobility $\mu_D$ [46]. The V-I combination is given below:

$$v(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF} \left( 1 - \frac{w(t)}{D} \right) \right) i(t) \tag{7}$$

by putting $x(t) = {}^{w(t)}/_{D}$ ; $(0 \leq x \leq 1)$ in the equation (7) which gives:

$$v(t) = \left( R_{ON}.x(t) + R_{OFF}\left(1 - x(t)\right) \right) i(t)$$

$$or, \qquad v(t) = M(w).i(t) \tag{8}$$

As a result, the value $M(w) = \left( R_{ON}.x(t) + R_{OFF}\left(1 - x(t)\right) \right)$ gives the memristance. Within this setting, $w(t)$ represents the state variable that Chua provided in the paper [34]. The following formula can be used to determine how much the state variable has changed:

$$v_D = \frac{dw(t)}{dt} = \frac{\mu_D R_{ON}}{D} i(t) \tag{9}$$

here ${dw}/{dt}$ represents the rate of change of the state variable, corresponding to the drift velocity ($v_D$) of the oxygen vacancies within the apparatus. Following the integration of equation (9), it becomes possible to ascertain the value of $w(t)$, which holds a proportional relationship to the charge (stemming from oxygen vacancies) within the device:

$$w(t) = \frac{\mu_D R_{ON}}{D} q(t) \tag{10}$$

The difference between the simulation produced by the HP model with a sinusoidal voltage input and the experimental pinched hysteresis I-V curve reported in reference [21] is seen in Figure 2.5. The generated curve demonstrates an almost straight-line pattern across the device, except for its boundaries. The non-linear behavior observed at the borders of the

memristor, notably at the boundaries where x=0 and x=1, is attributed to the significant electric field generated by oxygen vacancies at these sites. As a result, the state variable does not achieve values of 0 or D in these regions. In addition, the model does not take into account the nonlinear effects caused by the strong electric field (about MV/cm) at the edges of the memristor, as described in reference [47]. Consequently, the model inadequately replicates the real-world device behavior near its boundaries. In a physical memristor, the voltage remains relatively constant at the boundary—a characteristic not replicated by the simulation. Furthermore, the current values portrayed in the simulation curve are excessively elevated compared to actual measurements.

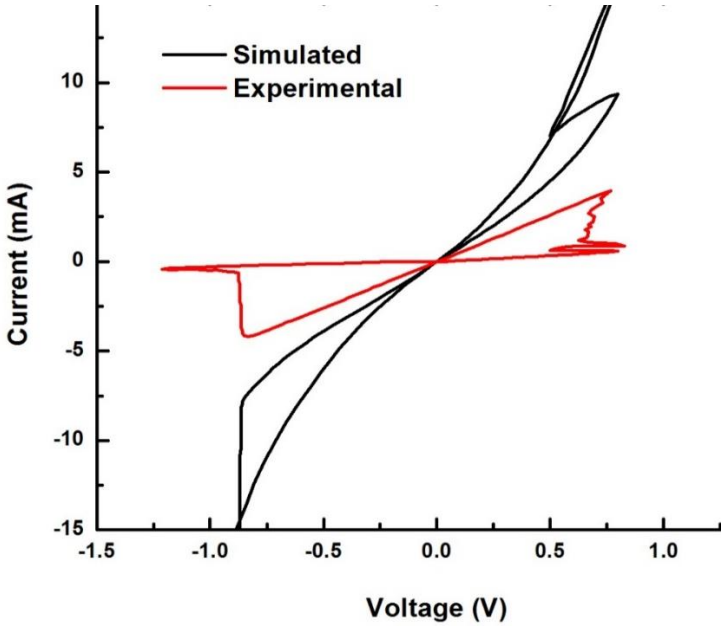



Figure 2.5: Comparing the experimental hysteresis curve from [21] with the simulated curve generated by HP model. Matlab is used to run the simulation with settings like $\mu_D$ = 3.8e-15$m^2V^{-1}s^{-1}$, D = 5nm, $x_0 = w_0/D = 0.2$ (where $w_0$ is the initial value of w), $R_{ON} = 100\Omega$, $r = R_{OFF}/R_{ON} = 160$, $v_0 = 1V$, $\omega = 2\pi$ rad/s, and $V(t) = v_0\sin(2\pi t)$ V. Most of these parameter values are obtained from [21]

### 2.5.2 Strukov Model

An improvement on the HP model, the Strukov model focuses mainly on the non-linear characteristics of the memristor in an effort to resolve problems related to the boundary conditions included in the HP model. They introduced a concept called the "window function" which is applied as a multiplier to the current in the state derivative. By formulating equation (13), they effectively address the following challenges: i) The limitations of Chua's initial assumption, ii) The representation of the non-linear relationship

between integrated current and voltage, taking into account the strict switching requirement, and iii) The establishment of the proportional connection between the state variable and the charge passing through the device [21].

$$v(t) = \left\{ R_{ON} \frac{w(t)}{D} + R_{OFF} \left( 1 - \frac{w(t)}{D} \right) \right\} i(t) \tag{11}$$

$$\frac{dw(t)}{dt} = \mu_D \frac{Ron}{D} i(t) F(w) \tag{12}$$

In this context, the term $F(w)$ is denoted as the window function, defined as follows:

$$F(w) = \frac{w(1-w)}{D^2} \tag{13}$$

The limit is given as: $F(0) = 0,\ F(D) = \frac{1-D}{D} \simeq 0$

The difference between the experimental curve and the simulated I-V curve produced by the Strukov model is seen in Figure 2.6. The experimental curve displays behavior that is different from the simulated curve. Furthermore, the state derivative, which represents the oxygen vacancy drift velocity, approaches zero at the boundary. As a result, the state variable gets stuck at the border and is unable to reverse. This situation is known as the "boundary lock problem" or the "sticking problem."

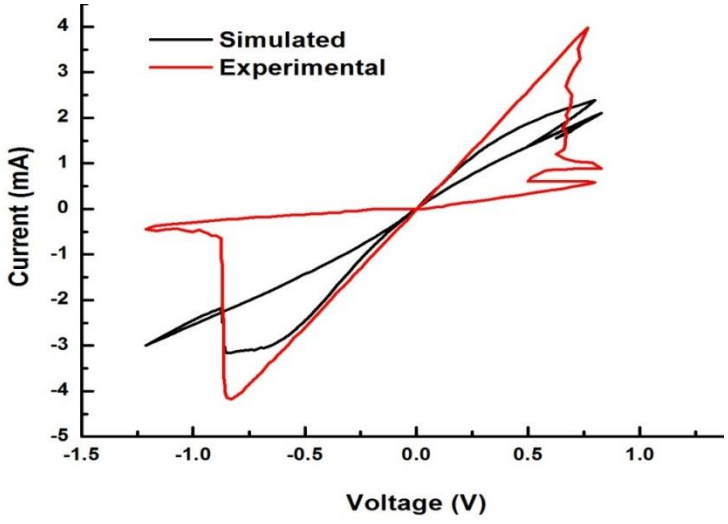



Figure 2.6: Comparing the simulated I-V curve produced by using the Strukov model to the experimental I-V curve. The simulation was conducted using Matlab, utilizing the same parameter values as those used in Figure 2.5

### 2.5.3 Benderli Model

During 2009, Benderli introduced a distinct window function with boundary conditions that deviate from the Strukov window function [48, 49]. Formula (14) presents the newly proposed window function, while equation (15) outlines the stipulations associated with this specific window function.

$$F(w) = \frac{w(D-w)}{D^2} \tag{14}$$

$$\begin{Bmatrix} w \to 0, F(w) \to 0 \\ w \to D, F(w) \to 0 \end{Bmatrix} \tag{15}$$

The I-V characteristic of this model is displayed in Figure 2.7, revealing dissimilarities from the experimental curve. Once more, the suggested model fails to elucidate the non-linear characteristics of the device when situated at the boundary states ($w=0$ or $w=D$) as defined. It's also evident that the simulated curve manifests significantly higher current levels than the experimental curve. The current value, mainly on the negative side, is particularly noticeable.

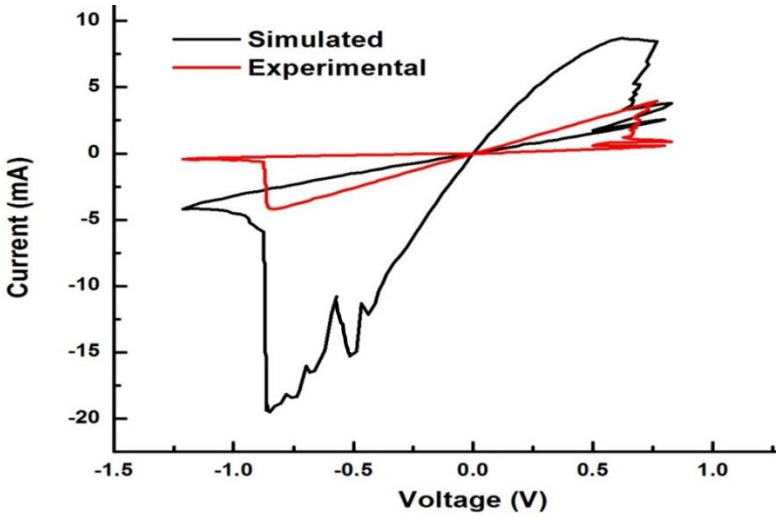



Figure 2.7: The hysteresis curve associated with the Benderli model. The simulation has been conducted in Matlab using identical parameters to those used in Figure 2.5

### 2.5.4 Joglekar Model

In 2009, Joglekar introduced his window function, proposing certain modifications to the HP model [50]. He incorporated two crucial parameters into the existing model. Firstly, the parameter η was introduced to signify the polarity of the memristor. When

$\eta$ = +1, it indicates that applying a positive voltage expands the width of the doped region, while $\eta = -1$ signifies that applying a positive voltage reduces the width of the doped region. Secondly, the window function (17) was implemented to address boundary-related concerns, requiring the drift velocity $v_D$ to be maximum at the device's center and to become zero at the device's edges. This alteration aimed to ensure that the normalized state variable, $x$, consistently maintains a range within $0 \leq x \leq 1$.

$$\frac{dw}{dt} = \frac{\eta \mu_D R_{ON}}{D^2} i(t) F(x) \tag{16}$$

$$F(x) = 1 - (2x - 1)^{2p} \tag{17}$$

here $x$ represents $^{w}/_{D}$ and $p$ denotes a positive integer. The nonlinearity effect is governed by the value of $p$ in the window function. Figure 2.8 illustrates the Joglekar window function for various $p$ values. The graph makes it evident that the window function achieves its maximum value at $x$=0.5, while being zero at the boundaries ($x$=0 and $x$=1). In Figure 2.9, the hysteresis I-V curve of the Joglekar window function model is depicted. This curve demonstrates better similarity to the experimental curve, although it exhibits higher current levels. This curve effectively captures the non-linear behavior of the memristor. However, it remains unsuccessful in addressing the boundary lock issue. Additionally, once the memristor reaches its boundary, this state becomes permanently maintained [51, 52].

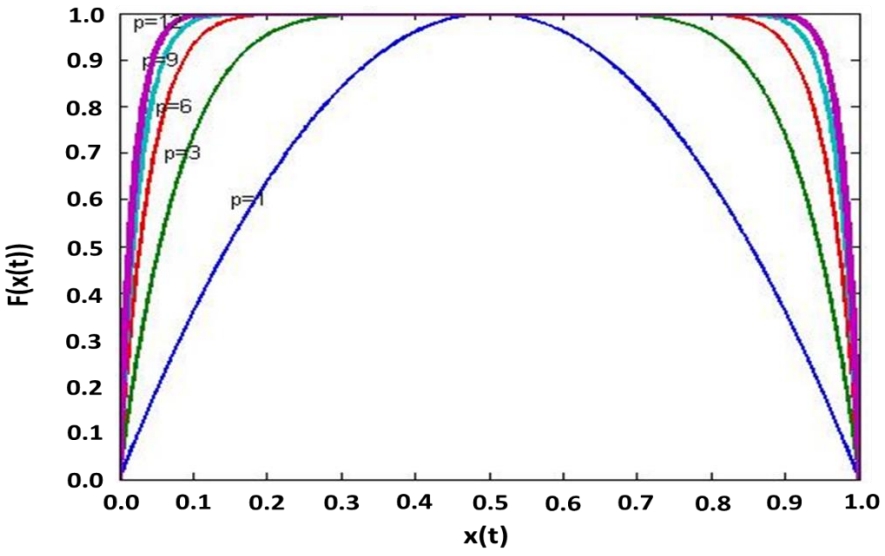



Figure 2.8: The Joglekar window function utilizing different p values

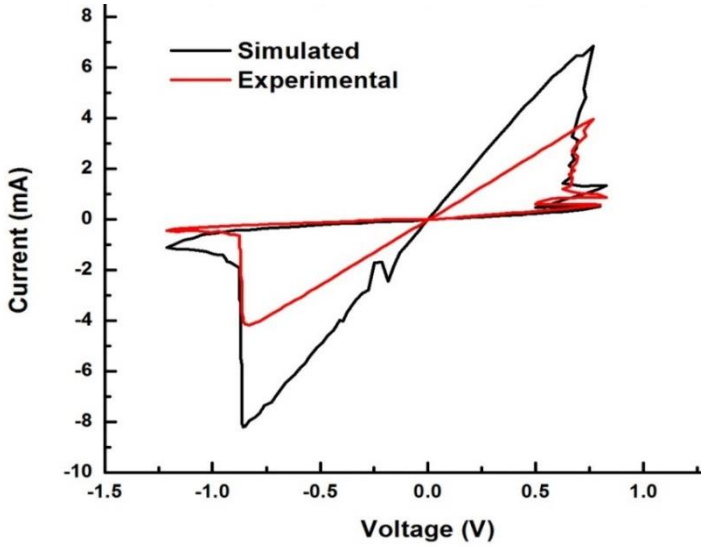



Figure 2.9: The hysteresis curve using the Joglekar model and the corresponding experimental curve, simulated using Matlab with the following parameter values: $\mu_D$ = 1e-15$m^2V^{-1}s^{-1}$, D = 5nm, $x_0 = w_0/D = 0.775$, (where $w_0$ represents the initial value of w), $R_{ON} = 100\Omega$, $r = R_{OFF}/R_{ON} = 100$, p = 7, $v_0 = 1V$, $\omega = 8\pi$ rad/s, $V(t) = v_0\sin(8\pi t+0.16)$ V [53].

### 2.5.5 Biolek Model

In 2009, Biolek introduced an intriguing and efficient window function [54]. This novel approach tackled the boundary lock challenge and aimed to resolve two distinct issues linked with the HP model and Joglekar model. The first complication involved the difficulty of altering the state through external stimuli at the edge. The second predicament concerned the inability to compute the quantity of electric charge stored at the boundary. Consequently, the restoration process suffered from the loss of the previous charge's boundary value. To tackle these problems, Biolek devised a modified window function wherein the boundary speed, governing the transition between doped and undoped regions, exhibited varying behavior.

$$F(x) = 1 - \left(x - stp(-i)\right)^{2p} \tag{18}$$

The provided equation represents the suggested window function, where $p$ stands for a positive integer, and $i$ denotes the current flowing through the memristor.

$$stp(i) = \begin{Bmatrix} 1, i \geq 0 \\ 0, i < 0 \end{Bmatrix} \tag{19}$$

When the width of a doped layer expands, the current in the memristor becomes positive, but this current remains zero at the edge according to reference [54]. Figures 2.10 display the Biolek window function with varying $p$ values and an associated hysteresis curve. However, the I-V curve of the Biolek model differs from the experimental curve, as depicted in Figure 2.11. While this model effectively addresses the memristor's nonlinear behavior and resolves the boundary lock challenge, it falls short in explaining the issues related to scalability and adjustability discussed in the subsequent section.

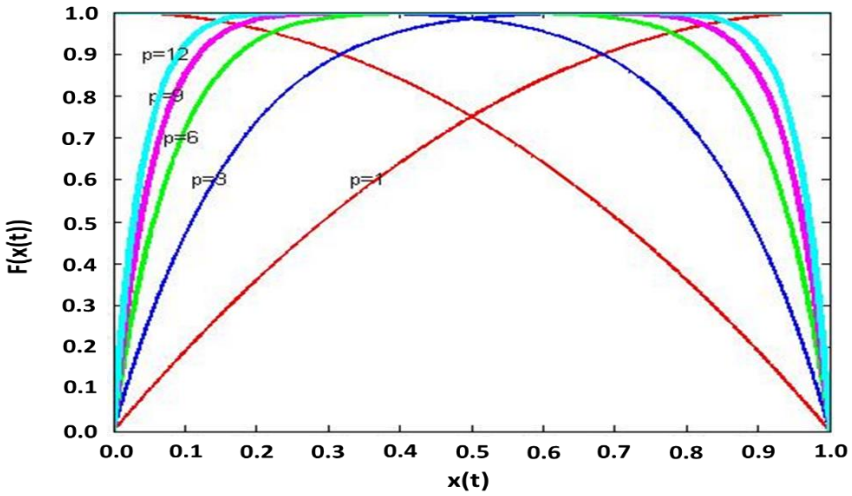



Figure 2.10: Biolek's window function with varying p values

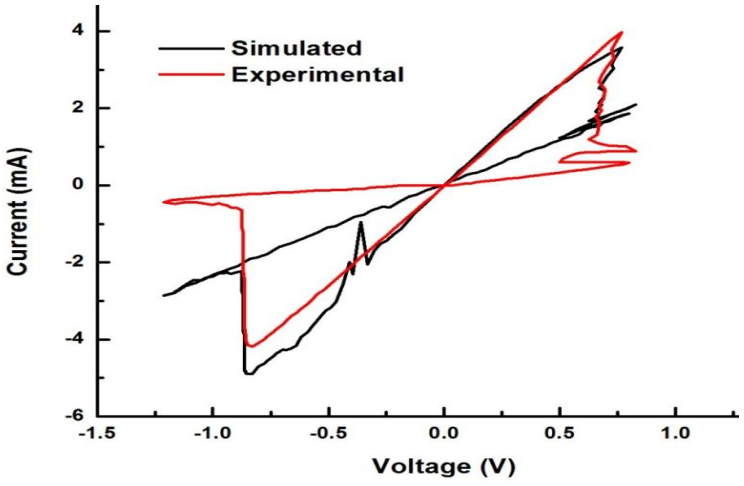



Figure 2.11: Simulated hysteresis I-V curves using Biolek model and the experimental curve. The simulation has been conducted using Matlab and involved specific parameters:$\mu_D$ = 1e-15$m^2V^{-1}s^{-1}$, D = 5nm, $x_0 = w_0/D = 0.7$, ($w_0$ = initial value of w), $R_{ON} = 100\Omega$, $r = R_{OFF}/R_{ON} = 10$, p = 7, $v_0$ = 1V, $\omega$ = 10rad/s, $V(t) = v_0\sin(100t+0.62)V$ [53]

### 2.5.6 Modified Biolek Window Function Model

In 2013, Biolek introduced an altered memristor model that additionally accounts for the non-linear characteristics of the memristor [55]. This model not only resolves the challenge of boundary locking but also provides insights into the issues of scalability (the capacity for control) and adjustability (the capability to finely tune behavior and attributes in a foreseeable manner). The equation below can be employed to ascertain the dynamic value of the state variable:

$$\frac{dw(t)}{dt} = \frac{\mu_D . R_{ON}}{D} i(t)$$

$$or, \qquad \frac{dx(t)}{dt} = k . i(t) \tag{20}$$

here, the rate of change of x(t) over time, denoted as $\frac{dx(t)}{dt}$, signifies the speed at which oxygen vacancies within the device drift, and $k$ stands as a constant factor [56]. The mentioned equations illustrate the memristor's linear attributes. Nevertheless, this linear framework possesses certain limitations; for instance, it necessitates an explanation for boundary conditions. A refined approach involves the integration of a non-linear model, wherein the concept of a window function is introduced. Equation (21) incorporates the window function, $F(x(t))$, which is multiplied by the derivative of the current in a specific state.

$$\frac{dx(t)}{dt} = k . i(t) . F(x(t)) \tag{21}$$

$$F\big(x(t)\big) = 1 - (2x(t) - 1)^{2p} \tag{22}$$

In context (22), $p$ denotes a positive whole number, and equation (22) represents the window function formulated by [50]. This model considers the boundary properties of memristance. Notably, it does not incorporate a switching threshold, making it susceptible to fluctuations and showcasing prolonged switching delays [57]. Essentially, equation (21) can be mathematically integrated for any arbitrary function $F(x(t))$, enabling the expression of $x(t)$ in terms of $q$. For instance, if the function $F(x)$ is represented by the equation (22) with $p$ set as 1, the result obtained is:

$$\frac{1}{4} ln \frac{x(t)}{1-x(t)} = k(q(t) + q_0) \tag{23}$$

where $q_0$ is the integration constant (initial condition). Consequently,

$$R\big(q(t)\big) = R_{OFF} + \frac{R_{ON} - R_{OFF}}{e^{-4k(q(t)-q_0)} + 1} \tag{24}$$

It is more convenient to rewrite $q_0$ in terms of the initial memristance $R_{ini} = R(q = 0)$, resulting in

$$R\big(q(t)\big) = R_{OFF} + \frac{R_{ON} - R_{OFF}}{ae^{-4kq(t)} + 1}; a = \frac{R_{ini} - R_{ON}}{R_{OFF} - R_{ini}} \tag{25}$$

Equation (25) depicts a dependable model [55] designed for SPICE simulation, where memristance is determined based on the inherent state variable $q$. Consequently, the state equation remains insensitive to truncation errors, unlike equation (21). Illustrated in Figure 2.12 is the I-V curve of the adopted Biolek window function model, which closely resembles the experimental curve. Furthermore, this model successfully addresses the concerns related to scalability and adjustability.

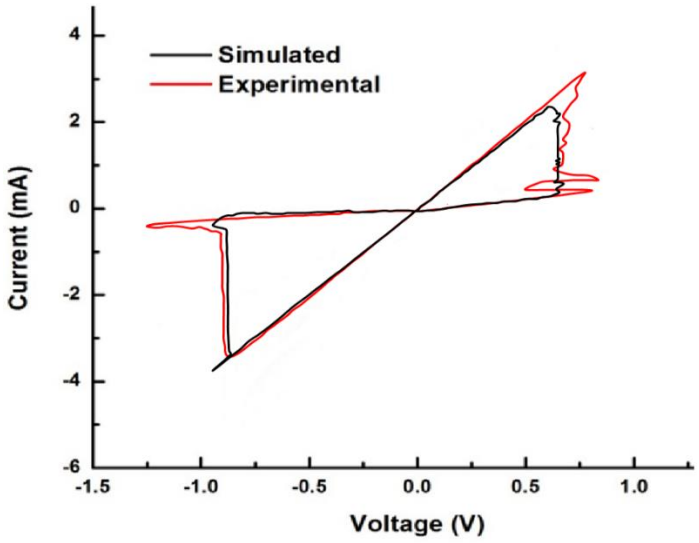



Figure 2.12: Hysteresis plot of the adjusted Biolek window function (the actual experimental curve and the simulation curve). The simulation has been conducted using Matlab, incorporating specific parameter settings: $R_{ON}$ = 100Ω, $R_{OFF}$ = 10KΩ, $R_{ini}$ = 5KΩ, $\mu_D$ = 10e-15$m^2V^{-1}s^{-1}$, D = 10nm

### 2.5.7 Prodromakis Model

In [58], Prodromakis outlined several criteria for an effective window function. To start, boundary conditions should exclusively apply to edge electrodes. Secondly, the window function should have the capability to encompass non-linear effects. Thirdly, a correlation

between linear and non-linear dopant drift models needs to be maintained. Fourthly, the window function could be designed in a manner such that $0 \leq F_{max}(x) \leq 1$, ensuring that the scaling is adaptable within the maximum range [59]. Lastly, additional control parameter is needed to address the nonlinear effect at the boundary. Based on these points he proposed a window function (26) where he succeeded to overcome the scaleable and adjustable issues.

$$F(x) = j(1 - [(x - 0.5)^2 + 75]^p) \tag{26}$$

In equation (26), $j$ serves as a controlling factor that determines the upper limit of the function, and this limit can be either below or above one. Depicted in Figures 2.13 and 2.14 are representations of the window function value, showcasing changes in $p$ and $j$ values. Additionally, Figure 2.15 illustrates the simulated I-V curve using the Prodromakis window function model, which differs from the experimental curve. However, despite this disparity, the model effectively addresses the concerns surrounding scalability and adjustability.

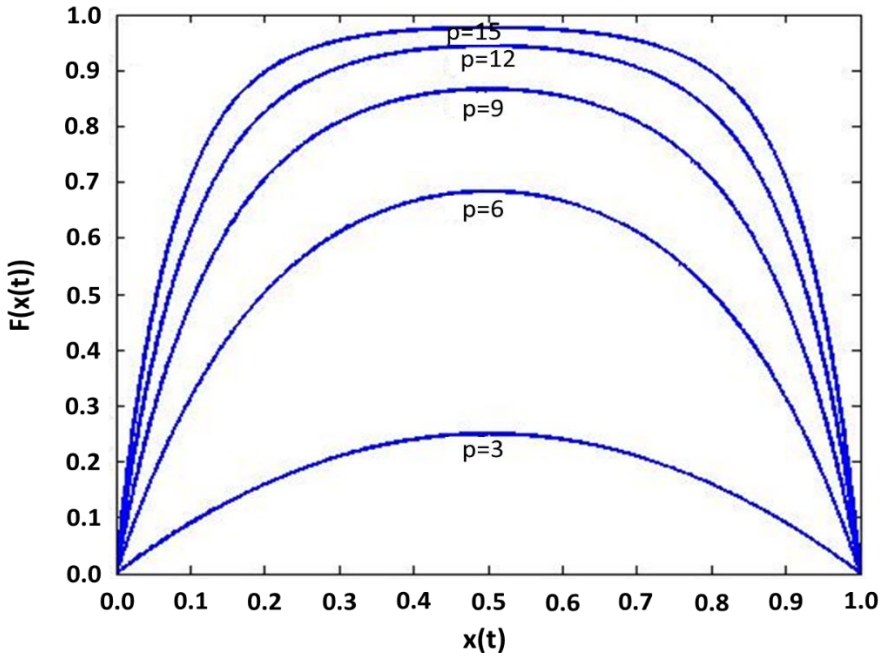



Figure 2.13: The window function proposed by Prodromakis, featuring a setting of j = 1 and different p values

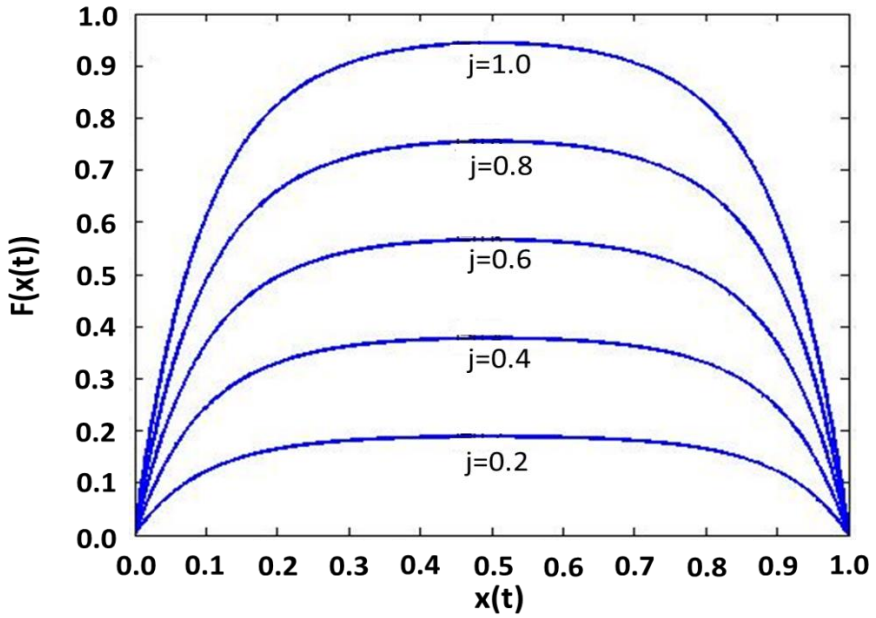



Figure 2.14: The window function introduced by Prodromakis, utilizing a parameter p value of 10, while the j values are adjusted

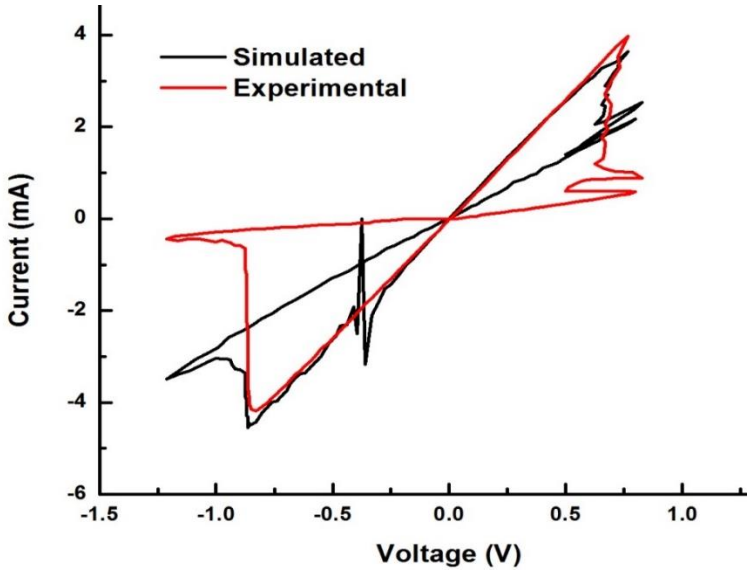



Figure 2.15: Hysteresis plot of the Prodromakis model with the simulation and the actual experimental curve

### 2.5.8 Zha et al. Window Function Model

In 2016, Zha et al. introduced an innovative window function [52]. Within their mathematical framework, they put forth two controlling parameters as a solution to three crucial challenges: boundary lock, scalability, and non-linear effects [52]. In essence, this

model amalgamates elements from both the Biolek and Prodromakis models. The provided window function is as follows:

$$F(x) = j(1 - \left[0.25\left(x - stp(-i)\right)^2 + 0.75\right]^p \tag{27}$$

In equation (27), $stp(i)$ is defined in equation (19), while $j$ and $p$ represent positive integers. Illustrated in Figures 2.16, 2.17, and 2.18 are graphical representations linked to the Zha et al. window function model. A contrast with the experimental outcome presented in Figure 2.18 highlights that the I-V curve of the Zha model falls short of replicating the behaviour of an actual device.

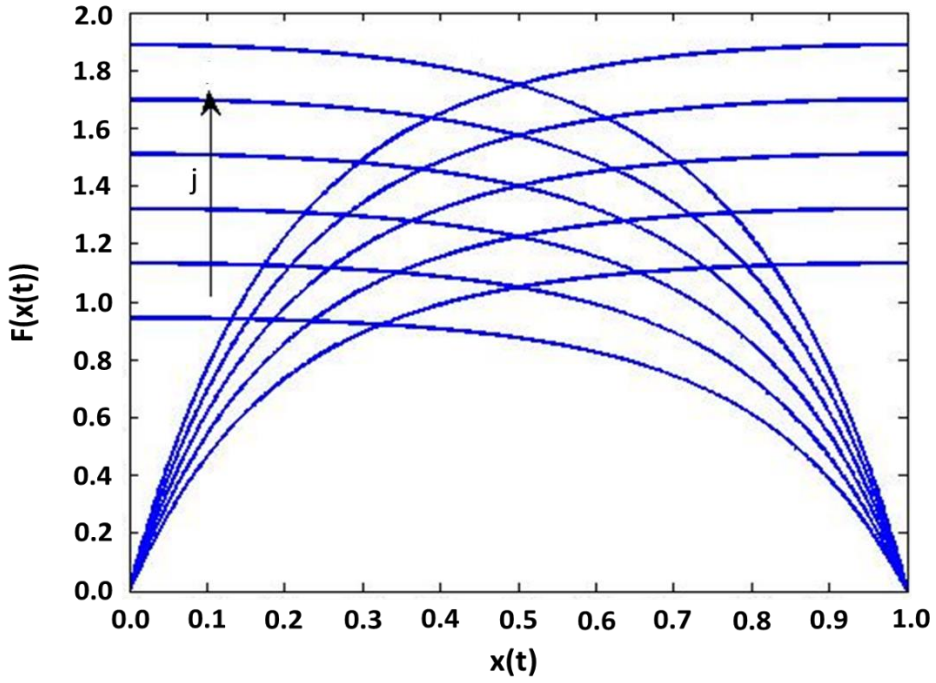



Figure 2.16: The window function introduced by Zha, utilizing a parameter p value of 10, while the j values are adjusted

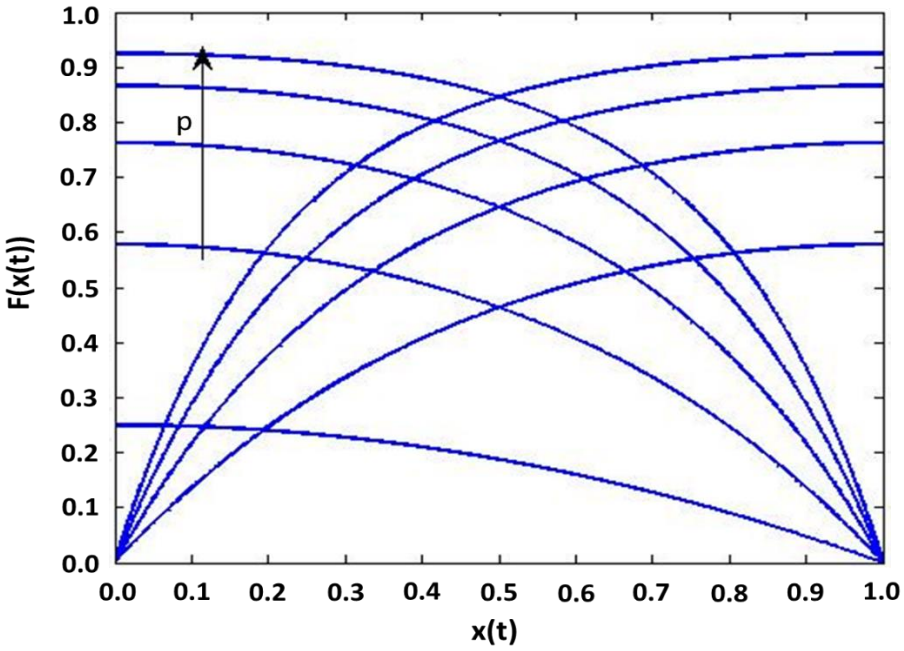



Figure 2.17: The window function proposed by Zha, featuring a setting of j = 1 and different p values

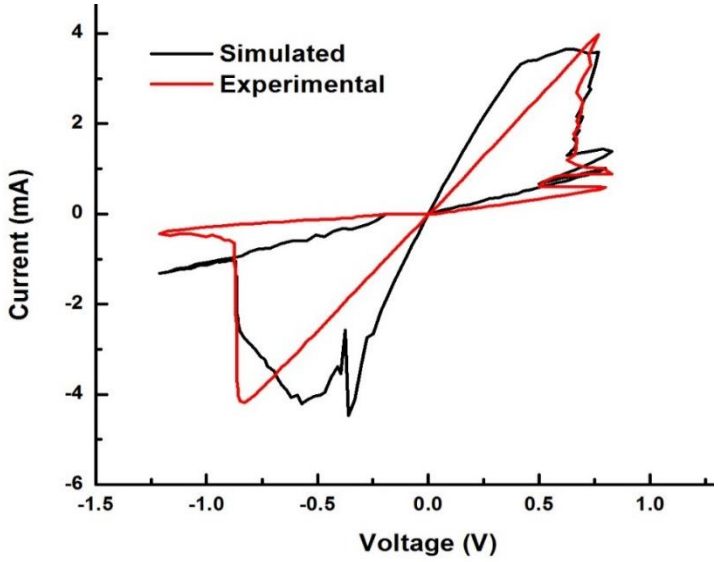



Figure 2.18: Hysteresis plot using Zha window function model and the actual experimental curve. It utilizes a parameter p value of 10, while the j value is 1

### 2.5.9 Nonlinear Ion Drift Model

In 2008 Yang et al. [60] observed rapid bipolar non-volatile switching. They achieved this by incorporating a slender 50nm $TiO_2$ insulating layer between two 50nm wide top and bottom *Pt* electrodes, as depicted in Figure 2.19. By applying a bias voltage

to the top electrode, they induced rectifying characteristics. A positive bias voltage corresponded to the OFF state (HRS), while a negative bias voltage corresponded to the ON state (LRS) switching. Essentially, the application of a slight bias voltage in the thin film generated a substantial electric field, which led to non-linear behaviors, including a reduction in the energy barrier. This renders the model significantly non-linear, evident from its current-voltage relationship (equation 29) [61].

$$i(t) = w(t)^n \beta \sinh\big(\alpha v(t)\big) + \chi[\exp(\gamma v(t) - 1] \tag{28}$$

In equation (28), $w(t)$ represents the state variable, while $n$ governs the extent to which the state variable influences the current. The remaining constants *(β, α, γ, χ)* are parameters tailored for fitting. The initial segment of the equation regulates the current when the device is in the ON state, while the subsequent segment takes precedence when the device is in the OFF state. The differential equation for the state variable can be expressed as:

$$\frac{dw}{dt} = a.F(w).v(t)^q \tag{29}$$

In equation (29), $a$ and $q$ stand as fixed values, while $F(w)$ represents the window function, and $q$ takes on an odd integer value. Illustrated in Figure 2.20 are the current-voltage (I-V) curves of both the experimental memristor and the simulated memristor. The curves exhibit a greater resemblance in the negative segment compared to the positive portion of the experimental curve.

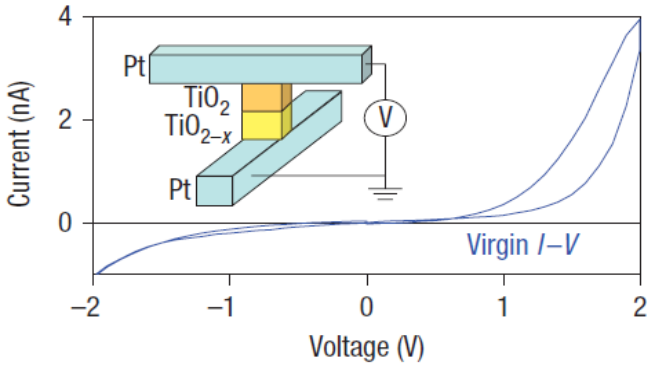



Figure 2.19: Bipolar behavior of non-volatile switching observed in a memristor device configuration [60]

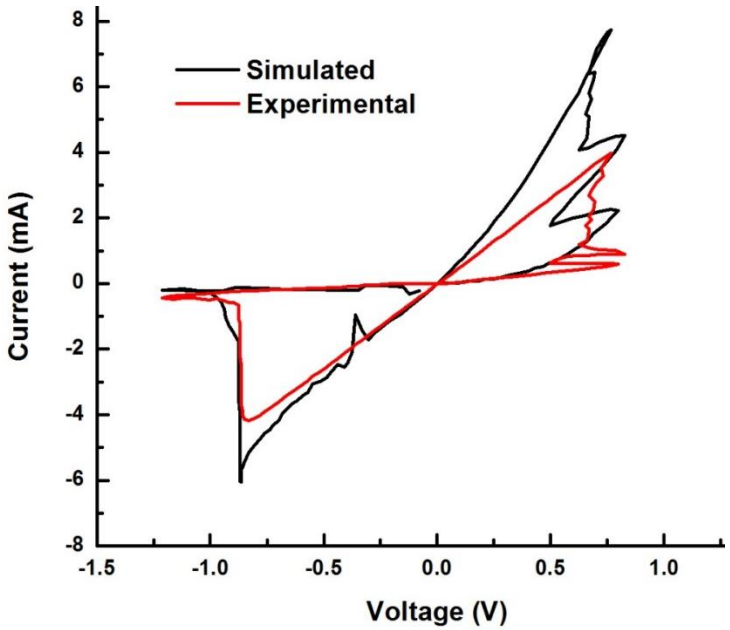



Figure 2.20: Nonlinear model's hysteresis curve, generated through Matlab simulation using specified parameters: $\mu_D = 10^{-14} m^2 V^{-1} s^{-1}$, D = 5nm, $R_{on} = 100\Omega$, $R_{OFF} = 16000\Omega$, f = 10Hz, q = 5, $\beta = 0.9\mu A$, $\alpha = 2V^{-1}$, $\gamma = 4V^{-1}$, $\chi = 10^{-4}\mu A$, a = 1, n = 2 and $V(t) = 1.5\sin(2\pi ft)$ V

### 2.5.10 Simmons Tunnel Barrier Exponential Model

HP's memristor model (described in reference [21]) represents two zones, one doped and the other undoped, as two resistors connected in series to conduct the simulation. However, Picket et al. put forth an alternative physical memristor model in reference [47], rooted in Simmon's formula. Simmon's formula, formulated in 1963, describes the electric tunneling effect through a potential barrier of arbitrary shape within a thin insulating film [62]. This derivation involves a configuration of two electrodes separated by an insulating thin film, resulting in tunneling effects and current flow. The electrodes proposed can either be similar or dissimilar. The derived formula encompasses a rectangular barrier for similar electrodes and a trapezoidal barrier for dissimilar electrodes, accounting for image forces. In Figure 2.21, the physical layout of the Simmon tunnel barrier model for memristors, as suggested in [47], is depicted. Here, $w$ represents the width of the tunneling barrier, $R_s$ denotes the channel resistance, $V$ signifies the applied voltage across the device, $v_g$ stands for the voltage in the oxide region, and $v$ indicates the internal voltage of the device, which may not necessarily be equal to the applied voltage $V$. The current equation involving the gap voltage $v_g$ is formulated in equation (30).

$$i = \frac{j_0 A}{\Delta w^2}\left\{\varphi_I e^{-B\sqrt{\varphi_I}} - \left(\varphi_I + e\left|v_g\right|\right)e^{-B\sqrt{\varphi_I + e\left|v_g\right|}}\right\} \tag{30}$$

where $j_0 = \frac{e}{2\pi h}$, $w_1 = \frac{1.2\lambda w}{\varphi_0}$, $\Delta w = w_2 - w_1$, $\varphi_I = \varphi_0 - e\left|v_g\right|\left(\frac{w_1 + w_2}{w}\right) - \left(\frac{1.15\lambda w}{\Delta w}\right)\ln\left(\frac{w_2(w - w_1)}{w_1(w - w_2)}\right)$, $B = \frac{4\pi\Delta w\sqrt{2m}}{h}$, $\lambda = \frac{e^2 \ln 2}{8\pi k \in_0 w}$, $w_2 = w_1 + w\left(1 - \frac{9.2\lambda}{3\varphi_0 + 4\lambda - 2e\left|v_g\right|}\right)$

$$v_g = v - i(t)R_s \tag{31}$$

Since the $w$ can exist in either ON or OFF state based on the voltage supplied, two distinct derivatives arise to account for these states. The model illustrated that there are nonlinear and unequal characteristics in how the switching occurs. The nonlinearity arises from the utilization of the $\left(sinh\left(\frac{i}{i_{off}}\right)exp\right)$ term to facilitate the movement of oxygen vacancies. In Equation (26), the OFF switching is manifested when $i > 0$, while the ON switching takes place when $i < 0$ [47].

$$\frac{dw}{dt} = \begin{Bmatrix} f_{off} sinh\left(\frac{i}{i_{off}}\right) exp\left[-exp\left(\frac{w - a_{off}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], i > 0 \\ f_{on} sinh\left(\frac{i}{i_{on}}\right) exp\left[-exp\left(\frac{w - a_{on}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right], i < 0 \end{Bmatrix} \tag{32}$$

The parameters in equation (32), namely $f_{off}, f_{on}, i_{off}, i_{on}, a_{off}, a_{on}, b,$ and $w_c,$ are all parameters utilized for fitting. Both $f_{off}$ and $f_{on}$ represent magnitudes that undergo changes due to alterations in $w$. $i_{off}$ and $i_{on}$, responsible for current thresholds, and $a_{off}$ and $a_{on}$, governing boundary limits, contribute to this process. When comparing the I-V curve of this model with the experimental counterpart depicted in Figure 2.22, it becomes evident that the simulated curve diverges from the experimental data. Shortcomings are also evident in this model. Its initial drawback lies in its complexity. Moreover, it fails to establish a clear relationship between voltage and current.

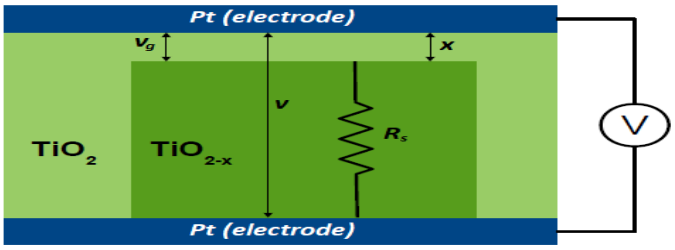



Figure 2.21: The structural configuration of the memristor's Simmons tunnel barrier model in terms of its physical attributes [63]

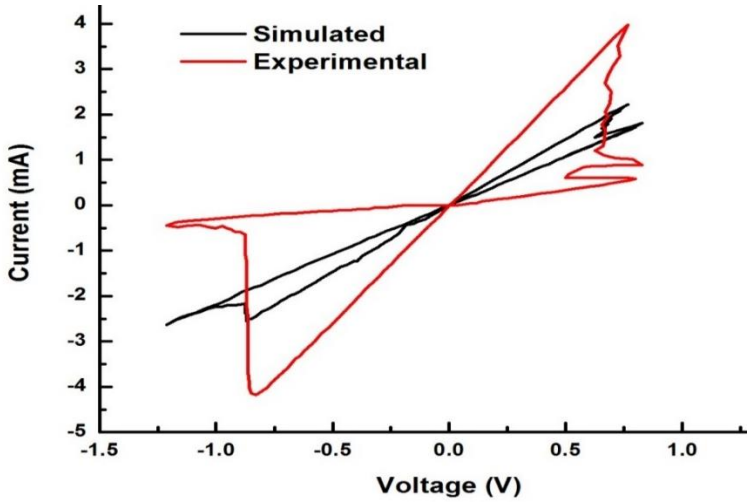



Figure 2.22: The hysteresis plot using the Simmon tunnel barrier model and the experimental data curve. The simulation conducted using Matlab and the specified parameters: $i_{on}$ = -8.9µA, $i_{off}$ = 115µA, $a_{on}$ = 2nm, $a_{off}$ = 1.2nm, $f_{off}$ = 3.5µm/s, $f_{on}$ = 40µm/s, $w_c$ = 107pm and b = 500µA

### 2.5.11 Yakopcic Neuromorphic Model

Drawing from the I-V correlation outlined in reference [64] and the switching state parameter elucidated in [47], Yakopcic introduced a model in 2011 [65]. This model comprises three notable attributes associated with their current-voltage interaction: a structure involving metal-insulator-metal composition, a threshold voltage dictating the state variable, and a nonlinear function governing the behavior of oxygen vacancies or dopant drift [66]. By adjusting the fitting parameters, it was possible to replicate devices with diverse physical compositions. The model's I-V equation relies on a hyperbolic sinusoidal approach, which augments conductivity at a specific voltage threshold (34). Notably, the state variable in this model ranges from 0 to 1, significantly influencing conductivity. The regulation of the state variable is entrusted to two functions, namely $g(V(t))$ and $f(w(t))$. In this context, $g(V(t))$ introduces the threshold voltage effect,

impacting the state variable's value, while $f(w(t))$ facilitates alterations in the state variable value at the boundary.

$$I(t) = \begin{cases} a_1 w(t) \sinh\big(bV(t)\big), & V(t) \geq 0 \\ a_2 w(t) \sinh\big(bV(t)\big), & V(t) < 0 \end{cases} \tag{33}$$

The equation (33) describes the fitting parameters as $a_1, a_2$ and $b$ and the state variable as $w(t)$ [66].

$$g\big(V(t)\big) = \begin{cases} A_p\big(e^{V(t)} - e^{V_p}\big), & V(t) > V_p \\ -A_n\big(e^{-V(t)} - e^{V_n}\big), & V(t) < -V_n \\ 0, & -V_n \leq V(t) \leq V_p \end{cases} \tag{34}$$

In this context, $A_p$and $A_n$represent the amplitudes of the exponential components, while $V_p$ and $V_n$ denote the threshold voltages for the positive and negative directions respectively.

$$f\big(w(t)\big) = \begin{cases} e^{-\alpha_p(w-w_p)}\omega_p\big(w, w_p\big), & w \geq w_p \\ 1, & w < w_p \end{cases} \tag{35}$$

$$f\big(w(t)\big) = \begin{cases} e^{\alpha_n(w+w_n-1)}\omega_n(w, w_n), & w \leq 1 - w_n \\ 1, & w > 1 - w_n \end{cases} \tag{36}$$

The equation (36) introduces $\alpha_p, \alpha_n, w_p$ and $w_n$ which are fitting parameters.

$$\omega_p\big(w, w_p\big) = \frac{w_p - w}{1 - w_p} + 1 \tag{37}$$

$$\omega_n(w, w_n) = \frac{w}{1 - w_n}$$

$$\frac{dw}{dt} = \eta g\big(V(t)\big) f\big(w(t)\big) \tag{38}$$

The term $\eta$ is employed to ascertain the orientation of the state variable [66]. This model is better suited for neuromorphic systems, characterized by neurobiological architectures, due to its distinct attributes. As stated in [65], it is emphasized that the neural spikes within neuromorphic systems exhibit greater similarity to linearly increasing zero-to-positive direct current sweeps as opposed to sinusoidal input. The Yakopcic model effectively captures this crucial feature, rendering it more accurate for neuromorphic applications. The model's accuracy was confirmed through examination with spintronic devices, RRAM

(resistive random access memory) units, and PCM [66, 67]. However, the comparison between the simulated I-V curve in Figure 2.23 and the experimental data reveals discrepancies.

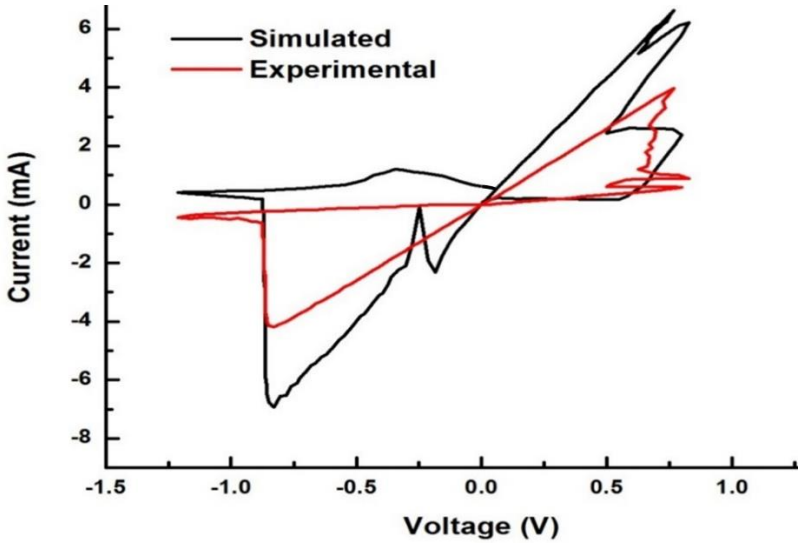



Figure 2.23: The hysteresis plot generated by the Yakopcic model and the corresponding experimental curve, simulated using LTSpice and incorporating the specified parameters: $a_1 = 0.17$, $a_2 = 0.17$, $b = 0.05$, $V_p = 0.16$, $V_n = 0.15$, $A_p = 4000$, $A_n = 4000$, $w_p = 0.3$, $w_n = 0.5$, $\alpha_p = 1$, $\alpha_n = 5$, $x_o = 0.11$ and $\eta = 1$ [66]

### 2.5.12 Threshold Adative Memristor (TEAM) Model

The TEAM model, introduced by Kvatinsky et al.[68], represents a more streamlined iteration of the Simmons tunnel barrier model. This model encompasses two distinct current-voltage associations, delineating linear and nonlinear drift phenomena. The internal current and the state variable are both conceptualized as the product of two autonomous functions: the first being contingent on the device current, and the second dependent on the state variable $w$ [63].

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\frac{i(t)}{i_{off}} - 1\right)^{\alpha_{off}} f_{off}(w), & 0 < i_{off} < i \\ k_{on}\left(\frac{i(t)}{i_{on}} - 1\right)^{\alpha_{on}} f_{on}(w), & i < i_{on} < 0 \\ 0, & otherwise \end{cases} \tag{39}$$

In this context, constants such as $k_{off}, k_{on}, \alpha_{off}$, and $\alpha_{on}$ hold values, with $k_{off} > 0$ and $k_{on} < 0$. Both $i_{off}$ and $i_{on}$ serve as current thresholds, while $w$ stands for the state variable. Functions denoted as $f_{off}(w)$ and $f_{on}(w)$ are both designated as window functions in this

model, their behavior contingent on the state variable. These functions play a role in constraining the state variable within the range of $w_{on}$ and $w_{off}$, where $w_{on}$ corresponds to the state variable during the ON state and $w_{off}$ corresponds to the state variable during the OFF state. $w_c$ is the fitting parameter. Assuming a linear relationship between current and voltage with regard to changes in memristance, the equation can be expressed as follows

$$f_{off}(w) = \exp\left[-\exp\left(\frac{w - a_{off}}{w_c}\right)\right] \tag{40}$$

$$f_{on}(w) = \exp\left[-\exp\left(\frac{w - a_{on}}{w_c}\right)\right] \tag{41}$$

$$v(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{w_{off} - w_{on}}(w - w_{on})\right] i(t) \tag{42}$$

Conversely, when adhering to the Simmons tunnel barrier model, alterations in the barrier width yield exponential variations in memristance.

$$v(t) = R_{ON} e^{\left(\frac{\lambda}{w_{off} - w_{on}}\right)(w - w_{on})} . i(t) \tag{43}$$

where λ is a fitting parameters [69].

$$\frac{R_{OFF}}{R_{ON}} = e^{\lambda} \tag{44}$$

In line with [68], this model boasts notable advantages concerning convergence conditions, computational efficiency, and the prerequisites of a memristive system. Unlike most other models, it addresses the presence of threshold voltage or current by incorporating a current threshold. Furthermore, it's adaptable to existing models such as the linear ion drift model [63]. Nevertheless, the comparison between the I-V curve derived from this model and the experimental data shows discrepancies, as depicted in Figure 2.24. An extension of this model, known as the voltage threshold adaptive memristor (VTEAM) [70], functions as a voltage-controlled device. In the VTEAM model, voltage serves as the threshold; a specific voltage level is necessary to transition the memristor's state. Notably, for memory applications and logic design, a threshold voltage proves more suitable than a threshold current [70]. The hysteresis curve of the VTEAM model, juxtaposed with the experimental curve, is demonstrated in Figure 2.25.

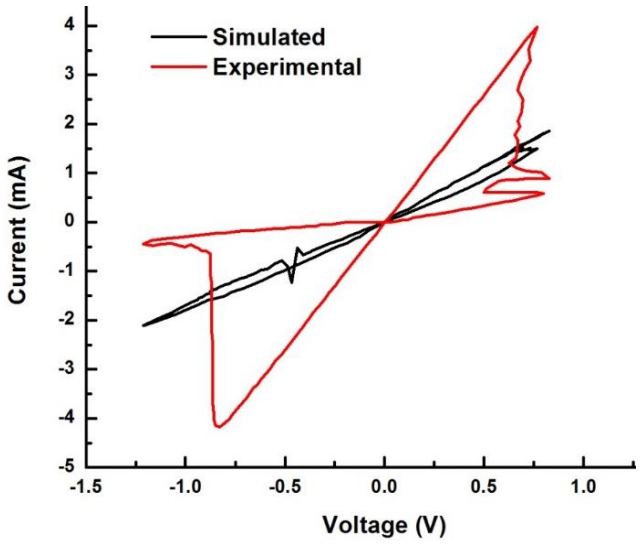



Figure 2.24: The hysteresis plot resulting from the TEAM model and the experimental curve, simulated using Matlab while incorporating the parameters: $k_{off}$ = 5e-4m/s, $k_{on}$ = -10m/s, $i_{off}$ = 115e-6A, $i_{on}$ = -8e-6A, $\alpha_{off}$ = 1, $\alpha_{on}$ = 3, $R_{off}$ = 1000Ω, $R_{on}$ = 50, $w_{on}$ = 0, $w_{off}$ = 3e-9m [70]

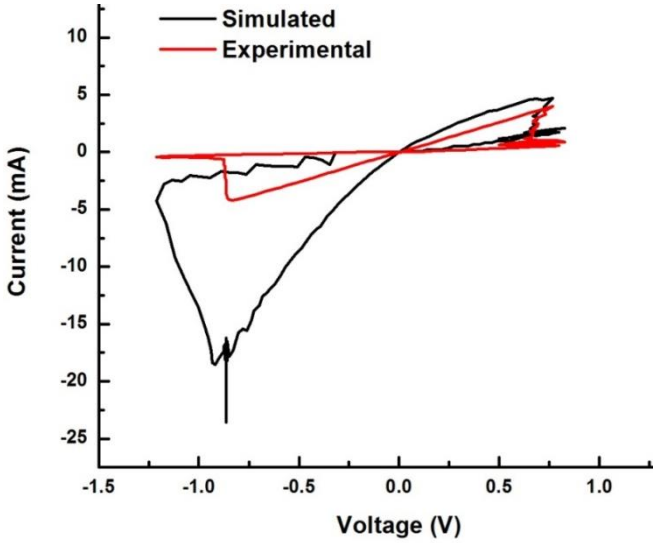



Figure 2.25: The hysteresis graph using the VTEAM model alongside the experimental curve. The majority of parameter values have been adopted from the source mentioned [70]

## 2.6 Model Selection

To compare the results of different models, three different statistical analysis have been done: correlation coefficient, Z-statistics, and p-value. The correlation coefficient, often denoted as *r*, is a measure of the strength and direction of a linear relationship between two variables. There are several methods to calculate the correlation coefficient,

but one of the most common ways is using Pearson's correlation coefficient formula [71]. Here is the method to find the correlation coefficient value using Pearson's formula:

**Collect Data**: First, a set of paired data points have been needed for the two variables (X,Y) to calculate the correlation coefficient.

**Calculate the Means**: The mean (average) of each variable has been calculated.

**Calculate the Covariance**: The covariance of the two variables have been calculated. The covariance measures how two variables vary together.

$$Con\ (X,Y) = \frac{\sum(X_i - \bar{X})(Y_i - \bar{Y})}{n} \tag{45}$$

where $X_i$ and $Y_i$ are individual data points, $\bar{X}$ and $\bar{Y}$ are the means of $X$ and $Y$, respectively, $n$ is the number of data points.

**Calculate the Standard Deviations**: The standard deviation of each variable has been calculated.

$$SD(X) = \sqrt{\frac{\sum(X_i - \bar{X})^2}{n}} \tag{46}$$

$$SD(Y) = \sqrt{\frac{\sum(Y_i - \bar{Y})^2}{n}} \tag{47}$$

**Calculate the Correlation Coefficient (Pearson's *r*)**:

$$r = \frac{Con\ (X,Y)}{SD(X) \times SD(Y)} \tag{48}$$

Pearson's correlation coefficient range spans from -1 to +1: a value of -1 signifies a perfect negative linear correlation, 0 represents the absence of linear correlation, and +1 denotes a perfect positive linear correlation.

The Z-score, also known as standard score or Z-statistic, is a measure of how many standard deviations a data point is from the mean of the dataset. It's a dimensionless quantity that allows statisticians to standardize different sets of data for comparison [72]. The formula to calculate the Z-score of a data point $x$ in a dataset with mean $\mu$ and standard deviation $\sigma$ is:

$$Z = \frac{x - \mu}{\sigma} \tag{49}$$

where $x$ is the individual data point, $\mu$ is the mean of the dataset, $\sigma$ is the standard deviation of the dataset. The Z-score indicates how many standard deviations a data point is above or below the mean. If the Z-score is positive, it means the data point is above the mean, while a negative Z-score indicates that the data point is below the mean.

A p-value, in statistics, is a measure that helps determine the strength of evidence against the null hypothesis. It indicates the probability of observing a test statistic as extreme as, or more extreme than, the one observed in the data, assuming that the null hypothesis is true. In simpler terms, it tells us how likely it is that the results we obtained occurred by chance [73].

Table 2.1: Comparison of all the models with the experimental one with the help of correlation coefficient, Z-statistics and p-value

| **Model** | **Correlation Coefficient** | **Z-Statistics** | **Significance Level (p-value)** |
|---|---|---|---|
| Experimental | 0.75 | N/A | N/A |
| Linear | 0.952 | -8.1814 | <0.0001 |
| Strukov | 0.99 | -15.9220 | <0.0001 |
| Benderli | 0.82 | -1.7563 | 0.0790 |
| Joglekar | 0.653 | 1.8907 | 0.0587 |
| Biolek | 0.95 | -8.1927 | <0.0001 |
| **Modified Biolek** | **0.995** | **-26.3368** | **<0.0000000001** |
| Prodromakis | 0.97 | -10.7070 | <0.0001 |
| Zha | 0.812 | -1.4616 | 0.1439 |
| Nonlinear | 0.86 | -3.0479 | 0.0023 |
| Simmon | 0.99 | -16.0527 | <0.0001 |
| Yakopcic | 0.791 | -0.9355 | 0.3495 |
| TEAM | 0.99 | -15.8772 | <0.0001 |
| VTEAM | 0.851 | -2.7016 | 0.0069 |

The Table 2.1 provides information about different models along with their correlation coefficients, Z-statistics, and significance levels (p-values). Based on the provided correlation coefficient values, the "Modified Biolek" model appears to have the highest correlation coefficient (0.995), indicating a very strong positive linear relationship with the experimental data. However, it is also important to consider the context and validity of each model, as well as potential biases or limitations in the experimental data. In analyzing the Table 2.1, it is seen that models with higher correlation coefficients as having stronger linear relationships with the variables they represent. However, models with lower absolute values of Z-statistics are closer to the mean of the dataset, suggesting that their data points are less extreme. In statistical hypothesis testing, a lower p-value indicates stronger evidence against the null hypothesis, suggesting that the observed correlation coefficient is unlikely to have occurred by chance. Generally, if the p-value is less than a predetermined significance level (often denoted as $\alpha$, commonly set at 0.05), the null hypothesis is rejected. The Experimental model doesn't have a p-value listed, which may imply that the statistical significance of its correlation coefficient was not assessed using a formal hypothesis test. Models with p-values less than 0.05 are typically considered statistically significant at the 5% level [73]. Among the models, the one with the lowest p-value, which implies the strongest evidence against the null hypothesis, is the Modified Biolek model with a p-value of <0.0000000001. Therefore, based on the p-values provided, the Modified Biolek model appears to be the most accurate compared to the Experimental model. The computation of both Z-statistics and p-values was performed using the MedCalc statistical software.

## 2.7 Summary

In conclusion, considering the presented correlation coefficients, Z statistics, and p-values, the "Modified Biolek" model appears to be the most appropriate choice for elucidating the variable relationship. This decision stems from its elevated correlation coefficient, exceedingly low p-value, and substantially large absolute Z statistic.

# Chapter 3

# MOSFET-based TCAM

## 3.1 Introduction

The MOSFET-based TCAM is extensively studied in the chapter, with a deep dive into its essential technical components. Broader aspects of CAM and TCAM systems, including architectural details, match-line (ML) structures, and bit cell arrangements, will be covered. Following that, discussion of multiple strategies for ML sensing and search line driving schemes will be done.

## 3.2 CAM/TCAM Systems

CAM stands for Content Addressable Memory, a specialized form of memory known for its high-speed searching capabilities. Also referred to as associative memory, associative storage, or associative array, CAM differs from RAM in its retrieval method. While RAM requires users to input a memory location to access stored data, CAM operates by searching based on a provided search phrase. It scans its entire content to determine if the word is stored anywhere within it. Upon finding a match, CAM returns a list of one or more storage addresses where the matching word is located. Despite the need to search across its entire memory, CAM aims to execute the search process within a single clock cycle. Additionally, CAM is capable of READ and WRITE operations. Figure 3.1 illustrates the architecture of a typical CAM, featuring a memory array organized into word entries with a predetermined word width.

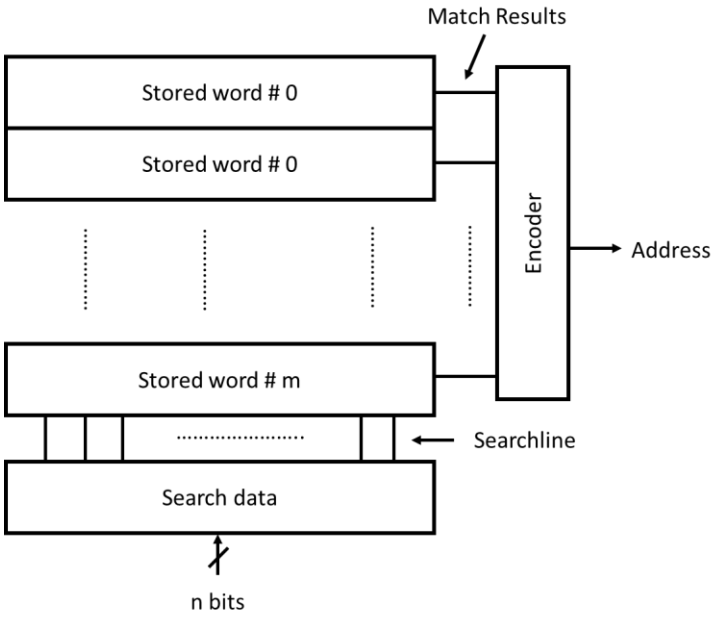



Figure 3.1: Conceptual architecture of a content addressable memory

RAM differs from fully parallel CAM, where each memory cell is associated with a specific comparison circuit. This circuit swiftly detects matches between stored bits and searched-for bits. Integration of match outputs from each cell in the data word is necessary to obtain a comprehensive data word match signal. Ternary CAM, or TCAM, offers the additional capability to store and search for "mask" or "don't care" bits, making it an attractive option for applications such as packet forwarding and categorization, where storing mask bits in routing tables is crucial. Priority encoders aid in determining the highest priority match among several matches, which is particularly useful in locating the Longest Prefix Match (LPM). However, these benefits come with the drawback of increased circuit size. Each cell in TCAM requires two SRAM cells, and the additional comparison circuitry enlarges the physical size of the TCAM chip, leading to increased cost and power consumption. Nonetheless, TCAM is virtually indispensable in modern routers due to its unmatched search speed and ease of table maintenance [74, 75].

## 3.3 CAM Cell Structure

The primary functions of a CAM cell involve storing bits and comparing them. SRAM is commonly employed as the fundamental storage element in each CAM cell. To facilitate programming of stored data and enable bit comparison between stored data and

search data, additional circuitry is incorporated. Two distinct cell topologies have been explored, which depend on the connection between the search result from each cell and the ML of the entire word: NAND and NOR cells. [75].

### 3.3.1 NOR cell

Figure 3.2 illustrates the schematic of a typical NOR cell. Within an SRAM cell, serving as the primary storage component, two inverters are present. Additionally, two access transistors (Mn5, Mn6) are included. To enable bit comparison, four transistors (Mn1, Mn2, Mn3, Mn4) serve as access transistors. During READ operations, bit lines (BLs) and a word line (WL) are utilized. Transistor pairs Mn1/Mn3 and Mn2/Mn4 function as a pull-down path from the ML to ground. During the SEARCH operation, the search data is applied to two complementary SLs. Activation of the pull-down path depends on the comparison outcome between the stored data and the search data SL. If data and SL differ, one pull-down path is enabled, discharging ML to ground. Conversely, if data and SL match, both pull-down paths are disabled, and ML maintains its original voltage. When cells are horizontally added to form a word, the ML retains its state if all bits of a word match the search content. However, a single mismatch alters the ML's state. Figure 3.3 illustrates the arrangement of multiple cells connected horizontally to form an n-bit data word.

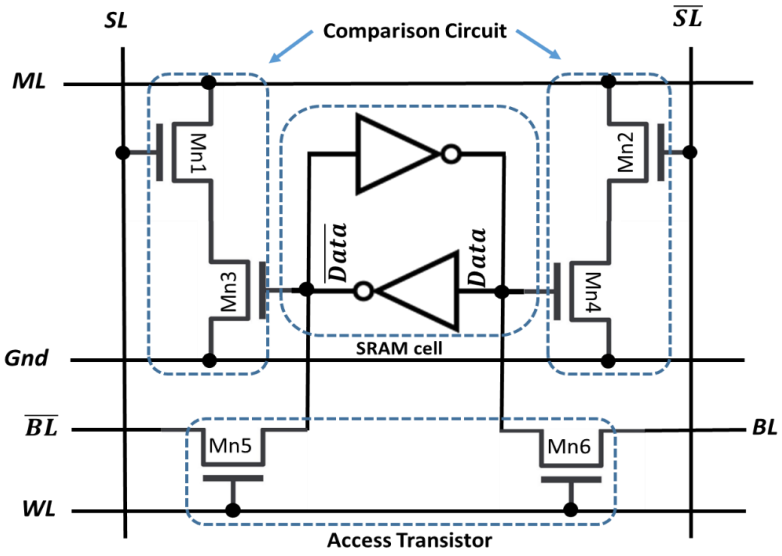



Figure 3.2: The representation of NOR-type CAM cell [74]

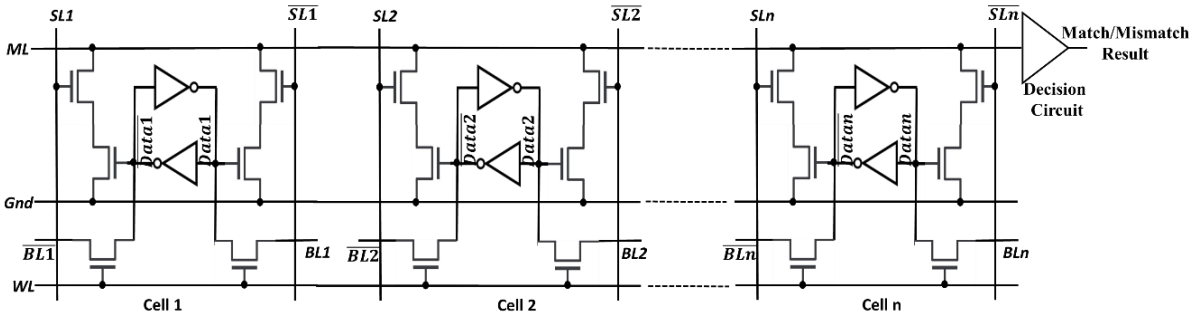



Figure 3.3: One BCAM data word consisting of n-bit NOR-type cells

### 3.3.2 NAND cell

Figure 3.4 depicts circuit diagram of a NAND cell in its simplest form. A SRAM cell serves the same purpose as a NOR cell when it comes to the storing element. The search procedure is carried out by the cell's inclusion of three access transistors (Mn1, Mn2, Mn3), which make up the cell. The outcome of the search influences the value of the voltage at node *B*, which in turn impacts the behaviour of Mn1 to decide whether or not there is a connection between two neighboring MLs ($ML_{n+1}$ and $ML_n$). Consider the scenario of a match in which *Data* equals 0 and *SL* equals 0 (or $\overline{Data}$ = 1, $\overline{SL}$ = 1), transistor Mn2 is ON and passes $\overline{SL}$ = 1 to node *B*, which causes node *B* to switch ON transistor Mn1, connecting corresponding *MLs*. In the alternative match scenario, where *Data* = 1, *SL* = 1, (or $\overline{Data}$ = 0, $\overline{SL}$ = 0), MLs are also connected to one another. In the event of a mismatch, the voltage at node *B* will be pulled to ground, which will turn off Mn1 and disconnect the ML. Each individual segment of the ML is under the control of a single bit as the NAND cells are successively appended to one another in order to produce a word. A pull-down path is established to discharge the ML only when all bits in a word match the search content. If any bit in a word mismatches the search content, the state of the ML is preserved. This behavior is inherent to the operation principle of the NAND cell design. Figure 3.5 illustrates the arrangement of multiple cells connected horizontally to create an n-bit data word for NAND-type cells.

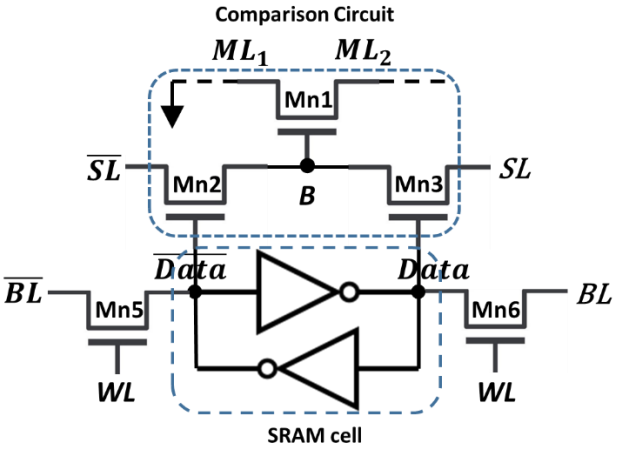



Figure 3.4: Schematic of a NAND CAM cell [74]

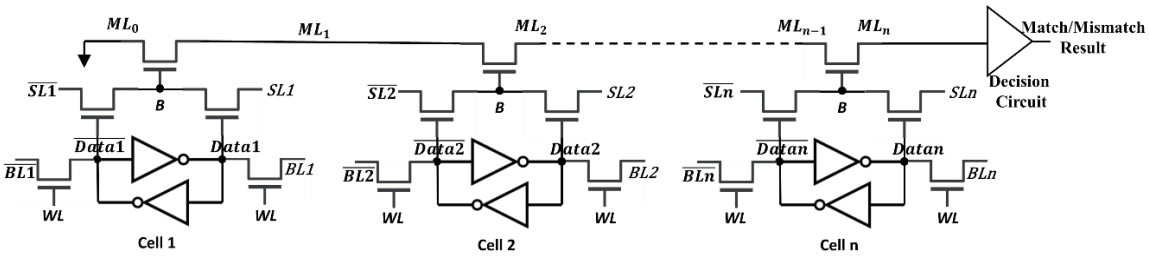



Figure 3.5: One data word consisting of n-bit NAND-type cells

One key characteristic of the NOR cell is that full rail voltage is accessible at every gate of the access transistors. In contrast, a voltage reduction occurs in the NAND cell because the gate voltage of Mn1 in Figure 3.4 is supplied by access transistor Mn2 or Mn3, hence it can only reach $V_{DD}$-$V_{th}$. As will be explored later in this chapter, this reduction in gate voltage leads to a decreased noise margin when sensing MLs.

## 3.4 TCAM Cell Structure

The term "ternary" is derived from the concept that every cell within TCAM has the ability to hold three distinct conditions: high, low, or a mask represented as 'X', denoting an unspecified state. Representation these three conditions necessitates the use of two bits. Consequently, each TCAM cell is comprised of two SRAM cells. There are two classifications for TCAM cells: NOR-type and NAND-type. Both of these types are illustrated in Figure 3.6 and 3.7.

In the NOR-type TCAM cell depicted in Figure 3.6, transistors Mn1–Mn4 form the comparison circuit. The three states are represented as Data1Data2 = 01 (indicating low),

Data1Data2 = 10 (indicating high), and Data1Data2 = 00 (indicating don't care condition). The state where Data1Data2 = 11 is not permitted. The encoding for search data follows a similar pattern, meaning SL1SL2 = 01, 10, or 00. When the stored data is in the state Data1Data2 = 00, this is referred to as local masking. If SL1SL2 = 00, it signifies global masking. When Data1Data2 = SL1SL2 (indicating a match) or local/global masking is applied, neither of the ML pull-down pathways (through Mn1, Mn2 or through Mn3, Mn4) is activated, and ML remains disconnected from the ground. Only in cases where Data1Data2 is not equal to SL1SL2 (indicating a mismatch) and there is no masking, ML is pulled down to the ground by one of the two transistor pairs, either Mn1Mn2 or Mn3Mn4.

In Figure 3.7, the NAND-type cell employs distinct cells for data and mask. The comparison circuit is formed by transistors Mn1 through Mn4. Local masking is accomplished by setting '1' in the mask cell ($M_{mask}$ = '1'), which activates the pass transistor Mn4 and connects both sides of ML segments ($ML_n$ and $ML_{n+1}$), regardless of the value stored in the data cell. Global masking is achieved by providing SL1 = '1' and SL2 = '1' (SL1SL2 = 00 is not permitted). This causes the pass transistor Mn3 to activate because either Mn1 or Mn2 is always ON. Consequently, it connects ML segments on both sides, regardless of the values stored in the data and mask cells. When there is no masking, meaning $M_{mask}$ = '0' and SL1 = $\overline{SL2}$, the operation is the same as that of a BCAM NAND cell. Pass transistor Mn3 turns on only if the stored data matches the search data, i.e., Data = SL1 (and $\overline{Data}$ = SL2 = $\overline{SL1}$). Consequently, both pass transistors Mn3 and Mn4 remain off only in the event of a mismatch.

Additional alterations made to CAM/TCAM cells include a decrease in the number of transistors per cell [76, 77], mixing parts of NAND and NOR cells, alternating the logic level of the pull-down path in the NOR-type cell, among many others [78-80].

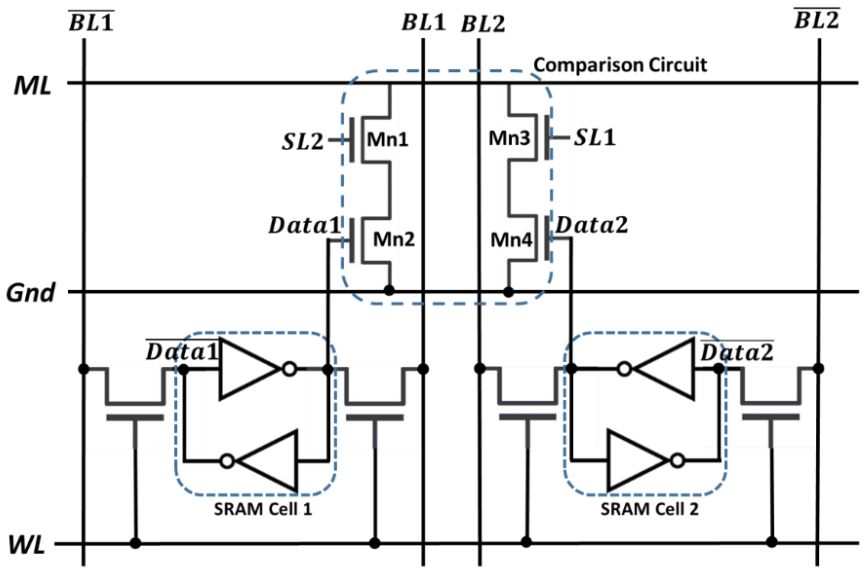



Figure 3.6: Schematic of a NOR-type TCAM cell [74]

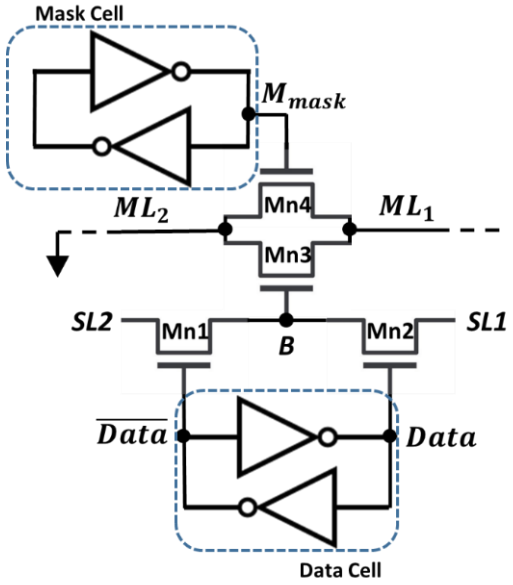



Figure 3.7: Schematic of a NAND-type TCAM cell [74]

## 3.5 ML Structure

A CAM or TCAM system would not function properly without the ML. The final state of ML after the conclusion of the search operation represents the match/mismatch status of the search. Therefore, its layout has a direct impact on the speed of the memory as well as the amount of energy it uses. As a consequence of this, many researchers have concentrated on coming up with ML structure that achieve a better

balance between power and latency. This section provides a concise explanation of the operational principles underlying two of the most important ML structures: the NOR-type and the NAND-type.

### 3.5.1 NOR-type ML

Figure 3.8 illustrates a NOR-type ML by showing how several NOR-type bit cells share a single ML and are connected to it in parallel [81]. This configuration allows many bit cells to share a single ML. This strategy worked for both CAM and TCAM systems. There are three stages that make up the search process of a NOR-type ML. These stages are the SL precharge, the ML precharge, and the evaluation. To begin, the SLs in each bit cell are brought down to their lowest possible setting to disable the pull-down routes. Second, with ML disconnected from ground, the precharge signal $\overline{pre}$ is asserted to charge ML to $V_{dd}$ through transistor Mp1. At this point, $\overline{pre}$ is de-asserted, and the search content is broadcast to SLs in order to initiate the evaluation phase. Since there is no discharge channel to ground when a match occurs, the voltage of ML continues to remain at its previous high level. In the event that there is a mismatch, there will be at least one discharge path constructed between ML and ground. The voltage of the ML is read by the match-line sense amplifier (MLSA) at the end of each search cycle, and the match/mismatch status is indicated by the logic level at the MLSA's output. Operating at a high speed is one of the primary benefits that come with using NOR-type ML. In the worst-case scenario, ML would be discharged through single path that includes two pull-down transistors. This discharge path is noticeably shorter than the one used in NAND-type ML systems, as will be demonstrated in the following analysis.

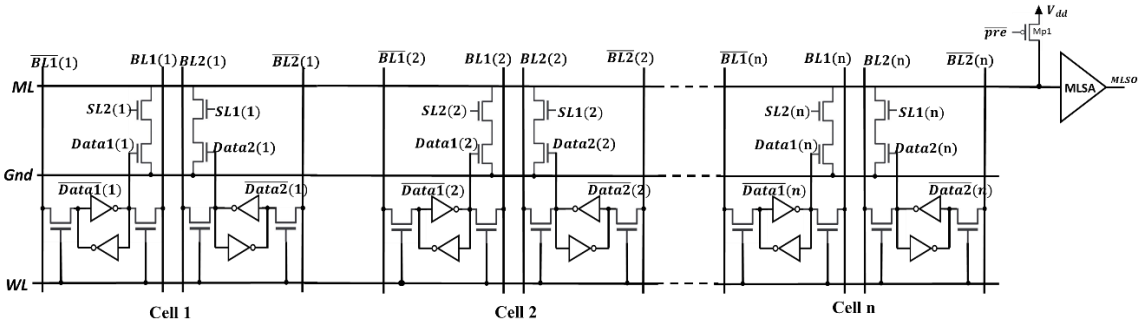



Figure 3.8: NOR-type ML [74]

### 3.5.2 NAND-type ML

In Figure 3.9, a schematic representation of a NAND-type ML has been drawn. The entire ML is divided into n+1 sections and each section is comprised of one bit cell. To put it another way, each bit cell that makes up a stored word is connected one after the other to create a discharge channel that goes from ML to ground. The search operation is divided into three stages: the searchline (SL) precharge, the ML precharge, and the evaluation stage. To begin, each SL is brought down to logic-0 value in order to stop any bit cells from linking adjacent ML segments. Second, the precharge signal $\overline{pre}$ is turned to logic-0 so that the voltage at ML can be brought up to the Vdd level. After that, $\overline{pre}$ is asserted to be high, and the voltage of ML is being determined by the result of the search. Because each bit cell joins its nearby ML segments, a discharge path is established in the event of a match between ML and ground. This occurs because each bit cell acts on its own ML segments. If there is a mismatch, at least one bit cell will disconnect ML segments. This will allow the voltage on the ML to be maintained since there will be no way for it to discharge.

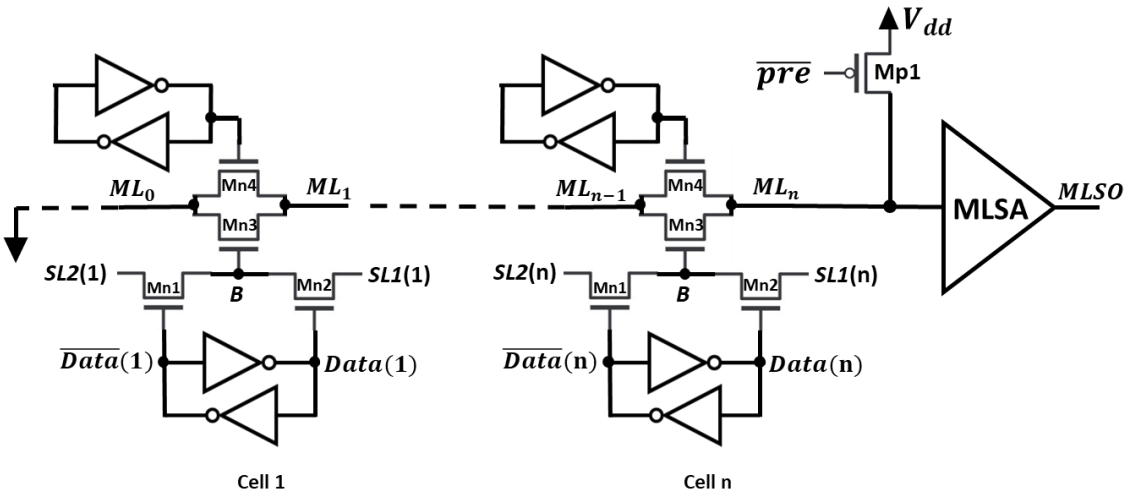



Figure 3.9: NAND-type ML [74].

In Figure 3.9, the entire ML system, comprising all intermediate nodes ($ML_n$, $ML_{n-1}$, ..., $ML_1$), is connected only when there's a complete match between the data word and the search key. The decision circuit assesses the ML state and generates a matching outcome. The design of the decision circuit differs based on the sensing method of ML. Regardless

of the sensing approach, a match result of '1' indicates a full match, whereas a result of zero indicates one or more mismatches.

## 3.6 Circuit Level ML Sensing Schemes

While both NOR-type and NAND-type cells possess their own advantages and limitations, the NOR-type cell predominates in current TCAM systems owing to its high speed and low power consumption [74]. Techniques have been devised at various design levels to notably diminish the power consumption of NOR-type TCAM systems.

### 3.6.1 Precharge-high scheme

In TCAM, precharge-high ML sensing scheme is a technique used to detect matches in the memory array efficiently. In TCAM, a ML is a sense line that runs horizontally across the memory array, connecting the cells in each row. When searching for a specific pattern or content, the ML senses whether there is a match or not. Before performing a search operation, the MLs are precharged to a high voltage level. Precharging means setting the MLs to an initial voltage state, typically high, to ensure accurate sensing during the subsequent search operation. During the search operation, the contents of the memory cells are compared with the search data. The ML sense whether there is a match between the stored data and the search data. Sense amplifiers connected to the MLs amplify the small voltage differences generated by the comparison process, making it easier to detect matches or mismatches. Based on the sensed voltage levels on the MLs, the TCAM outputs the address(es) of the matching data entries.

The precharge-high ML sensing scheme improves the speed and accuracy of the SEARCH operation in TCAM by ensuring that the MLs start from a known state before performing the comparison. This scheme helps in reducing the likelihood of errors and improves the efficiency of the TCAM in matching operations. However, this technique consumes a lot power which is very inefficient for any design.

### 3.6.2 Reduced ML swing voltage – precharge-low schemes

In order to decrease power usage in ML and potentially enhance sensing speed, there's a reduction in the voltage swing on the ML component, as noted in reference [82]. This reduction in voltage swing is aimed at addressing the dynamic power aspect of ML, which is described as:

$$P_{ML} = m.C_{ML}.V_{dd}.V_{swing}.f \quad (45)$$

In equation (45), $m$ represents the number of MLs, $C_{ML}$ signifies the total capacitance associated with a ML, $V_{swing}$ stands for the magnitude of voltage swing observed on ML, and $f$ denotes the operational frequency. Thus, the reduction in power consumption is directly proportional to the magnitude of voltage swing. Figure 3.10 illustrates a simplified circuit designed to reduce the voltage swing on ML. Initially, $C_{tank}$ is charged to the $V_{dd}$ voltage level during the precharge phase, and this charge is distributed to the ML during the evaluation phase. Consequently, the highest voltage level on the ML will be less than $V_{dd}$, depending on the ratio between $C_{tank}$ and $C_{ML}$. It's important to note that this approach necessitates a lower reference voltage for MLSA and it also requires additional space for $C_{tank}$ for each ML. Furthermore, the accuracy of the sensing process is compromised due to uncertainties in estimating the exact value of $C_{ML}$, even when post-layout extraction tools are employed.

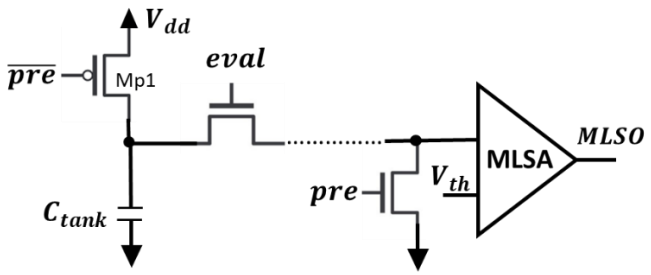



Figure 3.10: Low-swing ML scheme [82, 83]

### 3.6.3 Current-race sensing scheme

The schematic depicting the current-race approach is shown in Figure 3.11 [75, 84]. During the precharge phase, the ML is discharged to a low voltage level while the input to the MLSA is charged to a high voltage level. In the subsequent evaluation phase, the *MLRST* signal is deactivated, and the $\overline{en}$ signal is activated. As the current source ($I_{ML}$) initiates the charging of ML, the final voltage on ML depends on the search result. In cases where there is a match, each cell presents a high impedance to ML, resulting in ML being charged. Conversely, in cases of a mismatch, the voltage on ML will be $I_{ML} \times R_{ML} / k$, where $R_{ML}$ represents the equivalent resistance of an enabled pull-down path, and $k$ is the number of bit-wise misses within a word. By setting the maximum voltage for a miss to a sufficiently low level, the MLSA can easily distinguish between a match and a mismatch.

Figure 3.11 illustrates the MLSA design, which incorporates a sense transistor, Mn1, for detecting ML's voltage level and a half-latch to retain the result.

The advantage of this approach, compared to the conventional precharge-high method, is that the precharge-low scheme eliminates the need to separately precharge SLs to a low voltage level, as explained in Section 3.5.1, thereby conserving power. However, one of the challenges is determining the appropriate values for $I_{ML}$ and $R_{ML}$ to achieve an optimal sensing margin. Notably, the transistors in the pull-down path in Figure 3.9 must be sufficiently large to ensure an adequate margin between the match and mismatch states, which in turn increases the area occupied by the bit cell.

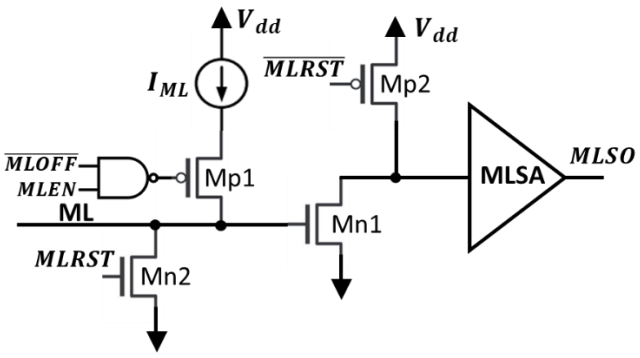



Figure 3.11: Current-racing scheme [84]

Managing the timing of clocked circuits poses a challenge in CAM design. One prevalent method to tackle this challenge involves employing a dummy word that consistently matches [85, 86]. This dummy word, along with its associated dummy ML, regulates the timing of both the precharge and evaluation phases. By doing so, it mitigates the impact of process variations across the array. The CR scheme further optimizes ML charging by adopting a similar concept of using a dummy word. Refer to Figure 3.12 for an illustration of the CR scheme with dummy word.

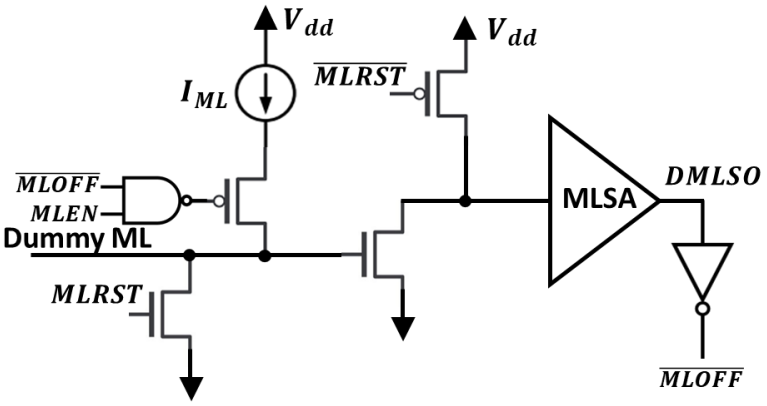



Figure 3.12: Dummy word

### 3.6.4 Selective-precharge scheme

Initially, a portion of the TCAM cells within a complete word is compared to determine whether further comparison is required. Only if all the bits in this initial subset match the corresponding search key bits will the comparison proceed to the remaining bits. Figure 3.13 illustrates the original selective precharge approach proposed for NOR-type ML in [87]. In this method, ML segments are initially discharged (the discharging circuit is not shown). Subsequently, the $\overline{SelPre}$ signal activates the first ML segment, which contains *k* bits. If all these bits match the corresponding bits in the search key, the charging through Mp1 results in a high voltage level in ML segment 1. This high voltage level causes the inverter output to be zero, turning ON Mp2 and turning OFF Mn1. In the case of a mismatch, the first ML segment has discharging pathways to the ground and, as a result, cannot charge to a high voltage. Consequently, the inverter output remains at 1, causing Mp2 to remain OFF and Mn1 to remain ON. During the second phase of the search, the *Eval* signal activates Mp3 and Mn2. If the first segment is fully matched, ML segment 2 charges through Mp2 and Mp3 (with Mn1 OFF). If there is no match in the first segment, there is no charging in the second segment (Mp2 OFF), and ML segment 2 remains connected to the ground through Mn2 and Mn1. If the second segment is matched in addition to the first segment, the voltage in the second segment can become high, triggering MLSA to produce a high output. However, if the second segment is mismatched, it has discharging pathways to the ground, causing its voltage to remain low, and consequently, the MLSA output remains at zero. Selective-precharge scheme is widely adopted among

TCAM systems [76, 88-92] since it reduces the dynamic power significantly and does not introduce excessive hardware complexity.

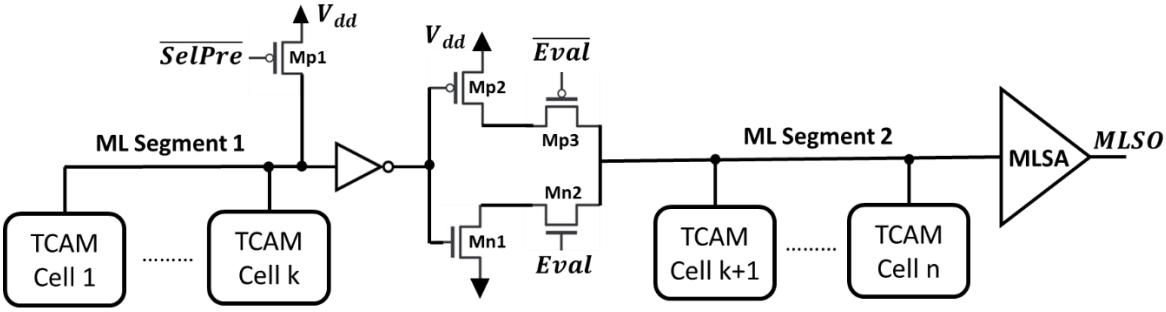



Figure 3.13: Selective-precharge scheme [87]

### 3.6.5 Pipeline scheme

The pipeline scheme builds upon the fundamental concept of the selective-precharge scheme [93]. However, instead of dividing the ML into just two segments, the pipeline scheme further subdivides the ML into multiple segments, offering a finer level of granularity for optimizing power efficiency. The concept of the pipeline scheme is depicted in Figure 3.14, where the ML consists of four pipeline stages, and NOR cells within each stage share a common local ML. The word's search is conducted sequentially, starting from the bit cells on the left and moving to the right. A successful match in one stage triggers the search in the next stage, while a mismatch in any stage halts the entire search process and produces the result at the end of the ML. Additional MLSAs and logic circuits are inserted between stages to facilitate the necessary operations. The pipeline scheme conserves power by deactivating subsequent stages when a mismatch has already occurred. However, this scheme does have drawbacks, including increased latency and additional area requirements due to the inter-stage circuitry.

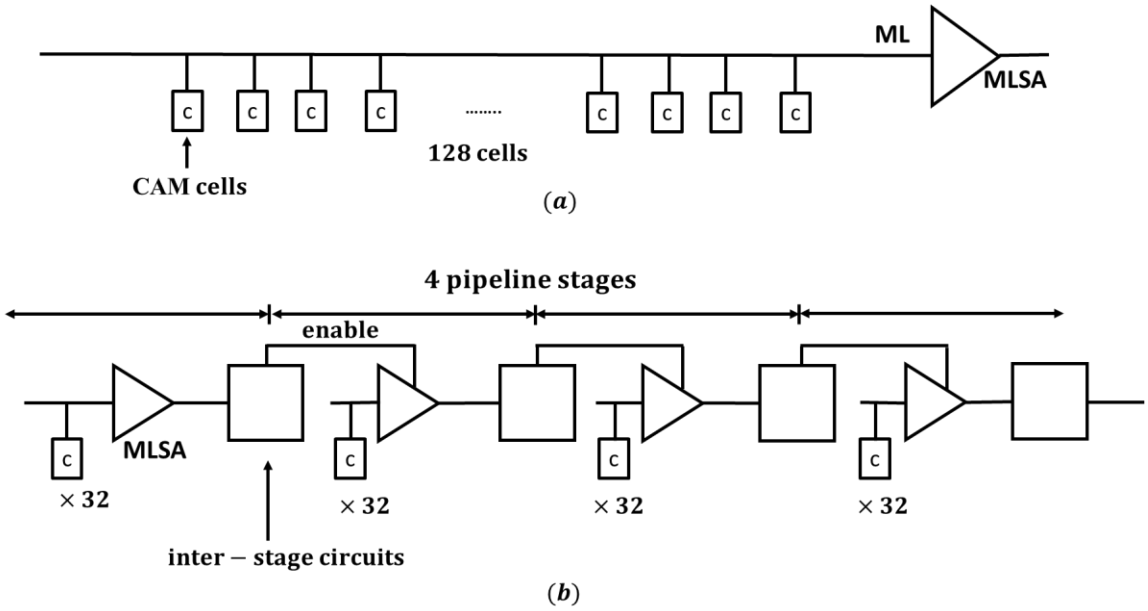



Figure 3.14: Conceptual diagram of conventional NOR-type ML (a) and pipelined ML scheme (b) [93]

### 3.6.6 CR-based positive feedback schemes

The following sections discuss different CR-based positive feedback ML schemes.

#### 3.6.6.1 Current saving technique/mismatch dependent (MD)

In [94, 95], the concept of using positive feedback in CR MLSA was initially put forth. This technique is also known as the current saving technique [94] or mismatch-dependent (MD) power allocation technique [95]. To detect mismatched MLs during charging and reduce currents to mismatched MLs, a feedback unit has been added to the basic CR MLSA in this method. Figure 3.15 depicts this technique in details. The feedback unit contains a level shifter and a feedback circuit to implement feedback. To control the length of the ML charging cycle, the MLOFF signal was generated using the same dummy word as in the CR system. When compared to a CR scheme, this technique can offer a large energy reduction in terms of ML energy. The level shifter and feedback circuit, however, use a significant amount of energy. Transistor Mn1 fully activates in the event of a full match. Mn1 continues to be partially ON for 1-bit or 2-bit mismatches. In the feedback circuit, this results in the development of a conducting channel from $V_{dd}$ to ground. Again, with higher numbers of mismatches, $V_{ML}$ is low because ML has several pathways for discharging to ground. This turns on both level shifter transistors and establishes a path for current to flow from $V_{dd}$ to the ground. Static power consumption results from conducting

routes from $V_{dd}$ to the ground. Since the level shifter divides the voltage, more $V_{dd}$ must be dropped over Mp1 as a result. This calls for Mp1 with a long gate and Mp2 with a wide gate. Due to the huge Mp2, the ML's capacitive loading increases. As a result, the energy savings are not substantial overall. The level shifter's massive transistors greatly slow down the match detection process [96]. In addition, the MLSA has more transistors than the CR MLSA.

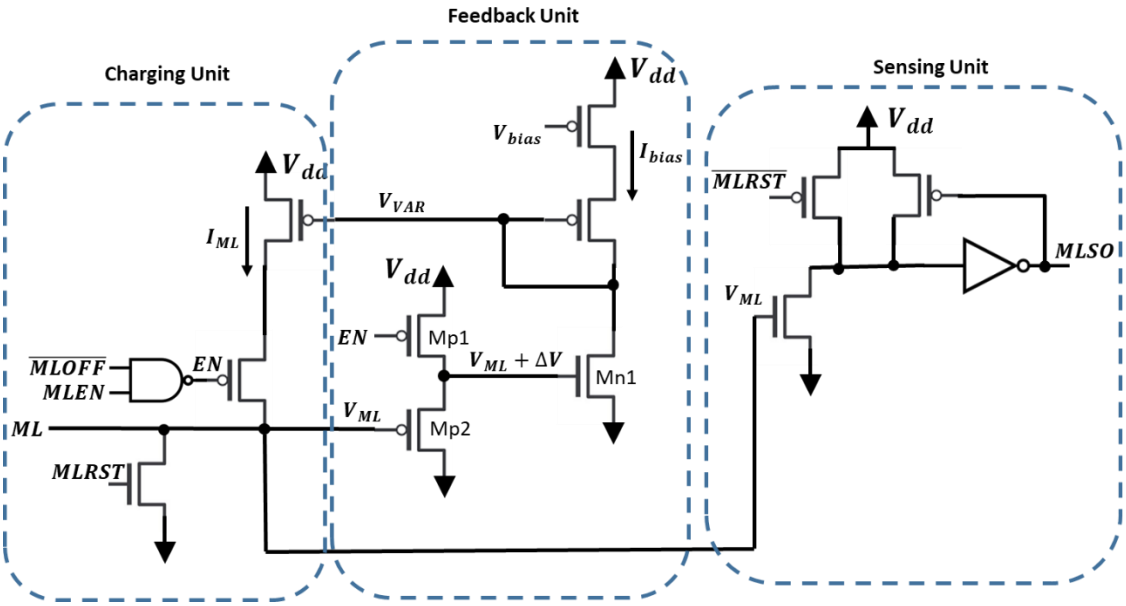



Figure 3.15: MLSA in MD power allocation technique for ML sensing [94, 95]

### 3.6.6.2 Active feedback and resistive feedback

The authors in [96] and [97] proposed two MLSAs with feedback – active feedback (AF) and resistive feedback (RF) to mitigate the limitation of MD technique. Figure 3.16 and 3.17 show the schematic diagrams of these technique. In AF technique, feedback unit is before the charging unit. In this technique, mismatched ML gets smaller current than matched ML and energy conmuption in mismatched words becomes small. $V_{bias}$ and MLSA transistor sizes need to be tuned to make this feedback mechanism effective. Dummy word provides the MLOFF signal to terminate ML charging. Some energy is wasted due to current through Mn1 (to ground) especially in all mismatched MLs. In RF technique, the feedback and charging unit is in the same block. In this technique, ML sensing is extremely simple in construction, i.e., only two additional transistors compared to CR MLSA are required. Yet, the technique is very effective not only to reduce energy consumption but also to speed up the SEARCH operation. Energy reduction occurs due to

the fact that large ML capacitances are not required to be charged to as large voltages as in CR or other feedback techniques for proper match detection. Energy overhead occurs due to the charging of node SP. Since $C_{SP}$ is very small, this energy overhead is small compared to other feedback techniques. The drawbacks of this technique are requirement of two analog control voltages ($V_{bias}$ and $V_{res}$).

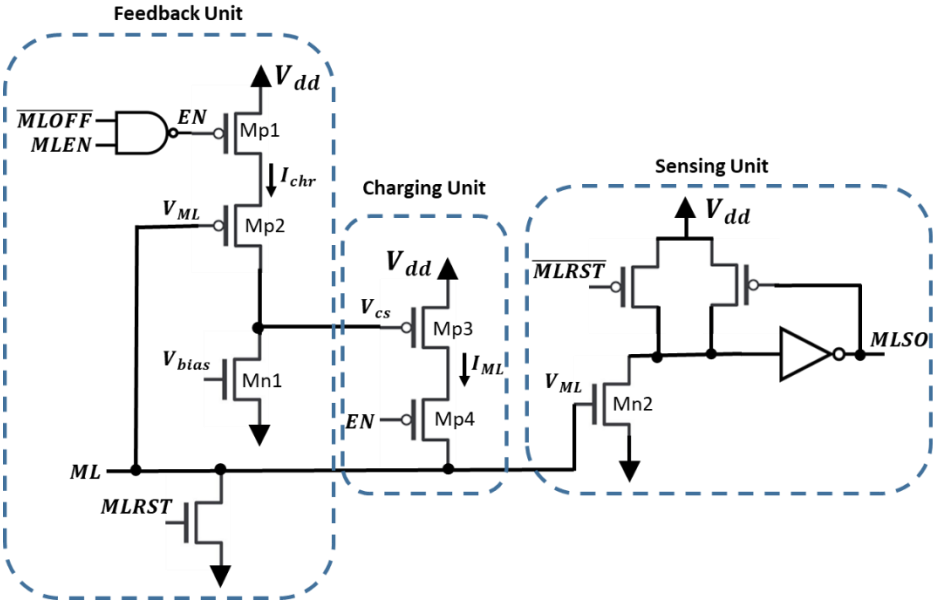



Figure 3.16: AF ML sensing scheme [96, 97]

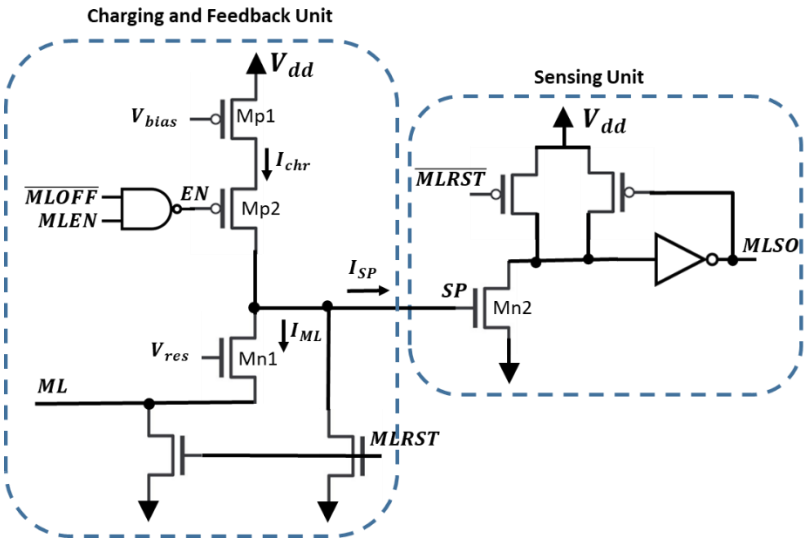



Figure 3.17: RF ML sensing scheme [96, 97]

### 3.6.6.3 Dual feedback

In [98] and [99], the authors improved the previous feedback techniques by removing the two bias voltage. The authors proposed a technique where they used positive feedback twice in a way to control both the feedback using one bias voltage. Figure 3.18 shows the dual feedback ML sensing scheme. The transistor Mn1 offers one positive feedback in a manner similar to an RF system. The feedback unit offers the second feedback. The feedback unit is a modified MD scheme created to solve the issue of static power usage. The dummy word MLSA output yields the signal DMLSO. Large differences between $I_{SN}$ currents in matched and mismatched MLs are produced by the feedback actions. When compared to other feedback techniques, match sensing is possible with very little ML voltage, which results in faster response times and lower energy usage. Process-voltage-temperature (PVT) changes affect all positive feedback schemes. Adjustable control voltages are necessary to counteract the impacts of these changes, which increases the cost. The control voltages have to be generated on-chip or have to be supplied off-chip.

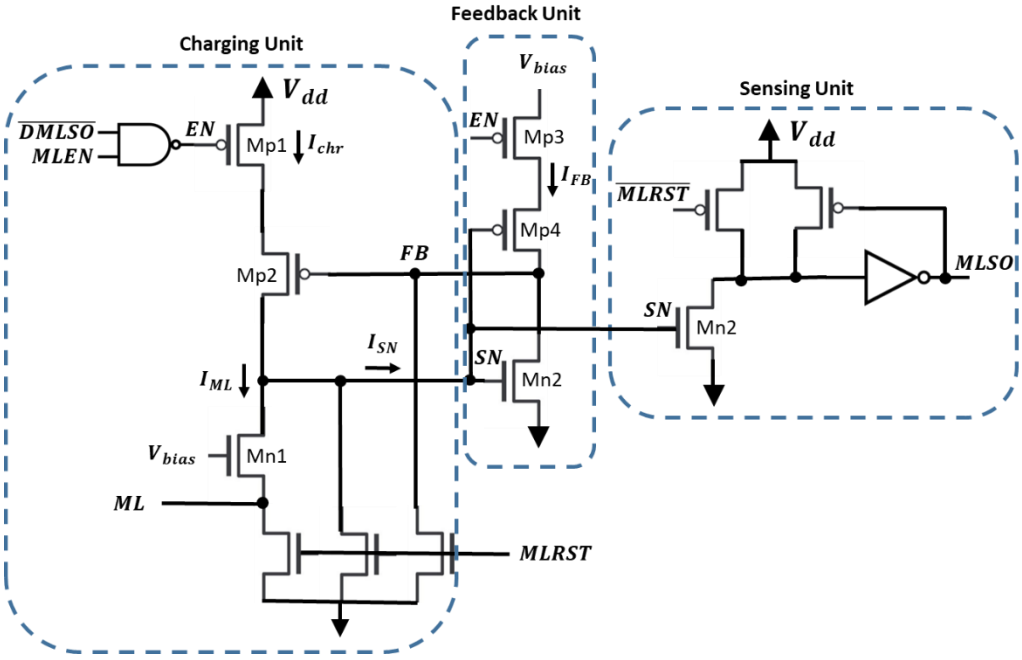



Figure 3.18: Dual feedback ML sensing scheme [98, 99]

## 3.6.7 CR-based charge-shared schemes

Figure 3.19 depicts the sensing method used in [100] for TCAM using NOR-type cells. Two ML segments are used, with the first segment being shorter than the second. There are two stages in the SEARCH process. All first segments of all words and MLs are

compared with the pertinent search key part in the first phase following MLRST's reset operation while being charged by MLEN. The ML segment 1 voltage can reach a high enough level to cause the sensing unit of MLSA1 to output high MLSO1 if the first segment of a word matches the search key section. The second ML segment is therefore charged as a result, and the pass transistor M2 also enables the second segment to share the charge stored in the matched first segment. Otherwise, the second segment remains inactive, transistor M2 remains OFF, MLSO1 remains zero, and MLSO2 remains zero. The activated second segments are compared to the remaining part of the search key during the second phase of charge. A fully matched second segment quickly charges to the detecting threshold of the sensing unit of MLSA2 thanks to the charging from the power source and charge sharing with segment 1. As a result, MLSA2 outputs logic high. A mismatched second segment discharges to ground and has a lower voltage. MLSO2 hence stays at zero. The dummy word is segmented exactly as real word. The charging durations of all the segments and the charge sharing duration between ML segments of a word are controlled by the delayed and inverted form of the MLSA outputs of the dummy word. As a result, this method combines CR, selective precharge, and charging sharing approaches. Only a little portion of the charge from the first segment is transferred to the second segment because the transistor M1 is only permitted to be ON for a short period of time. Because of this, the energy reduction achieved by this technology is not substantial. The authors proposed the use of a digitally controlled delay for the creation of MLOFF1 from DMLSO1 to improve the efficiency of charge sharing. This will make the MLSA design more difficult. The speed and energy usage of match detection in two segments are controlled by two bias voltages, $V_{bias1}$ and $V_{bias2}$.

The charge sharing scheme of [101] and [102] is a modified version of [100] where the requirement of charging in the second segment has been eliminated. The matched first segment is allowed to share its charge with the second segment until both the segment voltages become equal. The resulting low-swing ML voltage is detected by using a differential amplifier and a CR sensing unit. Absence of ML charging from the supply in the second phase causes more energy savings. The differential amplifier output node has much lower capacitance than ML segment 2. Hence, energy overhead in charging that node is small. Figure 3.20 shows the MLSA of

the scheme. If the fabrication process supports multi-threshold transistors, using lower threshold transistors at the differential amplifier input can cause even better energy performance.

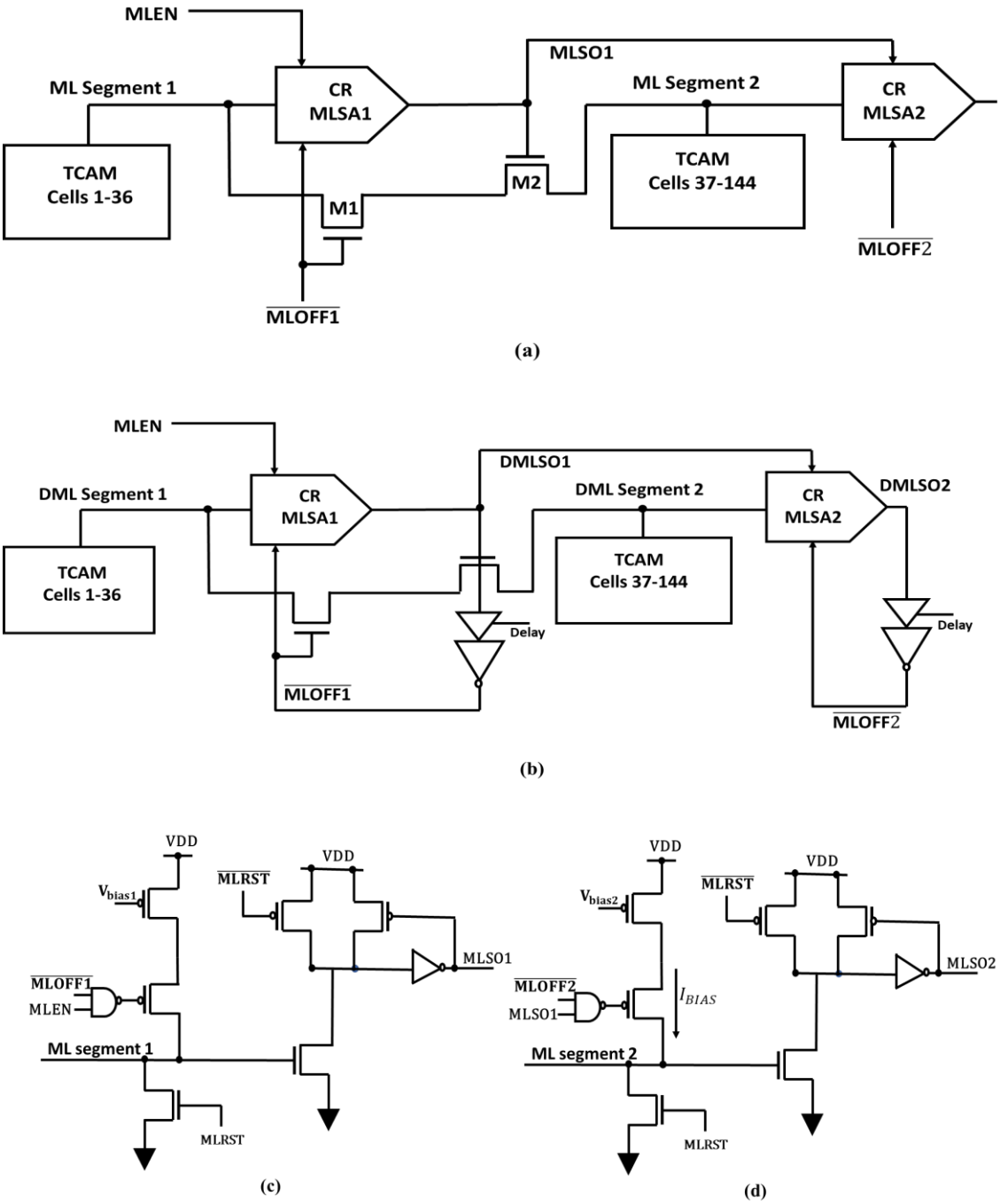



Figure 3.19: The ML sensing scheme utilizes a combination of charge sharing, selective precharge, and a dummy word: (a) one word of TCAM array, (b) dummy word with ML (DML) segments, (c) MLSA1 and (d) MLSA2 [100]

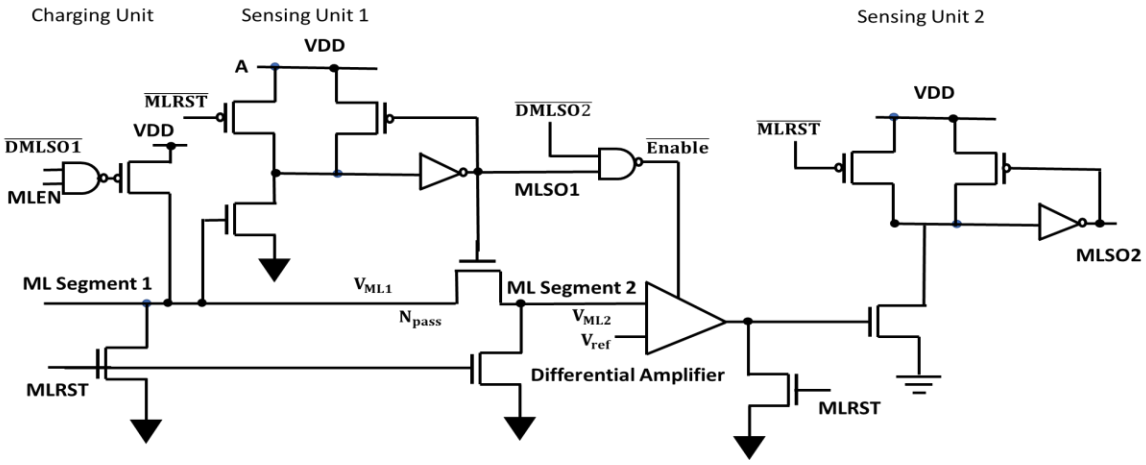



Figure 3.20: MLSA of charge-shared scheme using differential amplifier. DMLSO1 and DMLSO2 come from the dummy word [101, 102]

### 3.6.8 Summary

The CR and feedback schemes demonstrate faster operation and lower search energy compared to charge-shared schemes. Among them, the dual feedback scheme exhibits superior performance in terms of speed, energy efficiency, and peak power consumption. Following closely is the RF scheme. Although the AF scheme can achieve similar search speeds as the dual feedback scheme, its peak power consumption is notably high. The complexity of these schemes varies from low to moderate depending on the implementation of feedback mechanisms. Notably, the RF scheme stands out as the simplest, employing only a single transistor for feedback. However, schemes such as MD, AF, and dual feedback are highly sensitive to Process, Voltage, and Temperature (PVT) variations, necessitating the use of adjustable bias voltage ($V_{bias}$) for compensation. Conversely, careful design in the RF scheme can mitigate the need for such adjustments during PVT variations, despite having two adjustable voltages ($V_{bias}$ and $V_{res}$). Positive feedback results in a higher sense margin compared to the CR scheme. While charge-shared techniques may be slower, they exhibit lower sensitivity to PVT variations. The complexity of these schemes ranges from moderate to high, depending on MLSA construction or the number of ML segments. The improved charge sharing scheme outperforms others in terms of search speed, sense margin, search energy, and peak power consumption. However, the construction of MLSA becomes complex due to the presence of a differential amplifier. Taking all factors into account, this work opts for the basic CR

ML scheme for designing the MLSA due to its balanced performance across speed, energy efficiency, complexity, and sensitivity to PVT variations.

# Chapter 4

# Existing Memristor-based TCAM

## 4.1 Introduction

In the previous chapters, essential ideas and operating principles of MOSFET-based TCAM systems were presented, and well-known methods of constructing energy-efficient TCAM systems were discussed. MTCAM systems are the focus of the current chapter. Conventional MOSFET-based TCAM systems have consistently proven to be inadequate in applications where a significant quantity of data is available, as will be demonstrated in the following chapter. This is mostly because of the restricted storage density that these systems offer. TCAM systems, on the other hand, are actively being researched to attain superior storage density as well as competitive latency and power performance. These systems are based on emerging technologies of non-volatile memory (NVM). This chapter cover the literature survey of MTCAM designs. The purpose of this chapter is to conduct an assessment of existing studies and make an effort to identify any research gaps that may exist.

## 4.2 Literature Review

Several researchers are dedicated to advancing low-power, energy-efficient MTCAM technologies. A summary of the development of MTCAM is provided in Table 4.1 for reference.

In [103], the authors introduced a novel hybrid design for a MTCAM that combines MOSFETs and memristors. This MTCAM cell consists of two memristors in series and six transistors to perform the WRITE and SEARCH operations. Figure 4.1 illustrates the MTCAM cell, which utilizes distinct transistors for WRITE and SEARCH operations. Specifically, M1 and M2 are dedicated to the WRITE operation, while ML1, ML2, MR1, and MR2 serve in the SEARCH operation. The individual match lines, MLL and MLR, are distinct to display the outcome of the match operation on both MTCAM cell sides. The match or mismatch result of the MTCAM cell is produced by merging these two lines into a unified output line. The authors thoroughly examined this memory cell in terms memristance range, voltage threshold, and transistor size to optimize the processing of ternary data with speed and efficiency. They conducted a comprehensive simulation using

HSPICE at a 32nm, 45nm and 65nm CMOS technology, adopting the memristor model from reference [45], with a memristance range spanning from 100Ω to 19kΩ. It's worth noting that although the authors presented simulation results for write and search times, they did not perform array-level simulations. WRITE operation is performed with a two step process which takes more time than usual. It's also important to mention that ML is split into two parts, MLL and MLR, which introduce complexity into the SEARCH operation. The authors focused solely on designing the memory cell and did not provide any information about a sense amplifier.

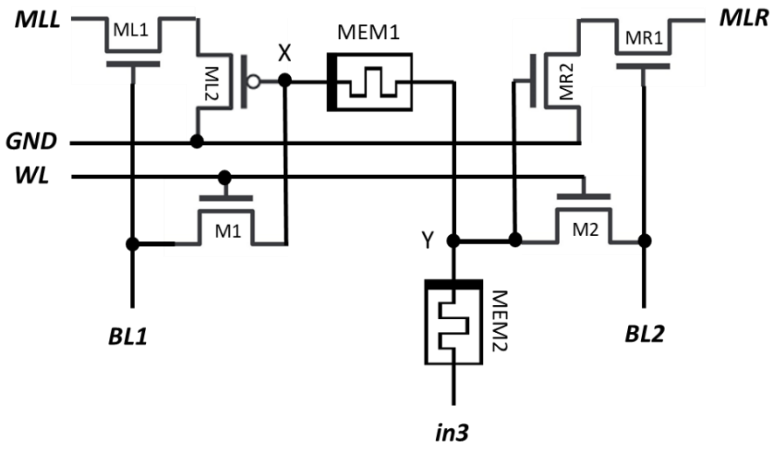



Figure 4.1: MTCAM cell proposed by [103]

In [104] the authors introduced a novel MTCAM. This MTCAM is adept at storing and searching for zero, one, and wildcard values while upholding energy and area efficiency. Each MTCAM cell consists of five transistors and two memristors, denoted as 5T2M, as depicted in Figure 4.2. These memristors can be individually programmed, creating a high impedance state between search lines (SLs) and thereby substantially reducing static current during WRITE and SEARCH operations. A novel two-step write scheme was proposed to guarantee successful cell programming, irrespective of its initial memory state. The study also addressed practical design considerations, such as voltage compliance to ensure reliable WRITE and SEARCH operations, parameter-dependent sensing margins, and device variations. The MTCAM design followed a NOR-type ML structure, as it offers high-speed operations, primarily due to the single transistor pull-down path in the worst-case scenario, as cited in reference [74]. The detailed word structure can

be observed in Figure 4.3, where all cells in a word are connected to the ML in parallel. The circuit depicted in dashed box in Figure 4.3 serves to generate signals on $SX$ and $\overline{SX}$, ensuring that, in the write mode, $\overline{SX} = \overline{SX}$, and in the search mode, $\overline{SX} = V_{dd}$. Since this circuit is required for every column, it should be incorporated into the SL driver circuitry. The schematic of the sense and latch (SAL) mechanism is presented in Figure 4.4. The authors successfully demonstrated the proper functionality of their MTCAM in both write and search modes, achieving a search delay of 2ns and a search energy consumption of 0.99fJ per digit search for a word width of 128 digits in 180nm CMOS technology. Nevertheless, while their MTCAM design proved effective, it lacked a thorough exploration of trade-offs between speed, energy consumption, storage density, and hardware complexity. Notably, they conducted their simulations using older technology node. Furthermore, the use of the same input lines for both WRITE and SEARCH operations raises concerns about data overwriting during searches, and their adoption of a two-step write operation added complexity to the WRITE operation.

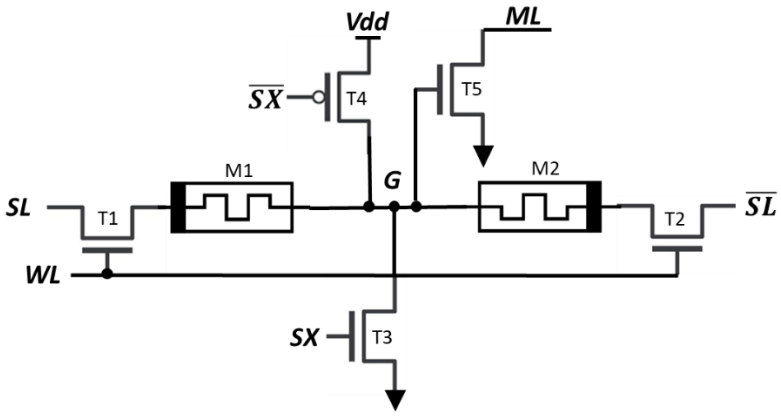



Figure 4.2: Schematics of the MTCAM cell of [104]

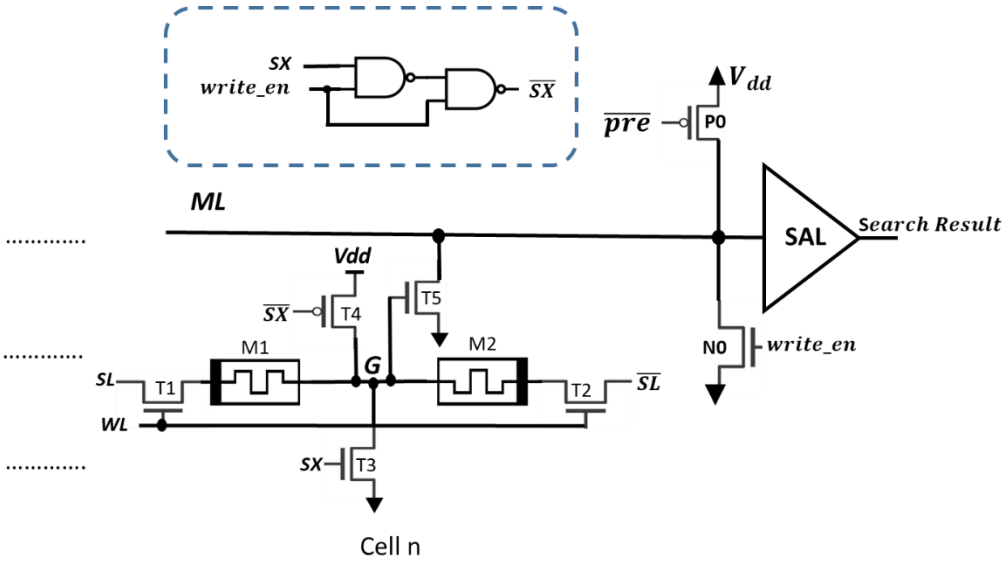



Figure 4.3: Detail word structure where all the cells of a word are connected to ML in parallel [104]

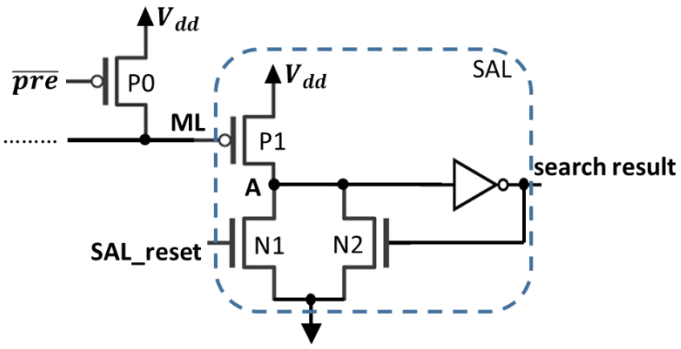



Figure 4.4: Schematic of SAL [104]

In [105], the authors introduced a novel hybrid 2T2M MCAM cell design, illustrated in Figure 4.5. They capitalized on the inherently parallel nature of the MCAM search operation to mitigate power consumption. This design was adaptable for both full and partial match applications. In the partial match design concept, each cell generates a 1-bit Hamming distance between the search bit string and the stored bit string. These individual Hamming distances are then aggregated across the entire word line and compared with results from other word lines to determine the closest match to the search input among the stored words. To enhance sense margin in the partial match design, the authors incorporated a current mirror structure to maintain a constant match current. The entire design boasts a reduced number of transistors and an efficient layout compared to previous approaches. Validation of their design's efficacy was conducted through Cadence Spectre using BPTM 45nm technology. The authors simulated their design in an 8×8 array

size, which is relatively small compared to other existing designs, yielding a power consumption of 24.85μW, a search delay of 0.041ns, and a power delay product of 1.0189fWs. However, the proposed design utilized the same input lines for both WRITE and SEARCH operations, resulting in data overwrite issues during search, and lacked a ternary state.

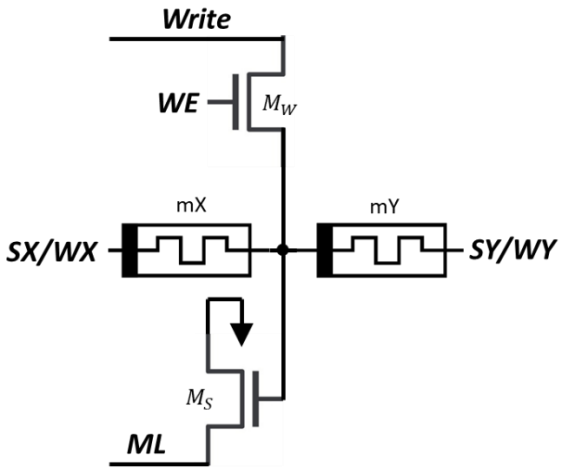



Figure 4.5: Structure of the full match cell block [105]

In [106], the authors introduced a condensed hybrid design of MTCAM accompanied by an innovative and streamlined approach for programming memristors within CAM. Not only does this novel structure streamline the processes of writing and searching, but it also results in a substantial reduction in the required layout area. The proposed MTCAM had five transistors and two memrostors which is shown Figure 4.6. They mainly compared their design with [104] and claimed to have reduced control lines, a one-step writing phase and reduced layout area by more than 27%. Furthermore, simulation was carried out in a 2×4 structure in order to demonstrate and verify the cell function. For performance evaluation, this array size is too small to evaluate the search time, search energy and other parameters. The authors used same input lines for their WRITE and SEARCH operation. They also used different voltage levels for WRITE and SEARCH operations.

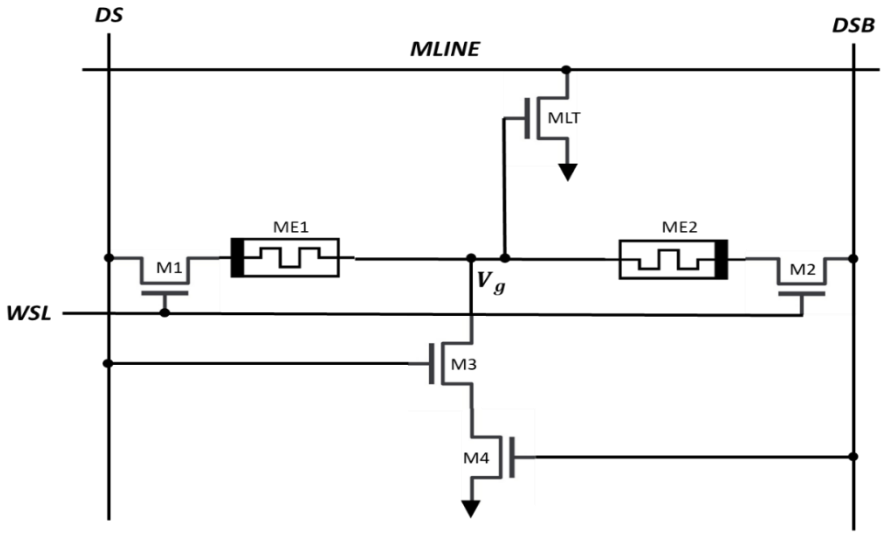



Figure 4.6: Compact 5T2M mTCAM [106]

The main goal outlined in reference [107] was to create a new, exceptionally fast MTCAM while keeping its power consumption at a minimal level. To achieve this, the author introduced an innovative MTCAM cell that utilizes a memristor as a bit storage component, combined with an ultra-fast match line sense amplifier. This novel MTCAM cell, as depicted in Figure 4.7, consisted of nine transistors and two memristors. Using 45nm technology node and a supply voltage of 1V, the search delay for the proposed 144-bit MTCAM was measured at 175ps, with a per-bit search energy of 1.2fJ and a bit-search error rate (BSER) of 1.7%. Compared to the fastest existing MTCAM design, this novel MTCAM was 1.12 times faster and consumed 67% less power. It's essential to note that the search time in a TCAM is contingent on the rate at which the match line discharges and the delay associated with the match line sense amplifier (MLSA) in the event of a single-bit miss. Consequently, the pursuit of ultrafast TCAM hinges on having an equally rapid MLSA. The paper's second significant contribution was the development of a swift MLSA design using conventional CMOS technology, illustrated in Figure 4.8. Notably, the proposed MLSA attained a 70ps delay for a sense margin of 100mV, operating at a supply voltage of 1.2V. The memristor lengths were set at 5nm, and the simulations utilized the VTEAM memristor model for the $TiO_2$ bipolar metal-oxide memristor, a model whose accuracy had been experimentally validated [70]. The memristor parameters $R_{ON}$ and $R_{OFF}$ were established at 100KΩ and 10MΩ, respectively. However, it's worth mentioning that

the proposed MTCAM cell, designed with 9T2M, exhibited a relatively larger cell area compared to other MTCAMs, resulting in higher layout complexity.

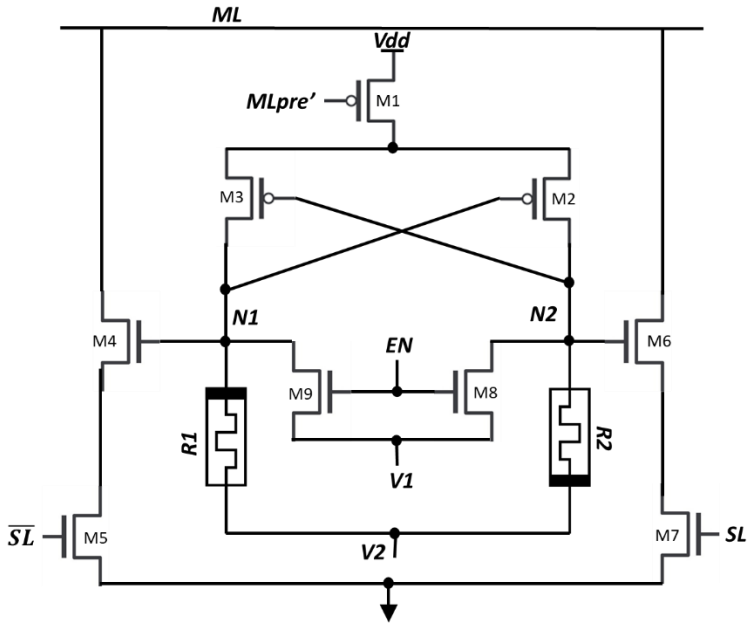



Figure 4.7: The Proposed TCAM Cell [107]

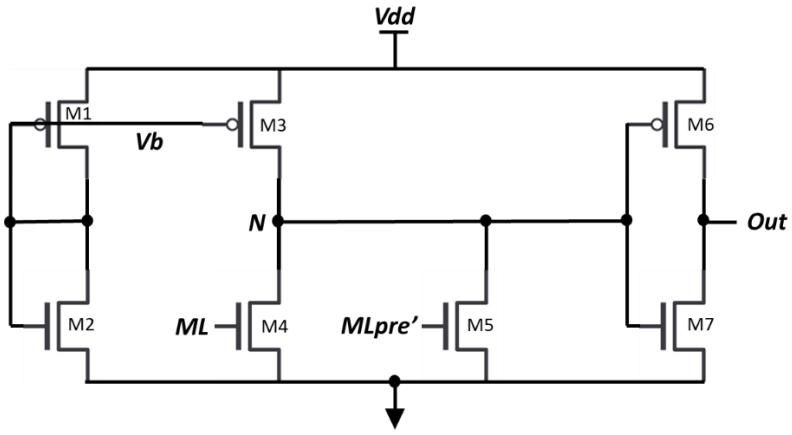



Figure 4.8: The proposed Match Line Sense Amplifier [107]

In [108] the authors developed a TCAM cell where they used two transistors and two memristors for their design. The MTCAM is shown in Figure 4.9. In their TCAM cell, the memristor pair is placed in anti-serial position (connected in series but opposite in polarity). They also proposed simple writing and searching operation by using same input lines. The authors claimed their design to be area efficient because of reduction in the number of transistors and wiring. Again, the proposed MTCAM cell were used to form

128×128 memory arrays. For their SPICE simulation, they used 65nm TSMC high-threshold MOS model parameters and the mathematical model of Biolek et. al [55]. For the memristor model the $R_{on}$ = 2KΩ and $R_{off}$ = 200KΩ with threshold voltage $V_{th}$ = 1V was used. 1V was used as supply voltage, 3.3V was used as write voltage, and 0.7V was used for search voltage. The simulation results of 128×128 MTCAM array required 22.174ns to write logic-1, 29.15ns to write logic-0, and 11.11ns to write logic-X. The search delay is calculated to be 0.75ns and search energy 0.866fJ/bit/search. The cell layout gives an area estimation of 6.11μm$^2$. The robustness of the design was verified with fast and slow corner simulations. Parasitic RC components were analyzed using Cadence Virtuoso layout-XL and Quantus QRC extraction tools. Simulation results illustrate the fast search speed and low power consumption of the design. The authors used same input lines for WRITE and SEARCH operation which creates data overwrite problem. Two different voltage levels for WRITE and SEARCH operations are needed which is difficult to attain.

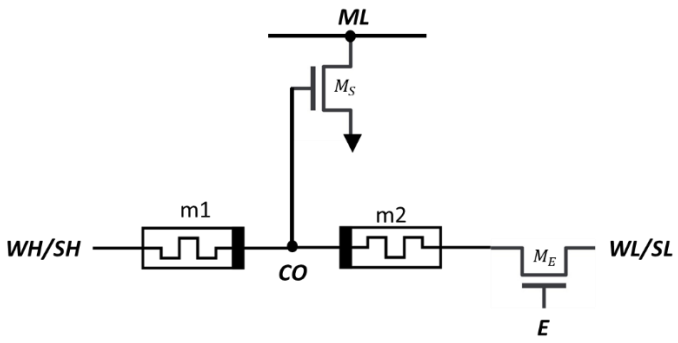



Figure 4.9: Schematic of MTCAM cell of [108]

Table 4.1: Summary of developing MTCAM cells in different years are enlisted

| **Parameters** | **[103]** | **[104]** | **[105]** | **[106]** | **[107]** | **[108]** |
|---|---|---|---|---|---|---|
| Memristor Model | HP Model | Own model | Own model | Biolek | VTEAM | Biolek |
| Word Size | Not mentioned | 128 | 8 | 4 | 144 | 128 |
| Cell Structure | 6T2M | 5T2M | 2T2M | 5T2M | 9T2M | 2T2M |
| Search Delay (ns) | 6.08 | 2.0 | 0.041 | 2.1 | 0.175 | 0.75 |
| Search Energy(fJ/bit/ search) | not calculated | 0.99 | 1.012 | 0.81 | 1.2 | 0.866 |
| Supply Voltage (V) | 1.0 | 1.5 | 1.0 | 1.0 | 1.0 | 1.0 |
| Technology | 32nm | 180nm | 45nm | 180nm | 45nm | 65nm |
| Memristance range | 100Ω - 19kΩ | 10kΩ - 1MΩ | 100Ω - 16kΩ | 1kΩ - 100kΩ | 100kΩ - 10MΩ | 2kΩ - 200kΩ |
| Write operation | single step | two step | two step | one step | one step | one step |
| WRITE and SEARCH Voltage Magnitude | Not mentioned clearly | different | different | different | same | different |
| ML sensing scheme | Not mentioned clearly | precharge-high | Not mentioned clearly | precharge-high | Own created | Charge sharing |

## 4.3 Summary

The existing designs proposed different cell structure of MTCAM to reduce the search energy of the cell. In some cases, the authors are successful but the cell area is high. Different technology nodes have been used for the simulation which varies from 32nm to 180nm. Almost all the papers used different voltages for their WRITE and SEARCH operation which is difficult to attain. The authors used different memristor models and ML sensing schemes for their MTCAM array simulation. As almost all the authors used the same input line for their write and search data, no clear explanation had been given by the authors about the data overwrite issue. However, it is clear from the above literatures that a high-speed, low-power, area-efficient and data-restoring capable (which can protect the stored data from being overwritten) MTCAM can give solution to any large-scale parallel data searching applications. Though, the researchers claimed to achieve high-speed and low-power but failed to achieve area-efficient and/or data-restoring capable design. This work aims to resolve this issue and to develop a high-speed, low-power, area-efficient and data-restoring capable MTCAM operated with same write and search voltage.

# Chapter 5

# Proposed Memristor-based TCAM

## 5.1 Introduction

In this chapter, a novel hybrid MTCAM cell design has been introduced, featuring five transistors and four memristors. A detailed explanation of the cell's functionality for both WRITE and SEARCH operations has been provided. Additionally, an encoding table outlining three distinct states using two bits and memristance status has been presented. The proposal also encompasses a comprehensive array architecture. Furthermore, ML sensing scheme employed in this research endeavor has been described.

## 5.2 Proposed Cell Structure

The proposed MTCAM cell comprises two units: the main unit and the data recall unit. Each unit serves distinct purposes in WRITE and SEARCH operations, respectively, utilizing the same input lines for both functions. This shared input arrangement poses the risk of potential data overwriting during SEARCH operations. To mitigate this concern, the proposed MTCAM cell integrates a dedicated data recall unit capable of preserving current data during WRITE operations. The main unit consists of two memristors, ME1 and ME2, along with three NMOS transistors: Mn1, Mn2, and Mn3, as depicted in Figure 5.1. ME1 and ME2 are serially connected memristors with opposing polarities. Mn1 and Mn2 serve as access transistors, linking input lines DS1 and DS2 to ME1 and ME2, respectively. Mn3 is linked to ML at its drain terminal, while its gate terminal connects to node G. The data recall unit comprises two transistors (Mn4 and Mn5) and two memristors (ME3 and ME4). Mn4 and Mn5 function primarily as access transistors for this unit. ME3 and ME4 are interconnected in series with opposite polarities. The digit stored in the main unit is mirrored in the data recall unit, ensuring data retrieval at any instance. Utilizing the resistance characteristics of memristors, data is written into the cell [21].

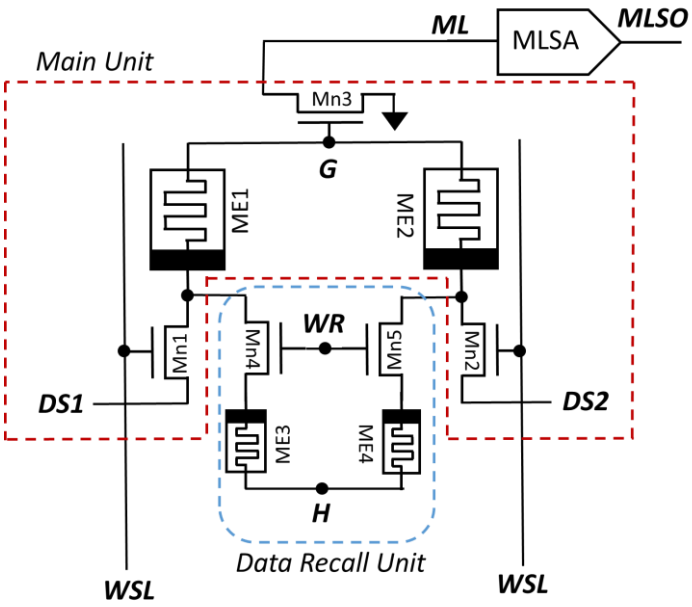



Figure 5.1: The proposed structure of the 5T4M MTCAM cell consists of two units: the main unit and the data recall unit

## 5.3 Encoding Table Description

As the design pertains to MTCAM, every cell is required to handle three distinct states: high, low, and mask (also referred to as 'Don't Care'). To encode these three states, a pair of bits, namely DS1 and DS2, are employed for writing and reading. Table 5.1 illustrates how these two bits represent the three states. According to the table DS1 and DS2 should be 0 and 1 when writing or searching logic-0 (low) in the memory. To write or search logic-1 (high) in the memory, DS1 and DS2 should be given 1 and 0, respectively. For the logic-X (don't care), DS1 and DS2 should both be given 0. DS1DS2 = 11 state is not allowed.

Table 5.1: Representation of three states using two bits with memristance status

| State | Stored/Search Bits | | Memristance Status | |
|---|---|---|---|---|
| | DS1 | DS2 | ME1 | ME2 |
| Logic-0 (Low) | 0 | 1 | LRS | HRS |
| Logic-1 (High) | 1 | 0 | HRS | LRS |
| Logic-X (Don’t Care) | 0 | 0 | LRS | LRS |
| Not Allowed | 1 | 1 | - | - |

Within TCAM, it is possible to enhance search flexibility by enabling partial searches. Rather than examining the entire data line, it becomes feasible to search only a specific segment of the line. This selective search operation is achieved through the use of masking. In the context of TCAM design, local masking and global masking refer to the techniques used to perform more complex matching operations and increase the flexibility of matching criteria within the TCAM. Local masking involves applying masks to specific portions of the data being searched in the TCAM. It allows for more granular control over which bits in the search key are significant for the matching process. With local masking, different parts of the search key can have different mask values applied, enabling the matching engine to ignore certain bits or treat them as "don't care" bits during the comparison process. Global masking, on the other hand, applies a single mask to the entire search key or across a broader range of bits in the search data. It is applied uniformly across all entries or rules in the TCAM, allowing for a broad modification of the matching behavior. Global masking is useful when you want to modify the behavior of the TCAM's matching for all entries simultaneously. For instance, it could be employed to mask certain fields or bits across multiple entries in a routing table. These masking techniques offer flexibility in configuring the TCAM's matching behavior, allowing more sophisticated matching operations and accommodating different types of search criteria. Local masking provides fine-grained control over specific bits, whereas global masking allows for uniform modification across multiple entries. The conditions for masking are detailed in Table 5.2.

Table 5.2: Masking Conditions

| Masking | Condition | Comment |
|---|---|---|
| Local | DS1 DS2 = 0 0 | Search Word |
| Global | DS1 DS2 = 0 0 | Dummy Word |

## 5.4 Array Architecture

Figure 5.2 provides an overview of the structural layout of an MTCAM array, featuring a 32-word×144-digit configuration. Each word in the array is equipped with a ML. The Match Line Sense Amplifier (MLSA) generates high or low outputs based on the

ML voltage, indicating whether there's a match or mismatch between the search data and the stored data.

During the WRITE operation, input lines supply data for storage in the memory. The WSL and WR signals are set high to enable the storage of specific data. DS1 and DS2, representing two input lines, provide data for the respective logic during this operation.

In the SEARCH operation, the same input lines are utilized, with only the WSL signal being activated. If there's a match between the stored data in a word and the search data, the corresponding ML becomes high, resulting in a high output from MLSO. Conversely, if there's a mismatch between the stored data and search data, both ML and MLSO remain low.

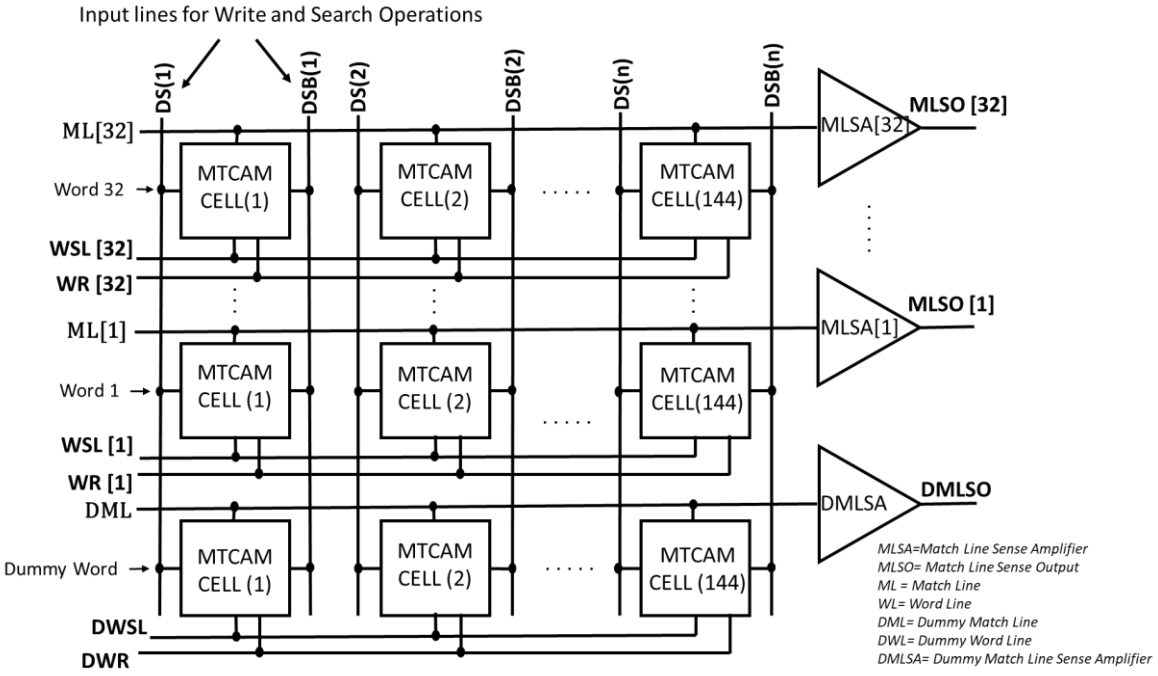



Figure 5.2: Structure of a 32-word ×144-digit TCAM Array

## 5.5 ML Structure

In this research work, a CR ML sensing scheme [84] has been deployed. In contrast to the conventional method of charging all MLs to high, this scheme pre-discharges all MLs to low. Within each word, all cells are interconnected to a single ML using NOR logic. The CR scheme is depicted in Figure 5.3, comprising two illustrations: one representing a single word and the other portraying a dummy word. To regulate the timing

of the clocked circuit, a dummy word is integrated. The dummy word consistently registers as matched due to local masking, effectively governing the circuit's timing. By leveraging this dummy word concept, the CR scheme mitigates excessive ML charging, thereby curbing power consumption and preventing unnecessary ML charging [94, 109].

Each word comprises two distinct units: the charging unit and the sensing unit. The charging unit consists of two PMOS transistors (Mp1 and Mp2) and a NAND gate. The sensing unit incorporates two PMOS transistors (Mp3 and Mp4), one NMOS transistor (Mn2), and an inverter. Additionally, a separate NMOS transistor (Mn1) is employed to reset the ML prior to commencing the SEARCH operation. The ultimate match or mismatch outcome is reflected in MLSO. The operation commences with a reset of any voltage present on the ML ($V_{ML}$) and MLSA outputs (MLSOs and DMLSO) to zero via the MLRST signal. Subsequently, the activation of the MLEN signal causes transistor MP2 to switch on, enabling current ($I_{ML}$) to flow. The ML capacitance ($C_{ML}$) begins to charge. In instances where a complete word match occurs, the ML can charge up to the threshold voltage of Mn2, prompting it to switch on. Consequently, MLSO can become high. Conversely, in the absence of a match, $V_{ML}$ remains low as the ML has discharge paths to the ground. Mn2 remains in the off state, and MLSO remains at zero. The dummy word always matches due to local masking, resulting in high DMLSO. A delayed and inverted version of DMLSO, known as MLOFF, is utilized to activate Mp2 transistors in all words. This action prevents unnecessary charging of MLs, reducing energy consumption. The delay following DMLSO ensures that all matched MLs have adequate time to charge up to the threshold voltage of Mn2 if the dummy word detects a match earlier, possibly due to process variations. The speed and energy consumption of the match detection process are regulated by $V_{bias}$, which controls $I_{ML}$.

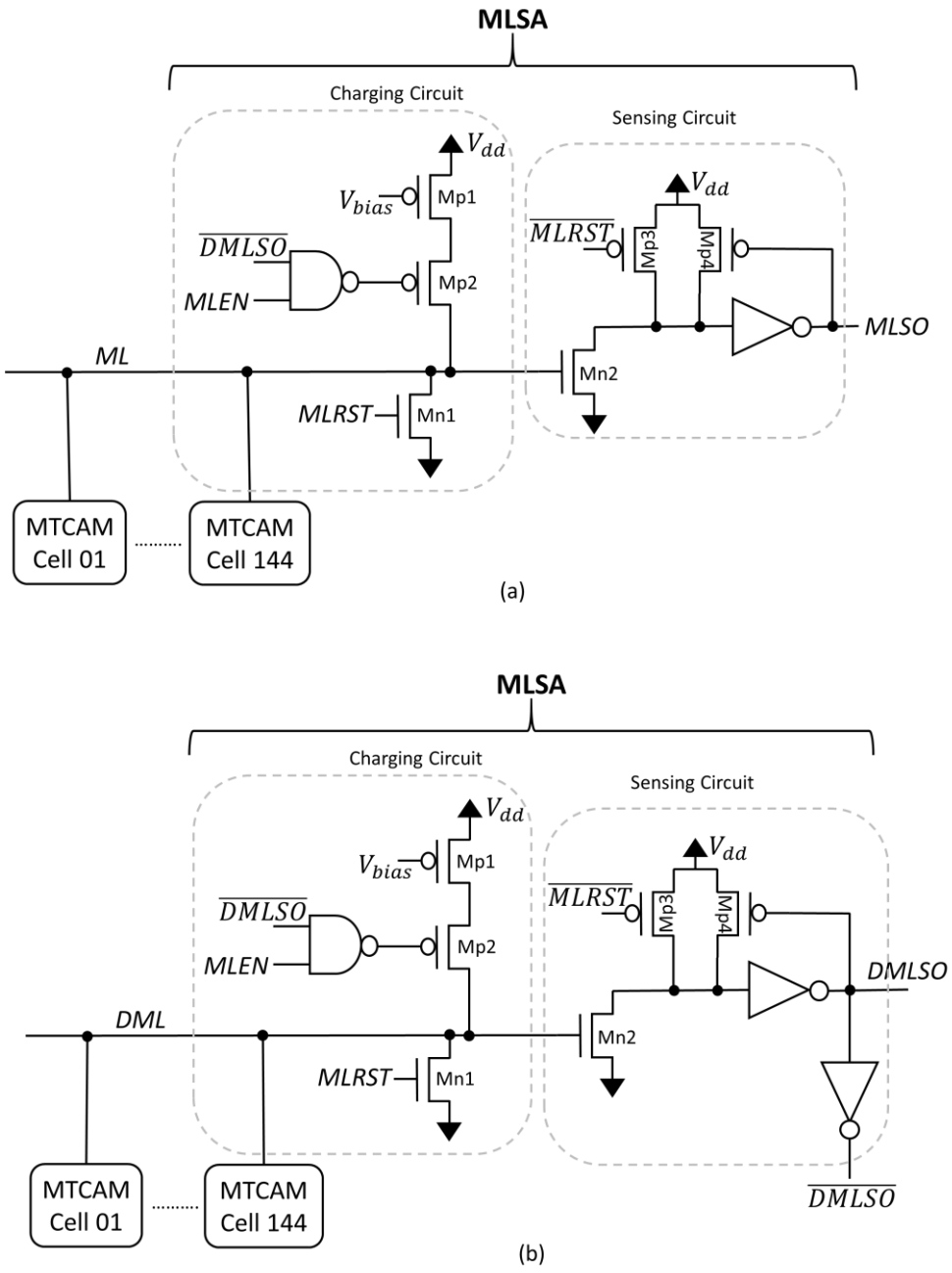



Figure 5.3: The precharge-low ML sensing scheme is illustrated in two diagrams: (a) representing one word, and (b) depicting a dummy word [84]

## 5.6 Write Mode

The reciprocal interaction between memristors markedly mitigates the non-linearity of memristance, accomplished by linking memristors in series with opposing polarities [110]. Figure 5.4 demonstrates the behavior of two memristors when connected in series with opposite polarity. Upon applying a positive voltage (+Ve) to the undoped section of ME1 (reversed-bias condition), the width of the doped region (W) diminishes, thereby

increasing the total memristance of ME1. Conversely, when a negative voltage (-Ve) is applied to the undoped section of ME2 (forward-bias condition), the width of the doped region (W) expands, leading to a reduction in the total memristance of ME2.

To initiate the WRITE operation, both the WSL and WR signals must be set high to activate the access transistors: Mn1 and Mn2 for the main unit and Mn3 and Mn4 for the data recall unit (as depicted in Figure 5.1). Table 5.3 outlines the memristance status, while Figure 5.5 illustrates various state values of three distinct logics: logic-0, logic-1, and logic-X, along with their respective current directions. When writing logic-0 (low) into memory, DS1 and DS2 (connected to the main unit) should be set to 0 and 1, respectively, as specified in Table 5.1. Here, ME1 is in a forward-biased condition, indicating the memristor is in a LRS ($R_{ON}$). Conversely, ME2 is in a reversed-bias condition, representing the memristor in a HRS ($R_{OFF}$). This holds true for ME3 and ME4 as well, with ME3 in LRS and ME4 in HRS.

For writing logic-1 into memory, DS1 and DS2 must be supplied with the values 1 and 0, respectively. Consequently, ME1 is in a reversed-bias condition, indicating the memristor is in HRS. Conversely, ME2 is in a forward-biased condition, indicating the memristor is in LRS. Similarly, ME3 and ME4 are in HRS and LRS, respectively. The data recall unit behaves analogously to the main unit for all logics.

To write logic-X into memory, DS1 and DS2 should be set to 0. In this scenario, both ME1 and ME2 are in a forward-biased condition, indicating both memristors are in LRS.

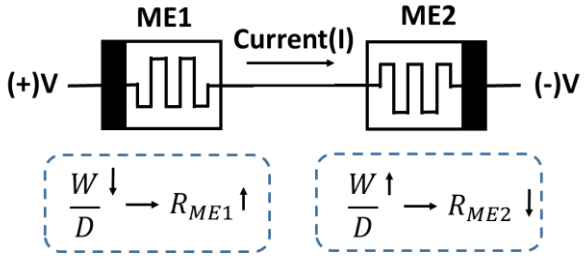



Figure 5.4: Performance of two memristors when they are connected in series.

Table 5.3: Memristance status of all three logics.

| State | Memristance Status | | | |
|---|---|---|---|---|
| | **ME1** | **ME2** | **ME3** | **ME4** |
| Logic-0 | $R_{ON}$ | $R_{OFF}$ | $R_{ON}$ | $R_{OFF}$ |
| Logic-1 | $R_{OFF}$ | $R_{ON}$ | $R_{OFF}$ | $R_{ON}$ |
| Logic-X | $R_{ON}$ | $R_{ON}$ | $R_{ON}$ | $R_{ON}$ |

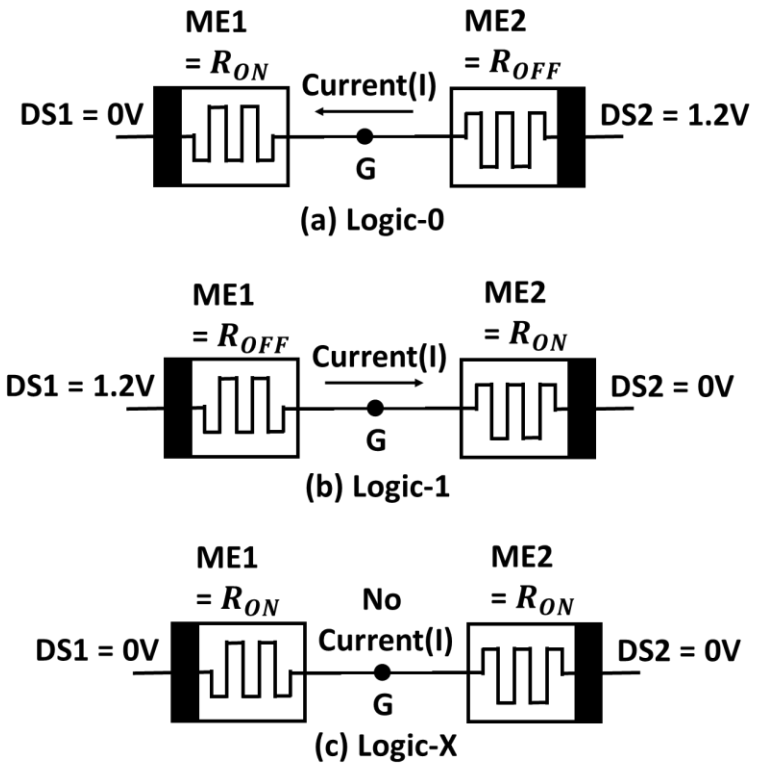



Figure 5.5: Writing conditions of three different logics: (a) Logic-0, (b) logic-1, and (c) logic-X

## 5.7 Search Mode

The same input lines DS1 and DS2 contain the search bits. The search process relies on pattern matching between the stored data and search data, leading to the classification of the search result as either a Match or Mismatch. The conditions for both Match and Mismatch are detailed in Table 5.4.

Table 5.4: Match and mismatch conditions during SEARCH operation

| Condition | Decision | Match-line |
|---|---|---|
| Stored data = Search data | Match | Charge |
| Stored data ≠ Search data | Mismatch | Discharge |

Before starting the SEARCH operation, WR needs to high to restore the data from the data recall unit. Since the CR method is employed as the ML sensing scheme, all MLs undergo pre-discharging to a low state initially. As the match evaluation process commences, all MLs are charged towards a high state. Given the presence of discharging paths, the ML voltage must remain low in the event of a mismatch within a word [111]. During the search for a logic-0 (low) digit, DS1 and DS2 are set to 0 and 1, respectively. At this stage, the access transistors Mn1 and Mn2 are activated, with ME1 and ME2 functioning as $R_{ON}$ and $R_{OFF}$, respectively. The decision-making node, G, determines the activation state of the Mn3 transistor. If the stored digit matches the search digit (both are 0), a match is detected. At this point, the voltage of G ($V_G$) is determined through a voltage divider, yielding a low value below the threshold voltage of Mn3. Consequently, the ML disconnects from ground, charges to a high state, and activates the MN2 transistor, resulting in a high output at MLSO. These conditions are outlined in equations (40) and (41).

$$V_G = V_{search} \cdot \frac{R_{ON}}{(R_{ON} + R_{OFF})} \tag{40}$$

$$V_G < V_{th,Mn3} \tag{41}$$

Here, $V_{th,Mn3}$ is the threshold voltage of the Mn3 transistor. $V_{search}$ is the positive voltage applied at DS1 or DS2. The value of $V_{search}$ must be selected in the range given in equation (42).

$$\begin{cases} V_{th,Mn3} < V_{search} < 3V_{th,Mn3} \\ V_{th,Mn3} > 0 \end{cases} \tag{42}$$

When the stored digit is 0 and the search digit is 1, a mismatch occurs in the result. At this juncture, $V_G$ surpasses the threshold voltage $V_{th,Mn3}$, activating the Mn3 transistor. Consequently, the ML discharges through this Mn3 transistor. As a consequence, MN2 is

deactivated, leading to a low output at MLSO. Once more, these conditions are delineated in equations (43) and (44).

$$V_G = V_{search} \cdot \frac{R_{OFF}}{(R_{ON} + R_{OFF})} \tag{43}$$

$$V_G > V_{th,Mn3} \tag{44}$$

The described operations and equations remain applicable for both match and mismatch searches when a logic-1 (high) digit is stored. However, in cases where the search data is a 'don't care' ('X'), both DS1 and DS2 are set to 0. Consequently, the result is always matched, and MLSO indicates a high output. Equation (45) delineates the resistor divider, while equation (46) specifies that $V_G$ must be sufficiently low to deactivate the Mn3 transistor [104].

$$V_G = V_{search} \cdot \frac{R_{ON}}{(R_{ON} + R_{ON})} \tag{45}$$

$$V_G < V_{th,Mn3} \tag{46}$$

The depicted Figure 5.6 illustrates an example search operation conducted using a 2×4 array. The first word within this context contains stored digits '1001,' while the second word contains 'X010.' The search digit employed is '101X.' As a confirmation of the SEARCH operation results in a ‘match’ for the second word. Furthermore, ML will charge and MLSO2 will give high in the output.

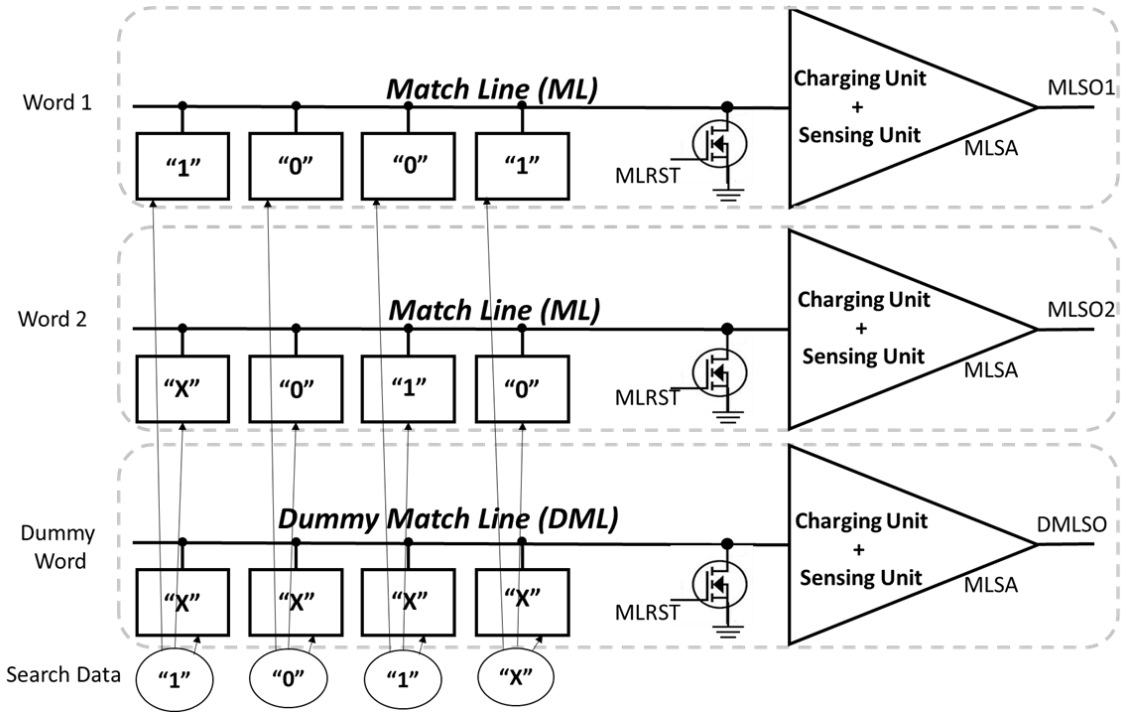



Figure 5.6: An example of 2×4 MTCAM array using the proposed MTCAM cell

## 5.8 Summary

The proposed MTCAM cell is compact in size as it uses only five transistors and four memristors. The working principle of this compact cell has been discussed in this chapter with masking conditions. The WRITE and SEARCH operations have been described in details. The ML scheme and array structure are also being discussed.

# Chapter 6

# Simulation Results and Comparison

## 6.1 Introduction

This chapter showcases the simulation outcomes for both WRITE and SEARCH operations conducted on a 32×144 MTCAM array. The results are derived from simulations performed in HSpice. Transistors are modeled using the BSIM 32nm PTM, while the memristor model is set the modified Biolek model [55]. The memristor boundaries $R_{ON}$ and $R_{OFF}$ are established at 1kΩ and 200kΩ, respectively [104, 108]. Search time and power dissipation are evaluated under a supply voltage of 1.2V. The Table 6.1 delineates the nominal length and width values of the transistor channels within the proposed MTCAM cell.

Table 6.1: Transistor size of the proposed MTCAM cell of Figure 5.1

| Word Size | Mn1 (nm/nm) | Mn2 (nm/nm) | Mn3 (nm/nm) | Mn4 (nm/nm) | Mn5 (nm/nm) |
|---|---|---|---|---|---|
| 144-digit | 704/32 | 704/32 | 128/32 | 40/32 | 40/32 |

## 6.2 Simulation of Write Operation

Figure 6.1 depicts the write operation of the proposed MTCAM cell, with WSL and WR set to high values as described in Section 5.4. The simulation has yielded three distinct memristance values: a low value of 1.2kΩ, a medium value of 48kΩ, and a high value of 184kΩ. In the logic-X (don't care) state, characterized by DS1 = 0 and DS2 = 0, the voltage value of $V_G$ is significantly diminished. The memristors exhibit LRS. In the logic-1 state, where DS1 is set to 1 and DS2 is set to 0, the voltage at $V_G$ is determined by the voltage divider formed by ME1 and ME2. In the first write cycle (DS1 = 0, DS2 = 0) ME1 exhibits LRS with a value of 1.2kΩ, while ME2 also is in LRS with a same value of 1.2kΩ. However, the scenario undergoes a transformation when logic-1 (where DS1 = 1 and DS2 = 0) is written. Now, ME1 has a high resistance (184kΩ), but the ME2 has a medium resistance (48kΩ). During WRITE operation of logic-0 (DS1 = 0, DS2 = 1) ME1 has 48kΩ and ME2 has 184kΩ. The finite switching time of the memristor is considered by allocating

a duration of 10ns to each write cycle. The energy value is measured to be 0.35pJ for 10 combination.

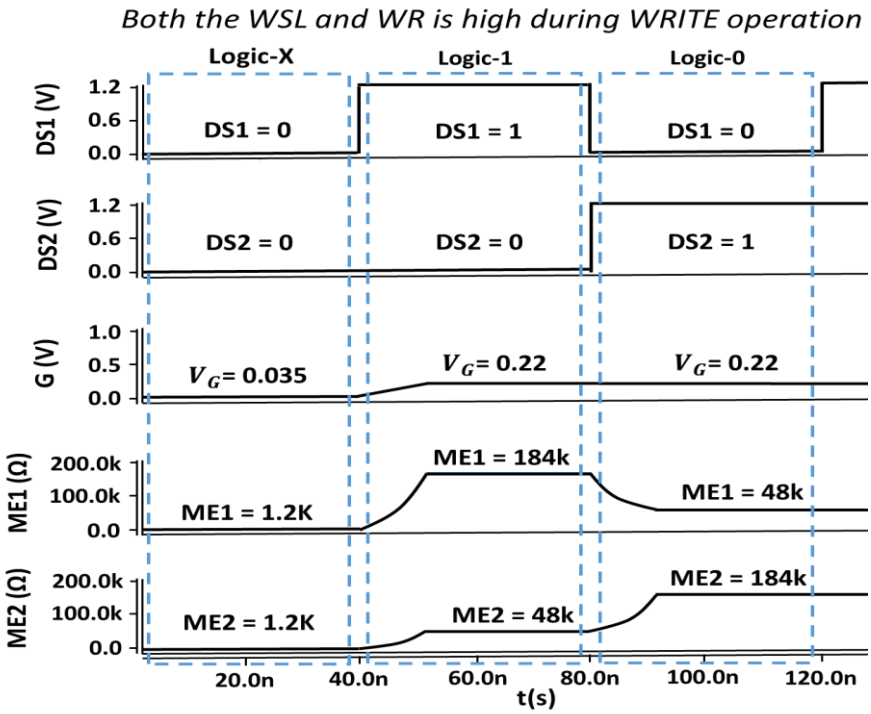



Figure 6.1: The simulation outcomes depict the write mode operation of the proposed MTCAM, employing the modified Biolek model [55] for memristors. The values are $R_{ON}$=1k, $R_{OFF}$=200k, $R_{int}$=10k, D=10n, p=1

## 6.3 Simulation of Search Operation

The search operation enables data retrieval and comparison. Figure 6.2 illustrates the sequence of search operations utilizing the proposed MTCAM cell. Five SEARCH operations are conducted sequentially and search results are verified. Following each search operation, the system resets the values to prepare for the subsequent search cycle.

The process unfolds over a precise timeline: At 0.5ns, the WRITE operation commences by storing a logic-1 in the memory. During this step, ME1 is in the HRS (184kΩ) while ME2 is in the LRS (48kΩ). Simultaneously, both WSL and WR signals are high. As time progresses to 1.3ns, a reset signal is applied, followed by the initiation of the first search at 2ns. In this initial search, a logic-0 is given. Consequently, the states of the memristors alter, with ME1 transitioning to the LRS and ME2 to the HRS. This change

causes the ML to discharge to ground, and as a result, the search output MLSO is low, indicating a mismatch between the stored data and the search data.

At 3ns, the data is restored through the data recall unit and at this time, only WR = 1. The memristors state will be the same as the stored data state. The second, third and fourth searches occur at 4ns, 5.7ns and 7.5ns, respectively, with search digits being logic-0, logic-x and logic-0. The second SEARCH operation mimicks the behavior of the initial SEARCH operation, leading to similar outcomes. After the search, ML is discharged to ground, and MLSO remains low, signifying that the result is mismatched. The third SEARCH operation gives don’t care logic which produces a match result with the stored result. This means ML is continuing its charging and MLSO goes high. Again in fourth search, the MLSO gives low because of miss match data.

The fifth search at 9.3ns, however, introduces a change, as it seeks a logic-1. At this point, the memristors' states are identical to the WRITE operation state, allowing ML to charge, and resulting in MLSO providing a match result. This final search operation demonstrates the versatility of the MTCAM array, showcasing its ability to adapt to various search senario, ultimately returning the desired results.

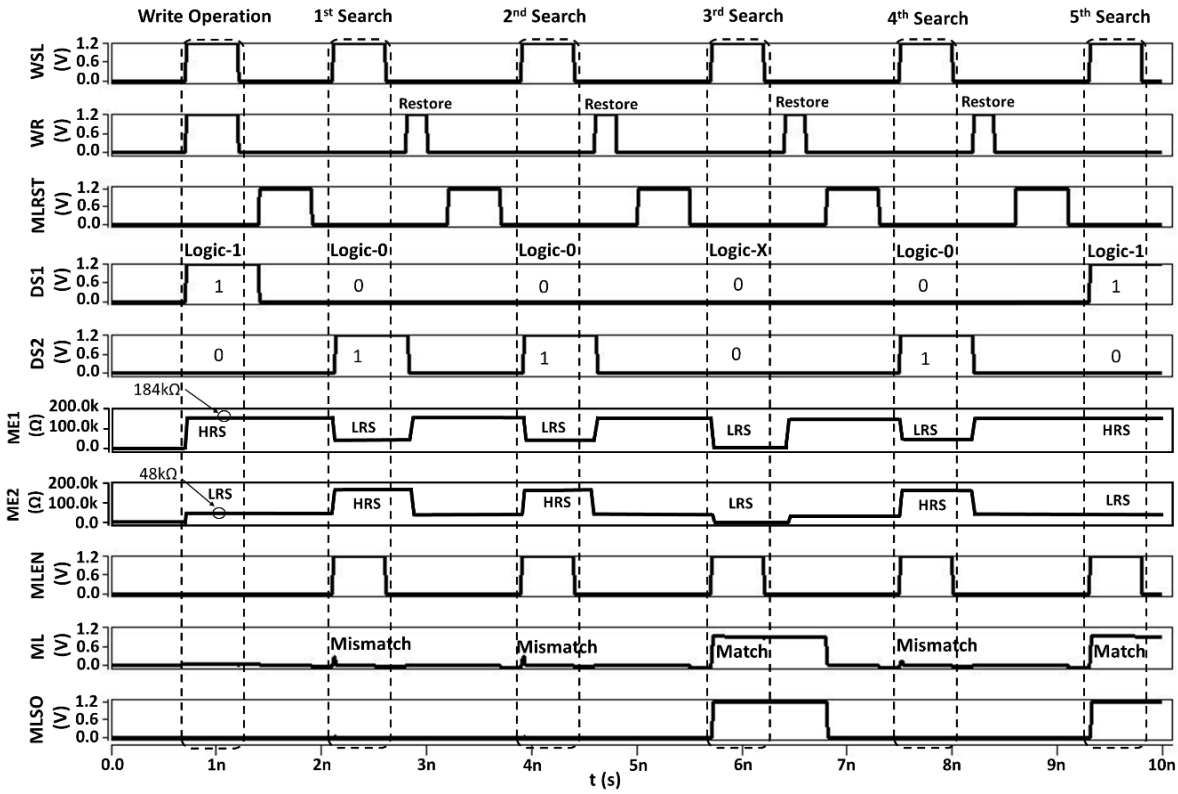



Figure 6.2: Successive search operations

## 6.4 Search Delay

The search delay is a critical parameter in evaluating the performance of a TCAM/MTCAM. There are some factors which may affect the search delay: parallel search mechanism, number of words, word width, speed of the MTCAM, search key complexity, search miss etc. MTCAMs employ a parallel search mechanism, which enables them to compare the search key with all the entries in the memory simultaneously. This parallelism makes MTCAMs extremely fast at finding matching entries. However, the time it takes for this parallel search operation to complete is a significant part of the search delay. The search delay is directly influenced by the number of words or rows in the MTCAM. The more words it has to search through, the longer it will take to locate a match. MTCAM entries are organized into words, and the width of these words plays a role in determining search delay. Typically, MTCAMs support a wide word width, which allows them to compare multiple bits or characters at once. The speed of the MTCAM hardware also affects the search delay. Faster MTCAM devices can complete searches more quickly than slower ones, reducing the search delay. The complexity of the search key itself can

influence the search delay. If the key is longer or more complex, it may take more time to search through the entries for a match. In some cases, the MTCAM may not find a matching entry, resulting in a search miss. The time it takes to determine that there is no match also contributes to the search delay. In this study, the search delay is determined from the rising edge of the Restore and MLSA output signals. In simpler terms, it represents the time gap between the 50% value of the restoring signal and the 50% value of the match result [84]. As illustrated in Figure 6.3, the search delay is evaluated using MLRST, MLEN, DMLSO, and matched ML in a 32×144 array configuration. A search delay of 215ps is achieved for the proposed MTCAM. Subsequent comparison reveals that this search delay is the shortest among existing designs.

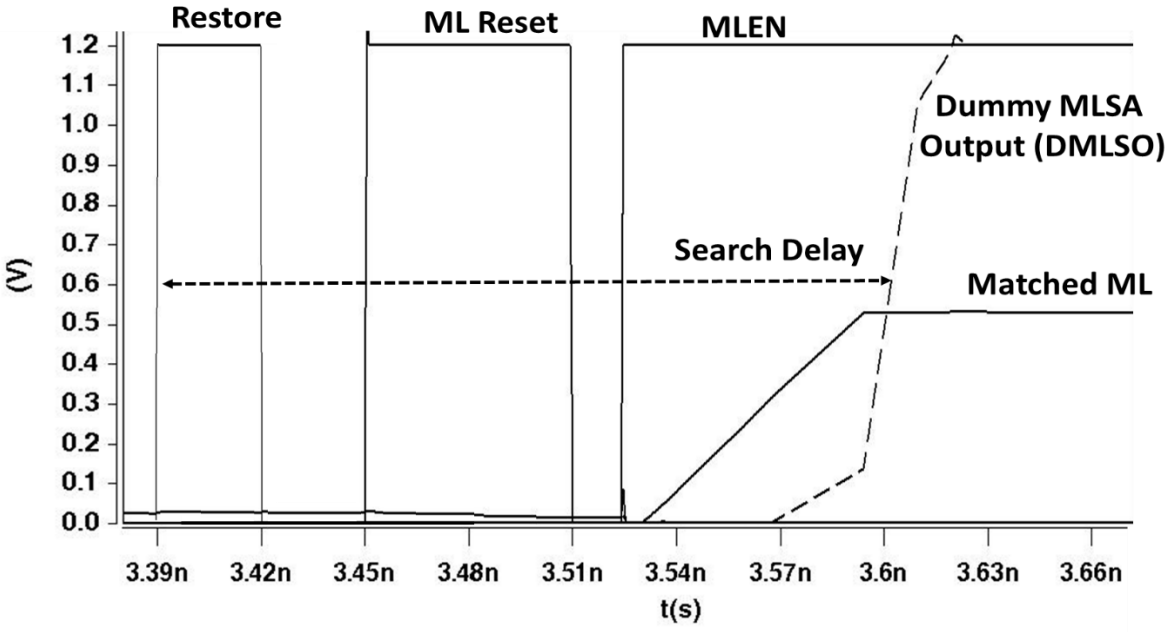



Figure 6.3: Calculating search delay using MLRST, MLEN, DMLSO, and Matched ML in a 32×144 Array

## 6.5 Voltage Margin and Search Energy

In MTCAM, voltage margin stands as a pivotal parameter governing the reliability of SEARCH operations. It denotes the permissible voltage range crucial for accurately comparing stored data. A robust voltage margin ensures the MTCAM cell's ability to effectively discern between matches and mismatches, even amidst noise or fluctuations in the power supply voltage. Defined as the disparity between the sensing threshold voltage of the sensing unit and the maximum voltage applied to a 1-digit mismatched ML segment [84], voltage margin plays a critical role. The sensing threshold voltage is determined by

the intersection of matched MLSO and matched $V_{ML}$. As depicted in Figure 6.4, ML voltage varies between match and 1-digit mismatch scenarios, with matches yielding higher voltages compared to mismatches. Notably, a voltage margin value of 343mV is obtained from the simulation.

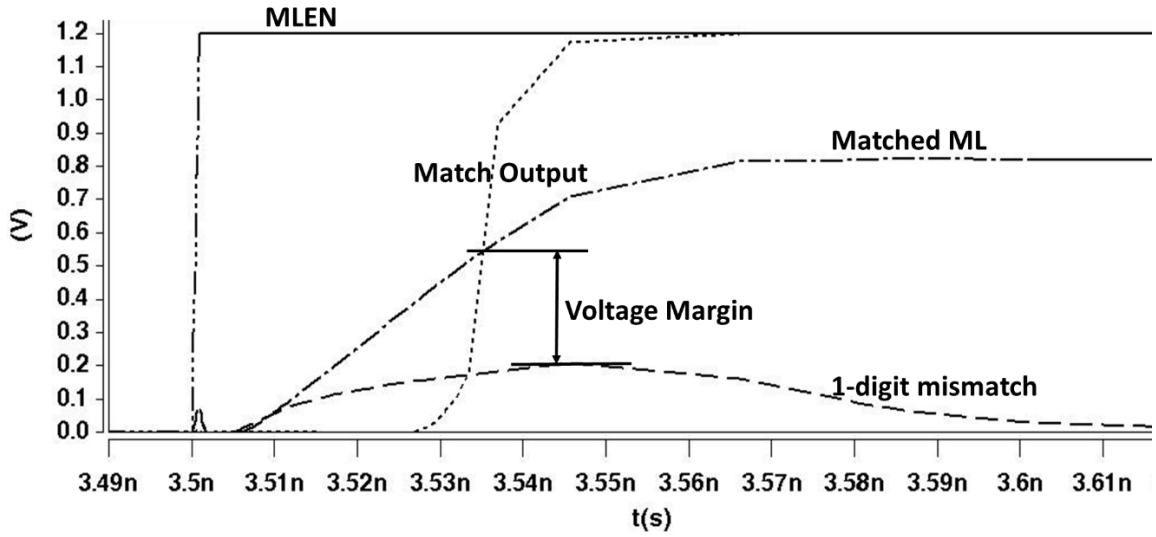



Figure 6.4: ML voltage variation over time in match and 1-digit mismatch scenarios

The search energy per digit per search is assessed across various word mismatch scenarios. Energy consumption per word per search fluctuates across different states, with lower consumption noted in full match conditions compared to mismatches. Additionally, as the number of mismatched digits rises, the energy per word per search also increases. Figure 6.5 illustrates simulated values, highlighting the lowest energy consumption in full match conditions. Furthermore, it's noted that beyond an 8-digit mismatch, the variation in energy values becomes negligible.

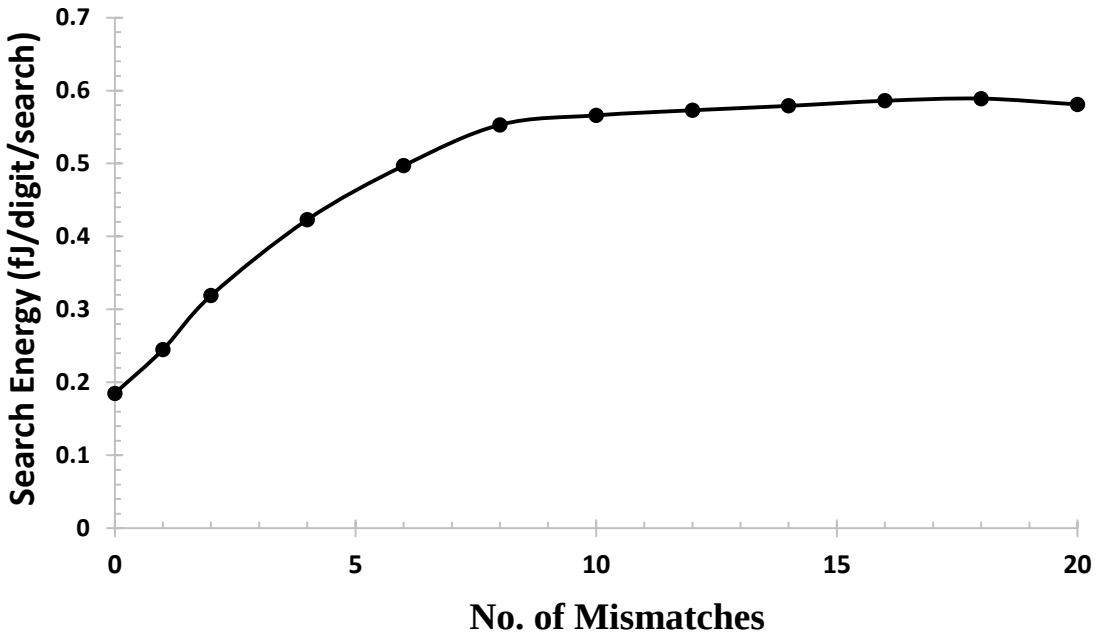



Figure 6.5: Variation in search energy with the number of mismatches

## 6.6 Area Estimation

Area estimation in the context of integrated circuit (IC) design involves determining the physical size or footprint of the chip. It is an important step in the overall chip design process, which includes various stages such as architecture design, logic design, and physical design. Area estimation provides an approximation of how much space on a silicon wafer the chip will occupy, and it helps in planning for manufacturing, cost estimation, and ensuring that the chip will fit within the desired package. Area estimation is typically done using Electronic Design Automation (EDA) tools that simulate and analyze the chip's layout and characteristics. In this research work, the layout is designed in Cadence using GPDK 45nm. To estimate the area of the proposed MTCAM, the layout of a single cell was designed, as illustrated in Figure 6.6. Following optimization, the proposed MTCAM cell measures 2.15μm × 1.51μm, resulting in a total area of 3.25μm².

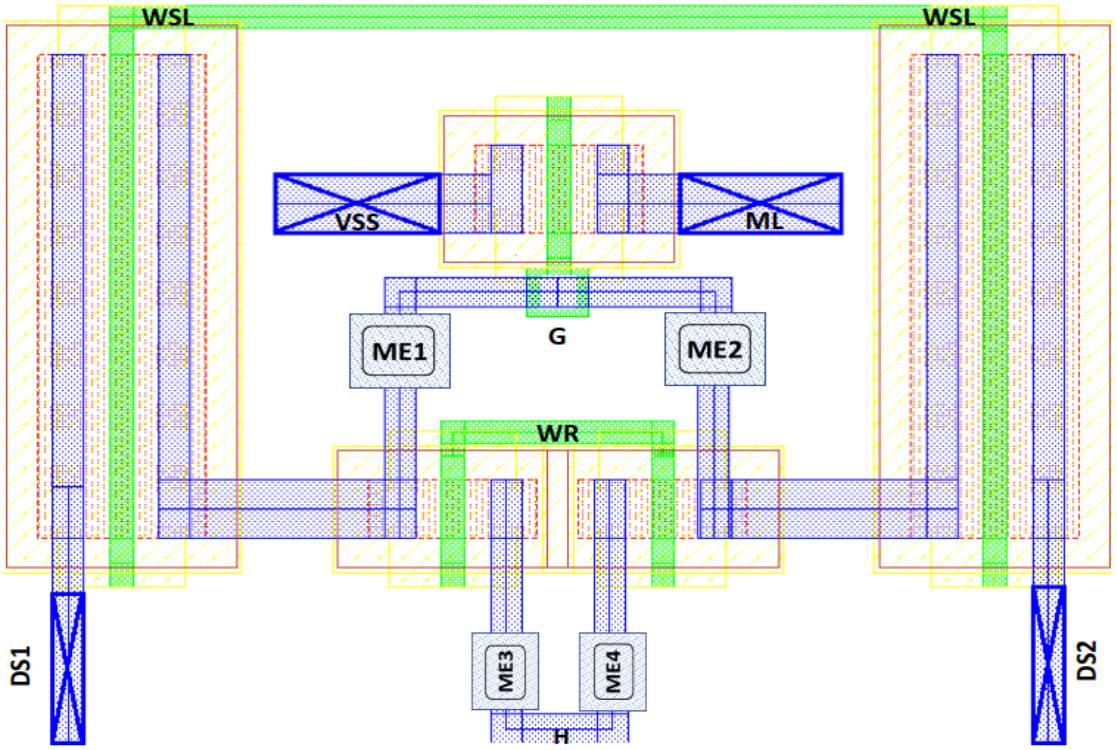



Figure 6.6: To estimate the area of the proposed MTCAM cell, the layout has been designed

## 6.7 Corner Analysis

Corner analysis in VLSI refers to a method used to assess the performance and reliability of integrated circuits under different process variations and operating conditions. VLSI designs are subject to various sources of variation, including manufacturing process variations, temperature fluctuations, voltage fluctuations, and other environmental factors. These variations can affect the performance, power consumption, and reliability of the ICs. Corner analysis involves simulating the performance of an IC design under different "corners" or extreme conditions that represent the range of expected variations. These corners typically include:

**Process corners:** These represent the extremes of manufacturing process variations, such as fast (typically represented by FF for fast-fast) and slow (typically represented by SS for slow-slow) corners. Process corners account for variations in transistor parameters such as threshold voltage, carrier mobility, and oxide thickness.

**Voltage corners:** These represent variations in the supply voltage, including high voltage (HV) and low voltage (LV) corners. Voltage variations can affect the speed, power consumption, and reliability of the IC.

**Temperature corners:** These represent variations in operating temperature, including high-temperature (HT) and low-temperature (LT) corners.

By simulating the IC design under various combinations of process, voltage, and temperature corners, designers can assess how the design performs under different operating conditions. This helps identify potential issues such as timing violations, power consumption outliers, and reliability concerns. Corner analysis is essential for ensuring that the IC design meets performance specifications across a range of operating conditions and manufacturing variations.

This work simulates two extreme corners of process variations: fast-fast (FF) and slow-slow (SS). The FF corner represents the extreme where all process parameters that affect the speed of transistors are at their most favorable values. In other words, transistors in this corner are expected to operate at their highest speeds. This corner is often used to model the best-case scenario for timing analysis, where the goal is to ensure that the design meets timing requirements even under the most favorable conditions. This study replicates this condition by incorporating a +10% fluctuation in the supply voltage (1.2V+0.12=1.32V), operating at a low temperature of -20°C, and incorporating a -10% variation in the threshold voltage (Vth=0.4956-0.05 for NMOS and Vth=-0.4956+0.05 for PMOS). Conversely, the SS corner represents the extreme where all process parameters that affect transistor speed are at their least favorable values. Transistors in this corner are expected to operate at their slowest speeds. This corner is used to model the worst-case scenario for timing analysis, where the goal is to ensure that the design still meets timing requirements even under adverse manufacturing conditions. Again, this study replicates this condition by incorporating a -10% fluctuation in the supply voltage (1.2V-0.12=1.08V), operating at a temperature of 55°C, and incorporating a +10% variation in the threshold voltage (Vth=0.4956+0.05 for NMOS and Vth=-0.4956-0.05 for PMOS). Figure 6.7 shows the search delay and voltage margin values of FF and SS conditions.

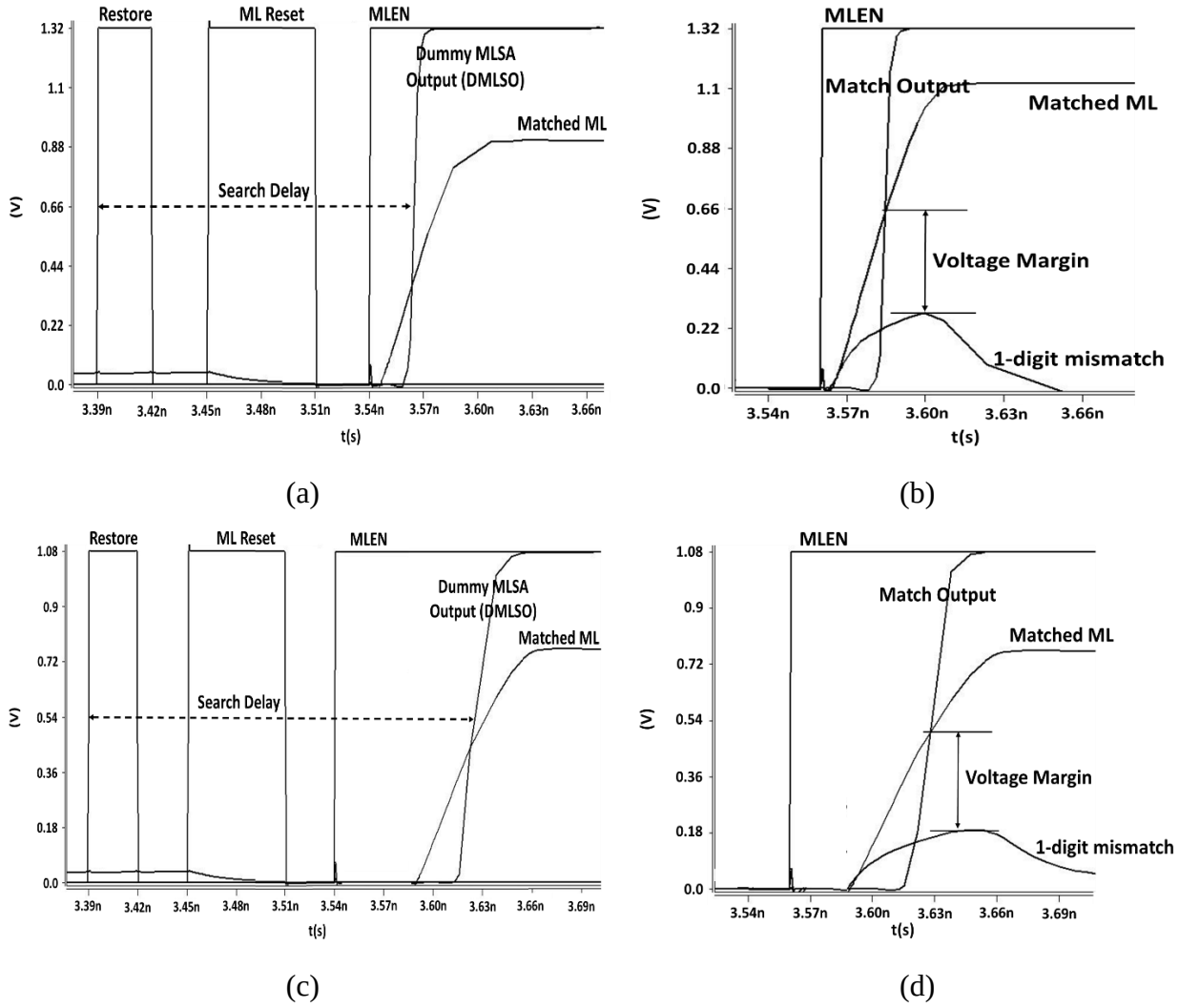



Figure 6.7: Search delay and voltage margin calculation of three conditions: (a) and (b) FF condition, (c) and (d) SS condition

Table 6.2: Corner Analysis values

| **Parameters** | **SS** | **Typical** | **FF** |
|---|---|---|---|
| Search Delay | 232ps | 215ps | 178ps |
| Voltage Margin | 318mV | 343mV | 357mV |

The values provided in Table 6.2 indicate that in the SS condition, the search operation takes 232ps, while in the typical condition, it is slightly faster at 215ps, and in the FF condition, it is the quickest at 178ps. On the other hand, the SS condition shows a voltage margin of 318mV, the typical condition has 343mV, and the FF condition demonstrates the highest voltage margin at 357mV, indicating greater tolerance to voltage

fluctuations or variations. These metrics are crucial for evaluating and optimizing the performance and robustness of the system under consideration.

Figure 6.8 showcases an additional investigation on search delay, specifically illustrating the fluctuation of search time relative to the word length of the proposed MTCAM.

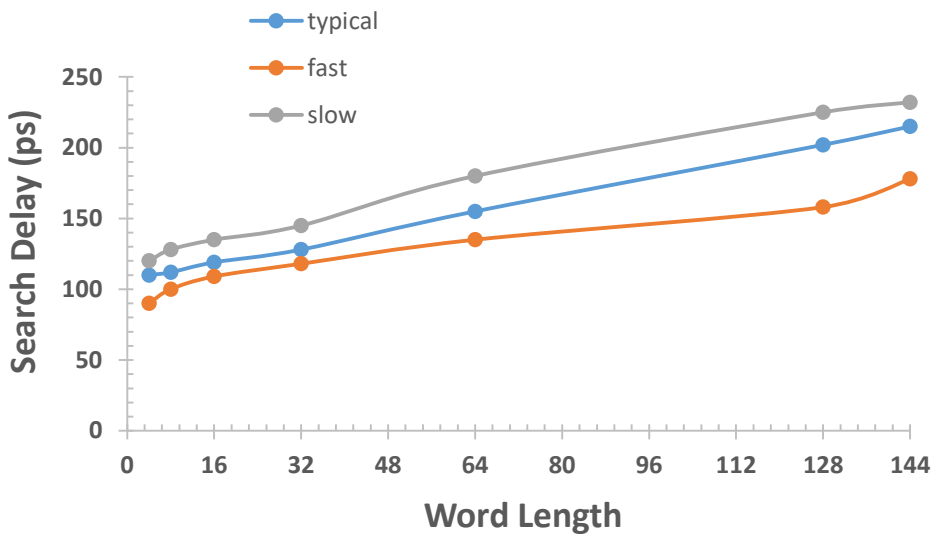



Figure 6.8: Search delay of single mismatch for different word lengths

## 6.8 Performance Evaluation and Comparison

The proposed study involves a comparative analysis with existing design approaches, wherein various parameters have been examined. Observed parameters are write and search voltages, ML sensing scheme, search delay, search energy, voltage margin, data restoring capability, peak power and area estimation. All arrays were simulated under identical conditions, and were optimized. The PTM model used for these designs is 32nm 0.9V strained Si [112]. Comparison between conventional MOSFET-based TCAM and proposed work is shown in Table 6.3. Following that, Table 6.4 provides a comparison of various research endeavors with the proposed work, highlighting their original values. Additionally, Table 6.5 delineates the replicated values of different research efforts alongside the proposed work in the same environment.

Table 6.3: Comparison between conventional MOSFET-Based TCAM and proposed work

| **Parameters** | **[113] (TCAM)** | **Proposed work (MTCAM)** | **Percentage** |
|---|---|---|---|
| Technology | 32nm 0.9V strained Si | 32nm 0.9V strained Si | - |
| Cell Structure | 16T | 5T4M | - |
| Word length | 144 | 144 | - |
| Search Voltage ($V_{Search}$) | 1.2V | 1.2V | - |
| Write Voltage ($V_{write}$) | 1.2V | 1.2V | - |
| ML Sensing Scheme | Precharge-low | Precharge-low | - |
| Search Delay (ps) | 1297.32 | **215** | **83%** |
| Search Energy for worst case mismatches (fJ/digit/search) | 1.437 | **0.556** | **61%** |
| Data Restoring Capability | Not Applicable | **Yes** | - |
| Voltage Margin (mV) | 295.52 | **343** | **14%** |
| Peak Power (mW) | 15.54 | **5.38** | **65%** |
| Cell Area Estimation ($\mu m^2$) | 6.8499 | **3.25** | **53%** |

A complete comparison between conventional MOSFET-based TCAM and proposed work is presented in the Table 6.3. This comparison covers a wide range of important parameters. The MTCAM system is a significant improvement over the conventional TCAM system in a number of ways. Particularly noteworthy is the fact that MTCAM has a more area efficient cell structure with 5T4M (five transistors and four memristors) in comparison to TCAM's 16T (sixteen transistors) structure, which results in a stunning reduction of 53% in the cell area. As a result of this reduction in cell area, total chip density and cost-effectiveness are improved, which is in line with the gains that have been achieved in semiconductor downsizing. In addition, MTCAM displays superior performance measures, such as a reduction of 83% in search delay, a reduction of 61% in search energy consumption for worst-case mismatches, and a considerable reduction of 65% in peak power usage. The potential of MTCAM for high-performance computing and

energy-constrained applications are highlighted by these improvements in speed, energy efficiency, and power consumption. All things considered, the table demonstrates that MTCAM is superior in a number of important features, indicating that content addressable memory technology is heading in a productive route.

Table 6.4: The table compares the original works of different research with proposed work

| **Parameters** | **[104] (MTCAM)** | **[106] (MTCAM)** | **[107] (MTCAM)** | **[108] (MTCAM)** | **Proposed work (MTCAM)** |
|---|---|---|---|---|---|
| Technology | 0.18µm TSMC | 0.18µm TSMC | 45nm PTM | 65nm TSMC | 32nm 0.9V strained Si |
| Cell Structure | 5T2M | 5T2M | 9T2M | 2T2M | 5T4M |
| Word length | 128 | - | 256 | 128 | 144 |
| Search Voltage ($V_{Search}$) | 0.64V | - | 1.2V | 0.7V | 1.2V |
| Write Voltage ($V_{write}$) | 1.5V | - | 1.2V | 3.3V | 1.2V |
| ML Sensing Scheme | Precharge-high | Precharge-high | Precharge-high | Charge-sharing | Precharge-low |
| Search Delay | 2ns | - | 175ps | 0.75ns | **215ps** |
| Search Energy for worst case mismatches (fJ/digit/search) | 0.99 | - | 1.2 | 0.886 | **0.556** |
| Data Restoring Capability | Not applicable | No | Not applicable | Not applicable | **Yes** |
| Voltage Margin (mV) | N/A | N/A | N/A | - | **343** |
| Peak Power (mW) | - | - | - | - | **5.38** |
| Cell Area Estimation ($\mu m^2$) | - | - | 4.73 | 6.11 | 3.2465 |

This Table 6.4 compares different implementations of across various parameters. It includes details such as the technology node and foundry used for simulation, cell structure, word length, search and write voltages, ML sensing scheme, search delay, search energy consumption for worst-case mismatches, data restoring capability, voltage margin, peak power consumption, and cell area estimation. Key differences among the implementations

include variations in technology nodes, cell structures, and search delays, with notable differences in energy consumption and data restoring capability.

Table 6.5: Comparing the research works in the same environment (reproduce)

| **Parameters** | **[104] (MTCAM)** | **[106] (MTCAM)** | **[107] (MTCAM)** | **[108] (MTCAM)** | **Proposed work (MTCAM)** | **Percentage improvement compared to [108]** |
|---|---|---|---|---|---|---|
| Technology | 32nm 0.9V strained Si | 32nm 0.9V strained Si | 32nm 0.9V strained Si | 32nm 0.9V strained Si | 32nm 0.9V strained Si | - |
| Cell Structure | 5T2M | 5T2M | 9T2M | 2T2M | 5T4M | - |
| Word length | 144 | 144 | 144 | 144 | 144 | - |
| Search Voltage ($V_{Search}$) | 0.64V | 0.6V | 1.2V | 0.7V | 1.2V | - |
| Write Voltage ($V_{write}$) | 1.2V | 1.2V | 1.2V | 3.3V | 1.2V | - |
| ML Sensing Scheme | Precharge-high | Precharge-high | Precharge-high | Charge-sharing | Precharge-low | - |
| Search Delay (ps) | 702.3 | 882.1 | 337.4 | 481.5 | **215** | **55%** |
| Search Energy for worst case mismatches (fJ/digit/search) | 0.791 | 1.003 | 0.913 | 0.680 | **0.556** | **18%** |
| Data Restoring Capability | No | No | No | No | **Yes** | **-** |
| Voltage Margin (mV) | N/A | N/A | N/A | 1st Segment = 317.58<br>2nd Segment = 143.22<br>3rd Segment = 121.69<br>4th Segment = 109.3 | **343** | **7%** |
| Peak Power (mW) | 8.12 | 8.33 | 7.02 | 5.97 | **5.38** | **10%** |
| Cell Area Estimation ($\mu m^2$) | 5.71 | 5.165 | 5.61 | **2.95** | 3.25 | - |

The Table 6.5 presents a comparative analysis of various parameters across different MTCAMs, including the proposed work. The percentages highlighted in the table indicate the improvement compared to the referenced technologies. Each design utilizes a different cell structure. All designs store data in 144-digit words, ensuring uniform data handling capabilities. Different designs employ various ML sensing schemes, which affect search speed and power consumption. Ref. [104], [106], and [107] use precharge-high schemes. Ref. [108] uses charge-sharing and lastly, the proposed work uses precharge-low CR ML sensing scheme. Previous implementations utilized distinct voltages for search and write functions, necessitating multiple power sources. Conversely, this study adopts a unified voltage for both SEARCH and WRITE operations. Search delay is the time it takes to perform a search operation. It varies for different designs, with lower values indicating faster search operations. The proposed work performs search with the lowest search delay of 215ps. For instance, the search delay for this work demonstrates a significant reduction by 55% compared to the most recent MTCAM implementation [108]. Search energy is measured in femtojoules (fJ) per digit per search operation. Lower values indicate lower energy consumption. Again, the proposed work has the lowest value of 0.556fJ/digit/search. The search energy shows an 18% decrease in energy consumption compared to [108]. All designs, except the proposed work, do not have data restoring capability, which means they cannot recover data in case of overwrite. The proposed work stands out as it offers data restoring capability. Furthermore, the proposed work achieves a voltage margin of 343mV. It's noteworthy that voltage margin values cannot be measured for other designs, except those employing the charge-sharing ML sensing technique, as they utilized precharge-high ML sensing. Moreover, the voltage margin of the proposed work exceeds that of [108] by 7%, implying better stability and reliability. Notably, the peak power consumption of the proposed work is 10% lower than [108], suggesting enhanced energy efficiency. The estimated area for the proposed MTCAM cell has been calculated as $3.25\mu m^2$. Since the proposed design utilizes only five transistors and four memristors, its estimated area is comparatively smaller than others except [108]. Furthermore, the absence of a PMOS structure (no n-well) and the deliberate circuit arrangement contribute to a reduced area footprint. Consequently, the proposed MTCAM cell occupies less estimated area compared to the 5T2M design. In summary, it's evident

that the proposed MTCAM cell offers reduced search time, lower search energy, a larger voltage margin, data restoration capability, and superior area efficiency compared to existing designs.

## 6.9 Summary

This study presents a compact MTCAM cell comprising five transistors and four memristors, offering a novel data retrieval method. Since the same lines serve both WRITE and SEARCH operations, there's a risk of data overwriting during searches. To tackle this, the proposed MTCAM integrates a data recall unit. Furthermore, it maintains a consistent voltage level during WRITE and SEARCH operations. Implemented in 32×144 arrays, the proposed MTCAM design is assessed against existing ones. It demonstrates reduced search delay and energy consumption, along with superior voltage margin values. Moreover, due to its minimized transistor and memristor usage, it occupies a smaller footprint compared to most alternatives.

# Chapter 7

# Conclusion and Future Work

## 7.1 Conclusion

This research work introduces a novel energy- and area-efficient structure of MTCAM, designed for applications demanding high speed and low power consumption. The MTCAM cell comprises five transistors and four memristors. While significant research has been conducted in this area, this work presents a fresh approach to data preservation and protection. One notable challenge addressed is the potential overwriting of stored data during SEARCH operations, which share input lines with WRITE operations. The proposed MTCAM includes a data recall unit to mitigate this issue. Additionally, the architecture utilizes the same voltage for both WRITE and SEARCH operations, enhancing efficiency and simplicity.

The SPICE simulation involved an array comprising 32 words, each containing 144 MTCAM cells. The design utilized 32nm 0.9V strained Si technology throughout. Employing a precharge-low CR scheme yielded impressive results: a search time as low as 215ps and a search energy of 0.556fJ/digit/search for worst-case mismatches at a supply voltage of 1.2V, with a observed voltage margin of 343mV. Comparing this approach to conventional MOSFET-based TCAM, the advantages are clear: an 83% reduction in search delay, a 61% decrease in search energy consumption, a 14% enhancement in voltage margin, a 65% decrease in peak power consumption, and a 53% reduction in estimated area. Moreover, in contrast to the latest existing MTCAM design, the proposed approach offers a 55% decrease in search delay, an 18% improvement in search energy efficiency, a 7% enhancement in voltage margin, and a 10% reduction in peak power consumption. Notably, the area occupied by the suggested MTCAM cell is significantly smaller compared to other designs.

## 7.2 Limitation

- Although the proposed design includes measures to prevent data overwrite during SEARCH operations, the effectiveness of the data recall unit in preserving data integrity under various operational conditions and in long-term usage scenarios requires further investigation.

- The reported simulation results are based on HSpice simulations conducted using specific technology parameters (32nm 0.9V strained Si). The performance of the proposed MTCAM design may vary under different process technologies, and its scalability to newer process nodes may be evaluated.
- While the proposed architecture utilizes the same voltage level for WRITE and SEARCH operations to improve efficiency, the compatibility of this approach with different power supply configurations and voltage scaling techniques needs consideration. Voltage compatibility issues may arise when interfacing with other circuit blocks or integrating the MTCAM design into larger systems.

## 7.3 Future Work

- Explore the integration of emerging non-volatile memory technologies, such as resistive RAM (RRAM) or phase-change memory (PCM), to replace or complement memristors in MTCAM cells. Assess their suitability in terms of performance, endurance, and scalability.
- Extend the analysis to evaluate the performance and scalability of the proposed MTCAM design across a range of process technologies, including advanced nodes beyond 32nm. Investigate optimization strategies to adapt the design to varying process parameters and technology trends.
- Developing rigorous characterization and testing methodologies for MTCAM can help identify and mitigate potential issues early in the development process.
- Investigate dynamic voltage scaling techniques and power management strategies tailored specifically for MTCAM architectures. Explore opportunities to optimize power consumption during both idle and active states while maintaining high-speed operation.

Overall, future work should be multidisciplinary, involving materials scientists, device engineers, circuit designers, computer architects, and system integrators. Collaborative efforts can help overcome the shortcomings and accelerate the adoption of MTCAM in high-speed and low-power applications.

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