3-D Model of Wrap Around CNTFET with Multiple CNT Channel and Analytical Modeling of Its Capacitances

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The thesis entitled **"3-D Model of Wrap Around CNTFET with Multiple CNT Channel and Analytical Modeling of Its Capacitances"** submitted by Md. Rakibul Karim Akanda, Student No.: 0411062201, Session: April, 2011 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on May 7, 2013.

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This thesis titled “3-D Model of Wrap Around CNTFET with Multiple CNT Channel and Analytical Modeling of Its Capacitances” was solely done by me with the help of my supervisor and was not submitted anywhere for any degree and diploma.

Md. Rakibul Karim Akanda _____

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Abstract

Wrap around CNTFET has gate around it except the bottom portion. Wrap around gate carbon nanotube field effect transistor (CNTFET) has the advantage of more accurately controlled channel than top gated CNTFET. 3-D simulation is performed using Finite Element Method (FEM) to model wrap around CNTFET with multi-CNT channel. For predicting the device speed, capacitance modeling is necessary. Along with gate to channel capacitance, there are fringing capacitance as well. Analytical expressions to model various capacitances of the same device are also derived from capacitances for 1-D FET with multiple cylindrical conducting channels incorporating screening effect due to multiple CNT. Various capacitances thus obtained exhibit remarkable improvement over planar top gate device with multiple conducting channels. This is attributed to the charge enhancement and better charge confinement in the channel of the wrap around CNTFET with multi-CNT channel. Capacitances are also extracted from the proposed FEM model. The extracted capacitances are in excellent agreement with the capacitances obtained from the analytical model presented in this study.

Temperature distribution of wrap around CNTFET with multi-cnt is presented in this paper. For predicting the device characteristics, temperature modeling is necessary. Temperature distribution is changed due to multi-cnt as voltage of adjacent cnt affects temperature of mid cnt. Again it is also changed by temperature dependent thermal conductivity of single walled carbon nano tube (SWCNT). Current flow is changed both due to multi-cnt wrap around structure and due to the temperature change. So, temperature has a great impact on current modeling and thus on device characteristics. All these issues are considered in this paper using finite element method.

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Chapter 1

Introduction

As the gate length of MOSFET has entered the deep submicron region, 65 nm technology becomes the mainstream since 2006, and 45 nm technology has been announced in 2007. As CMOS continues to scale deeper into the nanoscale, various device non-idealities cause the I-V characteristics to be substantially different from well-tempered MOSFETs. It becomes more difficult to further improve device/circuit performance by reducing the physical gate length. The discrepancy between the fabricated physical gate length and the ITRS [1] projected gate length becomes larger as the technology advances. On the other hand, as the major driving force for the semiconductor industry, the device contacted gate pitch (L_{pitch}) is scaled down by a factor of 0.7 every technology node. Reasonable questions to ask are: Will the MOSFET scaling be stopped? Is there a way to extend the silicon technology roadmap? After silicon technology, or as a complement to silicon technology, is there any potential technology that may be used?

The last few years witnessed a dramatic increase in nanotechnology research, especially the nanoelectronics. These technologies vary in their maturity, as illustrated by Fig. 1.1. The exciting opportunity is to design complex electronic circuits using the cutting-edge silicon technology and/or the novel nanometer-scale transistors in the future.

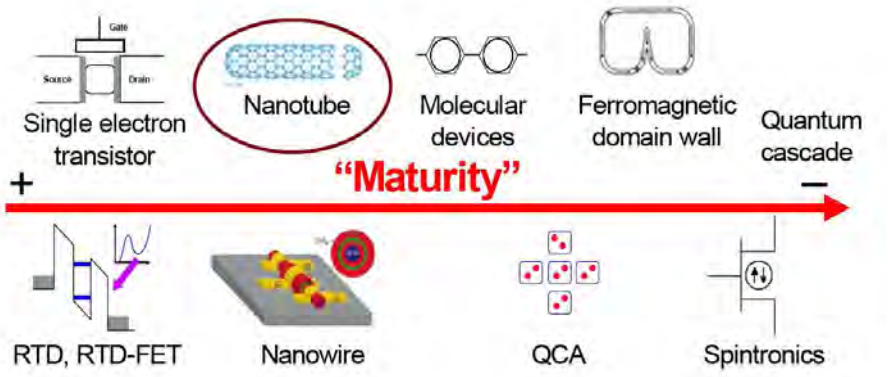

Figure 1.1: The novel nanoelectronic technologies in order of their maturity (presented at [2])

Carbon nanotubes (CNTs) are at the forefront of these new materials because of the unique mechanical and electronic properties. Carbon nanotube field effect transistor (CNFET) is the most promising technology to extend or complement traditional silicon technology due to three reasons: First, the operation principle and the device structure are similar to CMOS devices; we can reuse the established CMOS design infrastructure. Second, we can reuse CMOS fabrication process. And the most important reason is that CNFET has the best experimentally demonstrated device current carrying ability to date [3],[4].

1.1 Nanoscale MOSFET

Technology boosters such as strain have helped the continuation of CMOS historic performance trend up to 45 nm node. As device physical gate length is reduced to below 25 nm technology node, various leakage currents and device parameter variation become the most important considerations for device optimization. In fact, it can be argued that reduction of gate length below 25 nm may not offer the same advantage as short-gate devices had provided historically in terms of power and performance at

the system level. The major detractors are: the lack of a thin equivalent gate oxide (with low leakage current) for effective short channel effect control, the increasing contribution of the fringing parasitic capacitance to the total gate capacitance, and the rising contribution of the source/drain resistance to the total device on-resistance. A reasonable question to ask is: if the gate length scaling stops, can we achieve performance gains through a different device scaling scenario?

1.2 Carbon Nanotube Field-Effect Transistors

As one of the promising new devices, CNFET avoid most of the fundamental limitations for traditional silicon devices. All the carbon atoms in CNT are bonded to each other with sp^2 hybridization and there is no dangling bond which enables the integration with high-k dielectric materials. In the next section, we will introduce the basic properties of CNFET, and will describe the problem to be modeled.

1.3 Thesis Organization

This thesis is divided into five chapters. Chapter 1 provides a brief introduction of the thesis report. Basic idea about CNTFET is given here. Chapter 2 describes some basic physics of device. These device concepts are used in this thesis. The device structure, ballistic transport, fermi level and schottky concept is discussed. Apart from these, different types of existing structure of CNTFET is presented here with their advantages and disadvantages. Our proposed model is also introduced here with its three dimensional structure as well as its cross sectional view. Chapter 3 explores

different capacitances in CNTFET. Gate to channel capacitance, outer fringing capacitance and gate to drain/source capacitance are discussed. Comsol model of our structure to calculate different capacitances is also presented here. Comparison among different results are shown here. Chapter 4 describes the temperature effect on I-V characteristics.

Finally, summary of the major accomplishments of this thesis is stated in chapter 5. Possible future works are also included.

Chapter 2

Technical Background

The purpose of this chapter is to give a brief explanation of the physics which describes FET operation. A Field Effect Transistor or FET is a three terminal electronic device consisting of a Source, Drain, and Gate. Negatively charged carriers or electrons flow from the source to the drain via the channel. So the conventional current flow in CNTFET is from drain to source. The channel is a doped region in the semiconductor and basically offers good conduction. The channel can be p-type or n-type.

2.1 Carbon Nanotube

Carbon atom has an electron configuration of $1s^2 2s^2 2p^2$ in its normal state. In graphene, sp^2 hybridization occurs through covalent bonding. A carbon atom in graphene assembles in a single-sheet hexagonal lattice. The inter-carbon-atom distance within the hexagonal lattice (d) is approximately 1.44 , and the angle between carbon-carbon bonds (σ-bond) is 120 degrees. The lattice constant (a) is given by $\sqrt{3}d = 2.49\dot{A}$. The 2p electrons from all the atoms on a lattice form a delocalized - orbital between the two adjacent sheets. The inter-layer spacing between the multiple sheets in graphene is about $3.35\dot{A}$. The weak electrostatic interactions between the sheets make it possible to assume the electrical characteristics of the graphite sheets

are independent each other.

The dispersion relation for graphene, obtained by the Slater-Koster tight-binding scheme, considering only the π-orbital, is given by,

$$E_{g2D}(k_x, k_y) = \pm V_\pi \{1 + 4cos(\frac{\sqrt{3}k_x a}{2})cos(\frac{k_y a}{2}) + 4cos^2(\frac{k_y a}{2})\}^{\frac{1}{2}} \tag{2.1.1}$$

Where (k_x,k_y) are wavevectors, $V_{/pi}$ is the transfer integral (or the nearest-neighbour parameters). Fig. 2.1 illustrates the band structure calculated with the above equation. The high-symmetry points are indicated by capital letters. K-points are degenerate, indicating the zero-bandgap (semi-metallic) characteristic of graphene sheet.

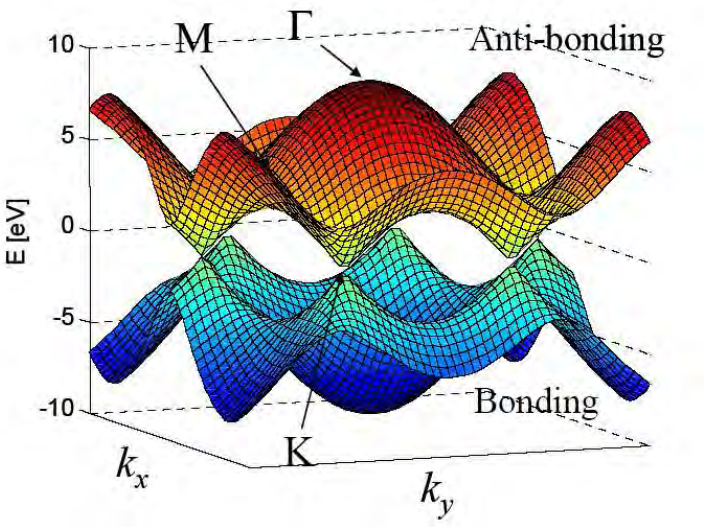

Figure 2.1: 3D energy band diagram

A single-walled carbon nanotube (SWCNT) can be visualized as a sheet of graphite which is rolled up and joined together along a wrapping vector $C_h = n_1 \cdot \bar{a}_1 + n_2 \cdot \bar{a}_2$, where $[\bar{a}_1, \bar{a}_2]$ are lattice unit vectors as shown by Fig. 2.2, and the indices (n_1, n_2) are positive integers that specify the chirality of the tube [5].

The length of C_h is thus the circumference of the CNT, which is given by [5],

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{2.1.2}$$

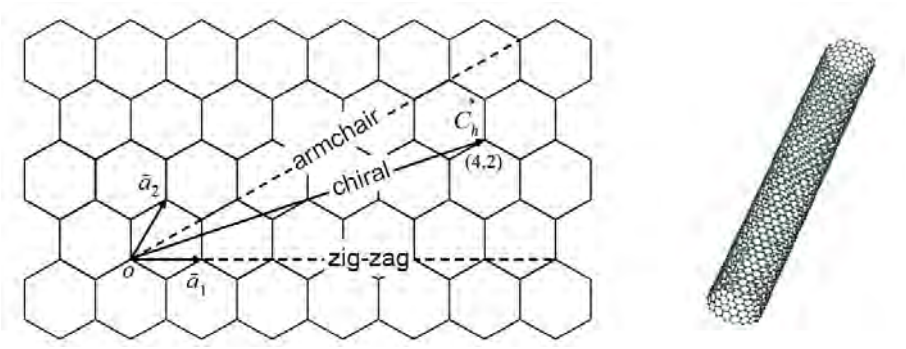

Figure 2.2: Chirality of CNT

Single-walled CNTs are classified into one of three groups, depends on the chiral number (n_1, n_2): (1) armchair $(n_1 = n_2)$, (2) zigzag ($n_1 = 0$ or $n_2 = 0$), and (3) chiral (all other indices).

The diameter of the CNT is given by the formula $D_{CNT} = C_h/\pi$. The typical diameters of CNTs are about several nanometers. Due to the small diameter of CNT, the quantization of wavevector in the circumferential direction occurs. A general analytic E-k dispersion relation for CNT is obtained by applying periodic boundary conditions in the circumferential direction to the 2D graphite sheet E-k dispersion relation.

To be compatible with the quasi 1D structure of CNT, we can convert the (k_x, k_y) coordinate to (k_t, m), where the wavevector k_t is in the direction of transport, and m is quantization number in the circumferential direction. Analytically, the dispersion of CNT is given by the formula [5],

$$E_{CNT}(k_t, m) = \pm V_\pi \{1 + 4cost_1 cost_2 + 4cos^2 t_2\}^{\frac{1}{2}} \tag{2.1.3}$$

where the parameters are given by,

$$t_2 = \frac{\sqrt{3}a}{4}\frac{n_2 + n_1}{n}k_t + \frac{\pi}{2}\frac{3n_1 - n_2}{n^2}m$$

$$t_1 = \frac{\sqrt{3}a}{4}\frac{n_2 - n_1}{n}k_t + \frac{\pi}{2}\frac{n_1 + 3n_2}{n^2}m$$

$$n^2 = n_1^2 + n_2^2 + n_1 n_2 \tag{2.1.4}$$

$$-\frac{\pi \cdot d_R}{\sqrt{3}a \cdot n} < k_t < \frac{\pi \cdot d_R}{\sqrt{3}a \cdot n}$$

$$m = 0 : \frac{2n}{d_R} - 1$$

$$d_R = gcd(2n_1 + n_2 \cdot 2n_2 + n_1)$$

In terms of the electrical conductivity, SWCNT is either metallic (when $|n_1 n_2|$ is a multiple of 3) with zero bandgap or semiconducting with finite bandgap. The band structure for both metallic CNTs and semiconducting CNTs are illustrated by Fig. 2.3, using both armchair SWCNTs and zigzag SWCNTs as examples.

Chiral, armchair Fig. 2.4 SWCNTs ($n_1 = n_2$) and zigzag Fig. 2.5 SWCNTs ($n_1 n_2 = 0$) are metallic, and the others ($|n_1 n_2|$ is a multiple of 3 but $n_1 \neq n_2$ and $n_1 n_2 \neq 0$) are quasimetallic with small bandgap.

The density of states (DOS) can be obtained as,

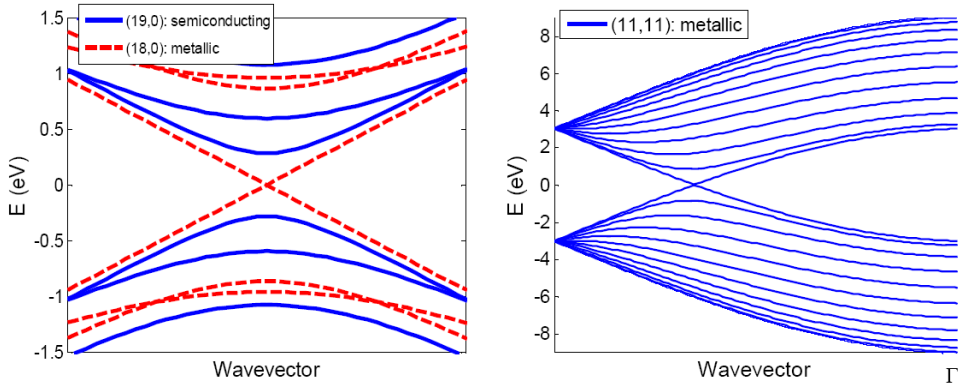

Figure 2.3: 1D energy band diagram

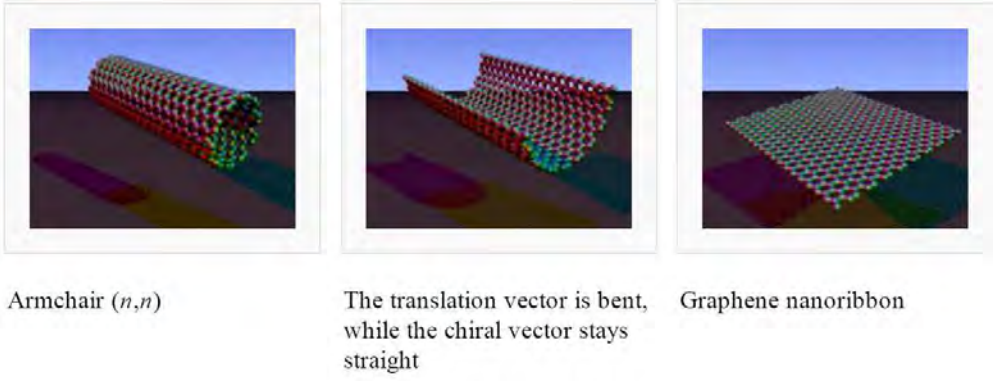

Figure 2.4: Armchair structure

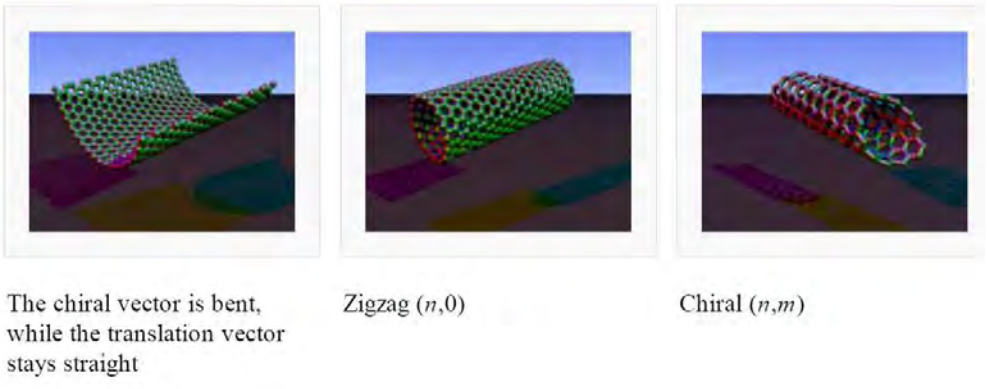

Figure 2.5: Zigzag and Chiral structure

$$g(E) = \frac{2}{\pi} \sum_{m} \int |\frac{\delta E_{CNT}}{\delta k_t}|^{-1} dE_{CNT} \tag{2.1.5}$$

The electrons in CNT are confined within the atomic plane of graphene. Due to the quasi 1D structure of CNT, the motion of the electrons in the nanotubes is strictly restricted.

Electrons may only move freely along the tube axis direction. As a result, all wide angle scatterings are prohibited. Only forward scattering and backscattering due to electron phonon interactions are possible for the carriers in nanotubes. The experimentally observed ultra long elastic scattering mean-free-path (MFP) [6,7,8,9] ($\sim 1\mu m$) implies ballistic or near-ballistic carrier transport. High mobility, typical in the range of $10^3 \sim 10^4\ cm^2/V \cdot s$ which are derived from conductance experiments in transistors, has been reported by a variety of studies [10,11]. Theoretical study also predicts a mobility of $\sim 10^4\ cm^2/V \cdot s$ for semiconduting CNTs [12]. The current carrying capacity of multi-walled CNTs are demonstrated to be more than 10^9 A/ cm^2, about 3 orders higher than the maximum current carrying capacity of copper which is limited by the electron migration effect, without performance degradation during operation well above room temperature [13]. The superior carrier transport and conduction characteristic makes CNTs desirable for nanoelectronics applications, e.g. interconnect and nanoscale devices.

2.2 CNTFET

The quasi-1D device structure provides better gate electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI) structures [14]. In terms of the device operation mechanism, CNFET can be categorized as either Schottky Barrier (SB) controlled FET (SB-CNFET) or MOSFET-like

FET [15]. The conductivity of SB-CNFET is governed by the majority carriers tunneling through the SBs at the end contacts. The on-current and thereby device performance of SB-CNFET is determined by the contact resistance due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance, as shown by Fig. 2.6(a). The SBs at source/drain contacts are due to the Fermi-level alignment at the metal-semiconductor interface. Both the height and the width of the SBs, and therefore the conductivity, are modulated by the gate electrostatically. SB-CNFET shows ambipolar transport behavior. The work function induced barriers at the end contacts can be made to enhance either electron or hole transport. Thus both the device polarity (n-type FET or p-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts [16]. On the other hand, MOSFET like CNFET exhibits unipolar behavior by suppressing either electron (pFET) or hole (nFET) transport with heavily doped source/drain. The non-tunneling potential barrier in the channel region, and thereby the conductivity, is modulated by the gate-source bias Fig. 2.6 (b).

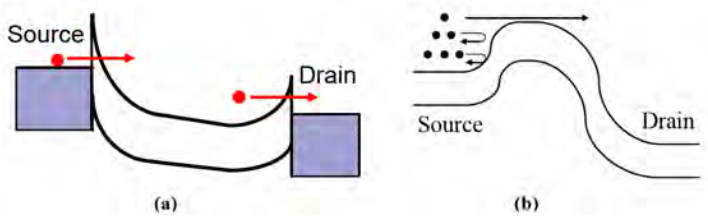

Figure 2.6: (a)SB-like and (b) MOSFET like energy band diagram

The first fabricated CNFET devices with Au or Pt source/drain metal contacts were reported in 1998 [17,18]. The gate dielectric material was a thick SiO_2 layer. A highly doped Si back gate was used to control the conductivity. The Al_2O_3 gate dielectric was introduced to improve the gate controllability over the channel region

[19]. The front gate device structure, by placing the gate electrode over the thin gate oxide that covers CNT, was used to further improve the channel electrostatics [20]. Better gate electrostatics was achieved by using high-k, e.g. HfO_2, gate dielectric material [21]. The source/drain contacts using a variety of metals (Ti, Ni, Al, Pd,) were fabricated to study the effect of the work function difference between the metal contacts and CNT on device conductivity. Ti source/drain metallization was reported to be efficient on reducing the contact resistance [22]. The device fabricated with Pd source/drain metal contact, Al gate electrode, and HfO_2 gate dielectric was reported to achieve excellent dc characteristics.

Logic circuits with field-effect transistors based on single carbon nanotubes have been demonstrated in the past few years. In 2001, [23] demonstrated one, two, and three transistor circuits that exhibit a range of digital logic operations, including an inverter, a logic NOR, a static random-access memory (SRAM) cell, and an three-stage ac ring oscillator operating at 5 Hz. A five-stage CMOS type nanotube ring oscillator using palladium p-type gates and aluminum n-type gates was reported in 2006 [24]. Owing to the compact device or circuit design, this ring oscillator works at a frequency of 72 MHz. Regarding RF analog application using CNFET, the first demonstration of ac gain in a single-walled carbon nanotube common-source amplifier was reported in 2006 [25]. The low frequency gain was almost 11.3 dB, and the unity-gain frequency was about 560 kHz which was mostly limited by the parasitic load capacitance.

While the CNT synthesis or fabrication technique and the performance of CNFET devices and circuits have been significantly improved since the first fabricated device in 1998, CNFETs is still premature for very large scale integrated (VLSI) circuits design and commercial use. Efforts have been made in recent years on modeling semiconducting CNFET [26,27,28,29] for digital logic applications and CNT for

interconnects in order to evaluate the potential performance at the device level.

2.3 Top gated CNTFETs

Eventually, researchers migrated from the back-gate approach to a more advanced top-gate Fig. 2.7 fabrication process. In the first step, single walled carbon nanotubes are solution deposited onto a silicon oxide substrate. Individual nanotubes are then located via atomic force microscope or scanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high resolution electron beam lithography. A high temperature anneal step reduces the contact resistance by improving adhesion between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric, completing the process. Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case. Also, due to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally preferred over back-gated CNTFETs, despite their more complex fabrication process.

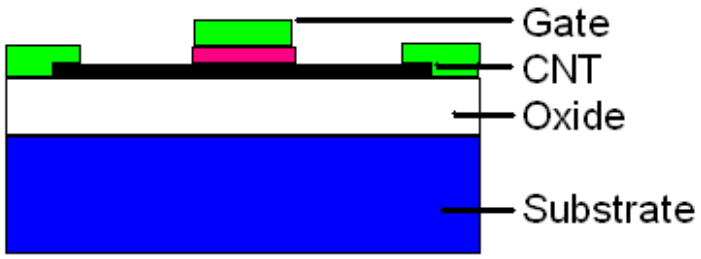

Figure 2.7: Top gated CNTFET

2.4 Gate all-around CNTFETs

Gate-all-around CNTFETs Fig. 2.8 were developed in 2008, and are a further improvement upon the top-gate device geometry. In this device, instead of gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated. This should ideally improve the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

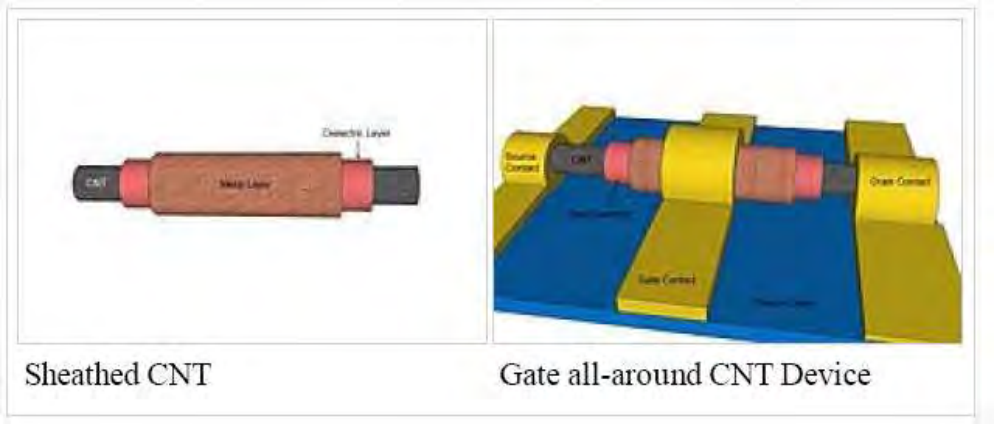

Figure 2.8: Gate all-around CNTFET

Device fabrication begins by first wrapping CNTs in a gate dielectric and gate contact via atomic layer deposition. These wrapped nanotubes are then solution-deposited on an insulating substrate, where the wrappings are partially etched off, exposing the ends of the nanotube. The source, drain, and gate contacts are then deposited onto the CNT ends and the metallic outer gate wrapping.

2.5 Suspended CNTFETs

Yet another CNTFET device geometry involves suspending the nanotube over a trench to reduce contact with the substrate and gate oxide. This technique has

the advantage of reduced scattering at the CNT-substrate interface, improving device performance. There are many methods used to fabricate suspended CNTFETs (Fig. 2.9), e.g. growing them over trenches using catalyst particles, transferring them onto a substrate and then underetching the dielectric beneath, and transfer-printing onto a trenched substrate.

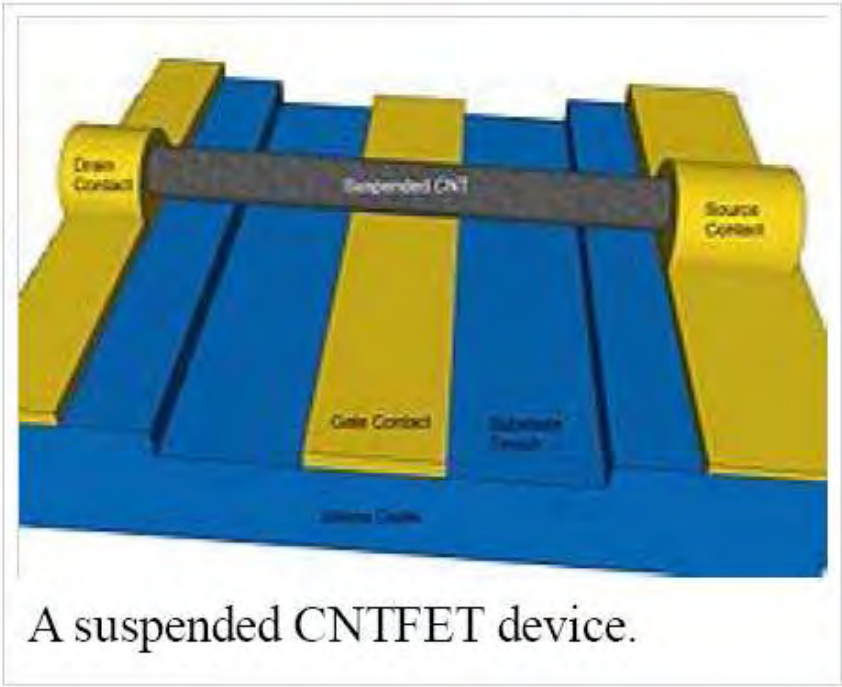

Figure 2.9: Suspended CNTFET

The main problem suffered by suspended CNTFETs is that they have very limited material options for use as a gate dielectric (generally air or vacuum), and applying a gate bias has the effect of pulling the nanotube closer to the gate, which places an upper limit on how much the nanotube can be gated. This technique will also only work for shorter nanotubes, as longer tubes will flex in the middle and droop towards the gate, possibly making touching the metal contact and shorting the device. In general, suspended CNTFETs are not practical for commercial applications, but

they can be useful for studying the intrinsic properties of clean nanotubes.

2.6 Proposed CNTFETs: Wrap Around with Multi-CNT

The proposed stucrure is shown in 3D Fig. 2.10 and 2D

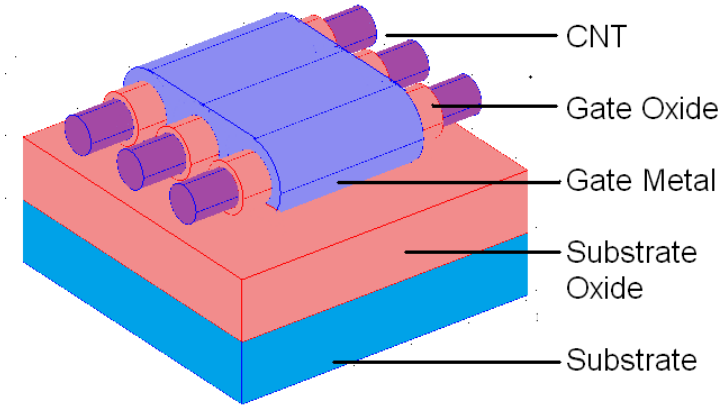

Figure 2.10: Proposed wrap around CNTFET with multiple gate (3D view)

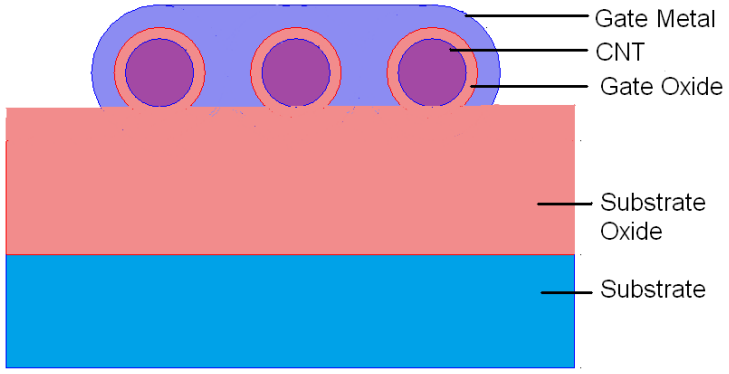

Figure 2.11: Proposed wrap around CNTFET with multiple gate (2D view)

2.7 Ballistic Transport

Ballistic conduction or Ballistic transport is the transport of electrons in a medium with negligible electrical resistivity due to scattering. Without scattering, electrons simply obey Newton's second law of motion at non-relativistic speeds.

In general, the resistivity exists because an electron, while moving inside a medium, is scattered by impurities, defects, or by the atoms/molecules composing the medium that simply oscillate around their equilibrium position (in a solid), or generically by any freely moving atom/molecule composing the medium, in a gas or liquid. For a given medium one can associate to a moving electron a mean free path as the average length that the electron can travel freely, i.e. before hitting against something and deviating from its original path, possibly losing some kinetic energy. The mean free path can be increased by reducing the number of impurities in a crystal or by lowering its temperature (except for some material like semi-conductors). Ballistic transport is observed when the mean free path of the electron is (much) bigger than the size of the box that contains/delimits the medium through which the electron travels, such that the electron alters its motion only by hitting against the walls. In the case of a wire suspended in air/vacuum the surface of the wire plays the role of the box reflecting the electrons and preventing them from exiting toward the empty space/open air. This is because there is an energy to be paid to extract the electron from the medium (work function). E.g. ballistic transport can be observed in a metal nanowire: this is simply because the wire is of the size of a nanometer (10 meters) and the mean free path can be bigger than that in a metal.

Ballistic conduction is the unimpeded flow of charge or energy carrying particles over relatively long distances in a material. Normally, transport of electrons (or holes) is dominated by scattering events, which relax the carrier momentum in an

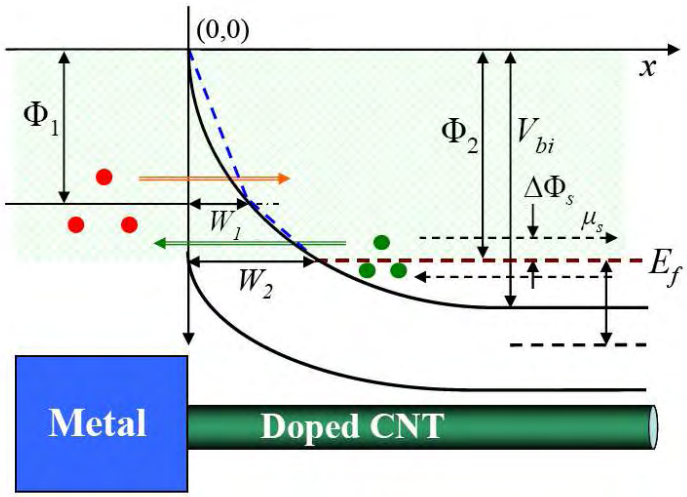

Figure 2.12: Energy band diagram of CNTFET

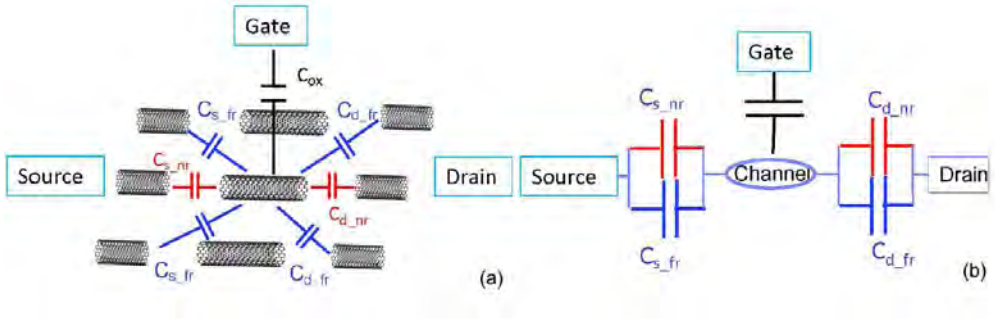

Figure 2.13: Equivalent circuit of CNTFET

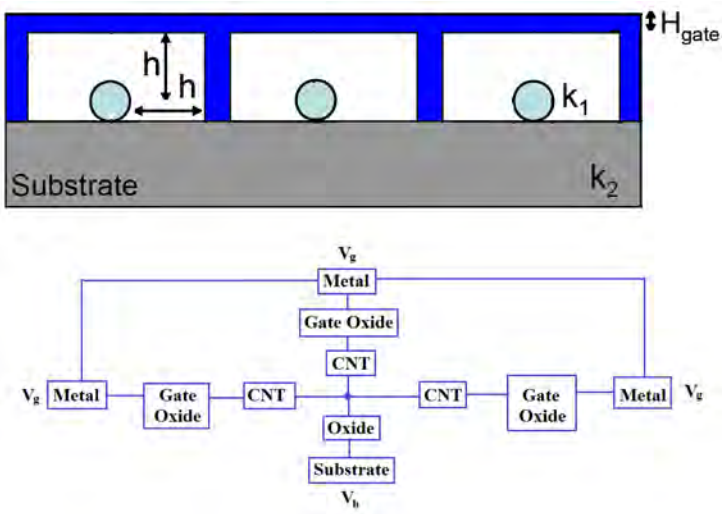

Figure 2.14: Potential in a wrap around CNTFET. k_1 represents gate oxide and k_2 represents substrate oxide di-electric constant.

effort to bring the conducting material to equilibrium. Thus, ballistic transport in a material is determined by how ballistically conductive that material is. Ballistic conduction differs from superconductivity due to the absence of the Meissner effect in the material. A ballistic conductor would stop conducting if the driving force is turned off, whereas in a superconductor current would continue to flow after the driving supply is disconnected.

Ballistic conduction is typically observed in quasi-1D structures, such as carbon nanotubes or silicon nanowires, because of extreme size quantization effects in these materials. Ballistic conduction is not limited to electrons (or holes) but can also apply to phonons. It is theoretically possible for ballistic conduction to be extended to other quasi-particles, but this has not been experimentally verified.

Fig. 2.12 shows simplified energy band diagram, Fig. 2.13 shows simplified equivalent circuit for predicting current in CNTFET and Fig. 2.14 shows potential in a wrap around CNTFET.

In general, carriers will exhibit ballistic conduction when the length of the active

part of the device (i.e., a channel in a MOSFET) is less than the mean scattering length for the carrier.

2.8 Discussion

Chapter 2 provided the technical background necessary to understand CNTFET device operation. Besides these, our proposed new model is introduced here.

Chapter 3

Capacitances of Wrap Around CNTFET

Wrap around gate carbon nanotube field effect transistor (CNTFET) has the advantage of more accurately controlled channel than top gated CNTFET. 3-D simulation is performed using Finite Element Method (FEM) to model wrap around CNTFET with multi-CNT channel. Analytical expressions to model various capacitances of the same device are also derived from capacitances for 1-D FET with multiple cylindrical conducting channels incorporating screening effect due to multiple CNT. Various capacitances thus obtained exhibit remarkable improvement over planar top gate device with multiple conducting channels. This is attributed to the charge enhancement and better charge confinement in the channel of the wrap around CNTFET with multi-CNT channel. Capacitances are also extracted from the proposed FEM model. The extracted capacitances are in excellent agreement with the capacitances obtained from the analytical model presented in this study.

3.1 Introduction

Top gate structure with high-k gate dielectric is a general structure for multiple conducting channel device. Carbon Nano Tube (CNT) transistors has been on active

research bench with extensive academic and technological interest in recent years. In the limit of ballistic or near-ballistic transport, the device current of 1-D device highly depends on the gate to channel capacitance (C_{gc}). The parallel conducting channels have screening/imaging effect on the actual potential profile in the gate region and therefore affect the capacitance. *Wang et al.* reported calculations of C_{gc} in CNT devices including screening effect using 2-D numerical modeling [30] ,[31]. Analytical models for performance parameters and high frequency electrical properties of CNT devices can be found in the literature [32], [33]. In addition to C_{gc}, the device speed also depends upon parasitic gate capacitance including outer fringe capacitance (C_{of}) and gate to gate (source/drain) coupling capacitance (C_{gtg}). Hence it is important to model the various component of total gate capacitance in order to evaluate and predict circuit performance of the device (on-current, speed, power etc.). *Deng and others* presented compact SPICE models for the channel region [34] of top gate CNTFET as well as full device [35] including nonidealities and discussed applications and circuit performance of the device. While, *Wei and others* discussed the impact of parasitic gate capacitance and screening effect and presented modeling and performance comparison of 1-D and 2-D top gate CNTFET [36],[37]. Now, wrap around gate CNTFET has gate around it except at the bottom. Hence it is expected to exhibit enhanced capacitance and drive current over top gate CNTFET for more controlled channel. However, the advantage and better performance of wrap around CNTFET remains to be investigated through theoretical as well as experimental studies. Experimental investigation is yet to overcome the technological limitations of poor control over CNT chirality and position. Therefore, theoretical simulation and modeling can be significant and useful work to benchmark CNTFET performance. Because of ultra small size and carrier confinement in the channel of wrap around CNTFET, 3-D simulation and modeling is necessary for accurate

estimation of capacitance, drive current and other electrical properties. To the best of our knowledge, 3-D simulation and modeling of multiple channel CNTFET is yet to appear in the literature. In this study, we performed 3-D simulation of wrap around CNTFET with multiple CNT channel using Finite Element Method (FEM) to develop an accurate model of the device. Modeling of various capacitances of interest are also carried out by extending the expressions of these capacitances for planar top gate device [38] to the structure used in this study.

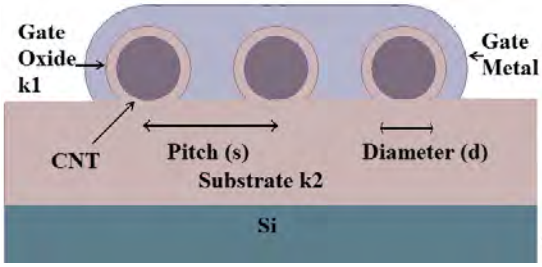

Figure 3.1: Schematic cross sectional view of wrap around gate multi-CNT channel FET.

3.2 Device Structure

In this work, we consider a wrap around gate structure with multiple cylindrical conducting channel. The device is constructed with high-k gate dielectric(k_1) and a substrate with a different dielectric constant (k_2). The whole device is mounted on Si as illustrated in Figure 3.1. Diameter of the cylinder is d and distance between the centers of two adjacent parallel CNTs is denoted by s. Figure 3.1 illustrates cross sectional view of the wrap around gate CNTFET with multi-CNT which is used to develop 3-D FEM model and analytical modeling of various capacitances of interest.

3.3 Capacitance Modeling

Various capacitances are associated with the structure of the device described above. The important capacitances to be modeled are gate to channel capacitance (C_{gc}), outer fringe capacitance (C_{of}) and gate to gate or gate to source/drain coupling capacitance(C_{gtg}). An associate phenomenon of the structure is screening effect of the neighboring conductors. This effect has been incorporated in modeling the capacitance. It is to be noted that analytical modeling of the capacitances and the conceptual illustrations in the following sub-sections are based on the expressions/ illustrations reported earlier [38] for top gate 1-D FET with multiple cylindrical conducting channels.

3.3.1 Gate to Channel Capacitance

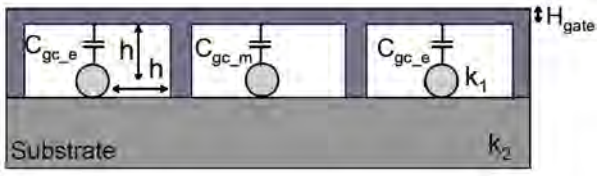

Figure 3.2: Approximate cross sectional view of the CNTFET with gate to channel capacitance for end CNT channel ($C_{gc,e}$) and middle CNT channel ($C_{gc,m}$).

Gate to channel capacitance (C_{gc}) plays a significant role in determining the drive current of the device. C_{gc} is strongly attenuated by the image charge across the dielectric boundary and screening of neighboring channels, specially for closely spaced channels which provide large drive current per unit width. These effects must be accounted for in modeling C_{gc}. Different components used to derive an analytical model of C_{gc} is illustrated in an approximate cross-sectional view of the multi-CNT channel transistor shown in Fig. 3.2. Here, shape of the gate dielectric around the CNT channel is approximated to be rectangular in order to simplify the analysis.

For the objects at the ends of an array, the screening objects are only at one side, so the capacitance is $C_{gc,e}$. For the objects around the middle of an array, because the geometry is symmetric around the object, so the capacitance between the electrode and the object in the middle is $C_{gc,m}$. Under applied gate voltage, charge distribution of CNT changes as illustrated in Fig. 3.3. Applying approximate boundary conditions, image charge can be determined.

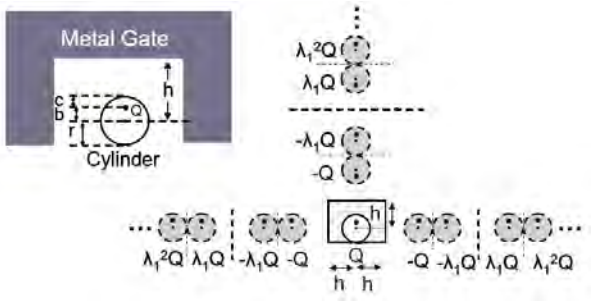

Figure 3.3: Conceptual representation of wrap around gate CNTFET illustrating image charge distribution of CNT channel. Here, $b = h - \sqrt{h^2 - r^2}$ and $c = r - h + \sqrt{h^2 - r^2}$. Due to metal gate mirroring, three $-Q$ image charge is formed in three sides. More images due to air and more metal layer.

Now, we consider the effects of the adjacent parallel cylinders on C_{gc} for a more general gate structure and derive the expressions for $C_{gc,e}$ and $C_{gc,m}$. Consider a gate with two conducting channels, cylinder A and cylinder B, in parallel as shown in Fig. 3.4. Only two image line charges with each real line charge Q is considered: the image line charge Q due to metal gate mirroring, and the image line charge λ_1Q due to $k_1 \neq k_2$ (Fig. 3.4). Due to the screening effect, in addition to the potential difference caused by the isolated cylinder A itself, there are additional potential drops between cylinder A and the real and image line charges by cylinder B. The additional potential difference caused by the line charge Q_B and the image line charge $\lambda_1 Q_B$ is given by, $V_{adj,1}$ and $V_{adj,2}$. Where $V_{adj,1}$ is the additional potential difference that is caused by line charge Q_B and $V_{adj,2}$ is the additional potential difference that is

caused by image line charge $\lambda_1 Q_B$.

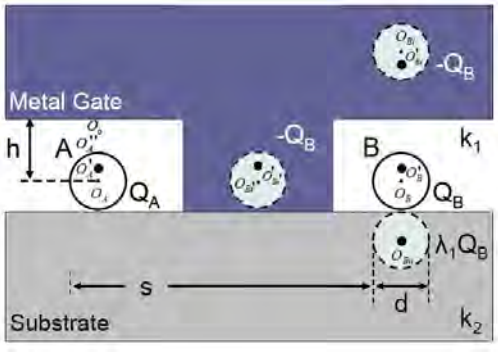

Figure 3.4: Schematic illustration of screening effect due to parallel conducting channel in wrap around CNTFET with multi-CNT channel.

When the same potential is applied to the two parallel cylinders, the charge distribution profiles in the regions around cylinder A and cylinder B should be identical. The equivalent series capacitance due to the adjacent channel screening is then given by,

$$C_{gc,sr} = \frac{Q_B}{V_{adj,1} + V_{adj,2}} \tag{3.3.1}$$

Since the electric field is well confined within the gate dielectric for the typical gate structure, we assume the cylinders which are more than s distance apart have a minor effect on each other, i.e. the gate to channel capacitance does not depend on the number of the cylinders in the array. Equation for different capacitance is found from [38],

$$C_{gc,e} = \frac{C_{gc,inf} \cdot C_{gc,sr}}{C_{gc,inf} + C_{gc,sr}} \tag{3.3.2}$$

$$C_{gc,m} = 2C_{gc,e} - C_{gc,inf} \tag{3.3.3}$$

Due to the presence of another Q_B charge and calculating the distances, the modified equation for wrap around gate can be obtained as,

$$C_{gc,sr} =$$

$$\frac{4\pi k_1 \epsilon}{ln(\frac{s^2+2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2+2(h-r)\cdot[h-\sqrt{h^2-r^2}]}) + ln(\frac{s^2+[r-h+\sqrt{h^2-r^2}]^2}{4s^2+[r-h+\sqrt{h^2-r^2}]^2}) + Z_1} \tag{3.3.4}$$

Where

$$Z_1 = \lambda_1 \cdot ln(\frac{(h+d)^2+s^2}{9r^2+s^2}) \cdot tanh(\frac{h+r}{s-d}) \tag{3.3.5}$$

$$C_{gc,inf} = \frac{2\pi k_1 \epsilon}{cosh^{-1}(\frac{2h}{d}) + \frac{1}{3}\lambda_1 \cdot ln(\frac{2h+2d}{3d})} \tag{3.3.6}$$

where from [38],

$$\lambda_1 = \frac{k_1 - k_2}{k_1 + k_2} \tag{3.3.7}$$

$C_{gc,e}$ is the unit capacitance of the gate to the cylinders at the two ends and $C_{gc,m}$ is the unit capacitance of the gate to the cylinders in the middle.

3.3.2 Outer fringing capacitance

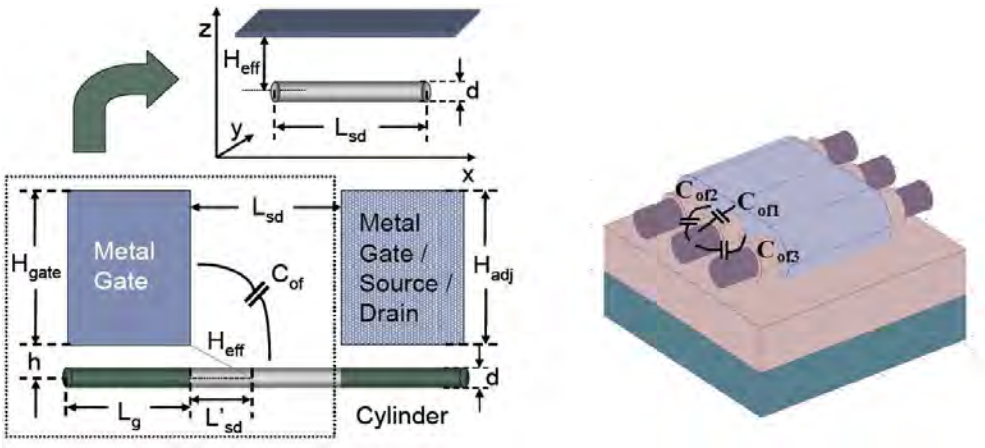

Figure 3.5: Schematic presentation of fringing capacitance and associated device parameters of the CNTFET.

Outer fringing capacitance (C_{of}) is an important parasitic gate capacitance which is strong function of device geometry. To evaluate the device speed accurately, it is

necessary to include the parasitic gate capacitance, e.g. the outer-fringe capacitance (C_{of}) and the gate to gate (or gate to source/drain) coupling capacitance (C_{gtg}). Since the channel region is screened by the conducting cylinders, the inner fringe capacitance is ignored in Fig. 3.5. For 1-D FET, the coupling capacitance between the gate and the source/drain due to the sidewall fringing field is more significant than the coupling capacitance due to the normal fringing field, because of the small diameter of 1-D channel compared to the gate width. For 1-D FET with L_{sd} shorter than the gate interconnect length in the gate width direction, which is well satisfied for typical device design. C_{of} is almost independent of the gate height and gate width. Applying same approach as C_{gc}, we find $C_{of,inf}$, the capacitance between the gate and the isolated S/D cylinder. It is convenient to calculate the capacitance if the cylinder is parallel with the sidewall of the gate, as shown in the inset in Fig. 3.5. For a 2-D structure, it is possible to convert an elliptical system to an equivalent parallel system using conformal mapping. We define an equivalent distance H_{eff} between the S/D cylinder and the sidewall of the gate. With more than one channel per gate, there will be additional potential drop between the two electrodes of the capacitor C_{of} caused by the adjacent cylinders. So the equivalent series capacitance for wrap around CNTFET due to adjacent cylinder screening ($C_{of,sr}$) should be included.

It is reasonable to group the fringe capacitances into two components: (a) the capacitance between gate and S/D at the ends ($C_{of,e}$) and (b) the capacitance between gate and S/D in between ($C_{of,m}$). The modified equation for wrap around gate can be obtained as,

$$C_{of,e} = \frac{\pi k_2 \epsilon_o L_{sd}}{ln(\frac{\sqrt{(2h)^2+(0.56L_{sd})^2+s^2}}{s}) + ln(\frac{\sqrt{(\frac{s}{2})^2}}{s}) + Z_2} \tag{3.3.8}$$

where

$$Z_2 = \eta_1 \cdot \frac{1}{3} cosh^{-1}(\frac{\sqrt{(2h)^2 + (0.56L_{sd})^2}}{d}) \tag{3.3.9}$$

η_1 is empirically represented as [38],

$$\eta_1 = exp(\frac{\sqrt{N^2 - 2N} + N - 2}{\tau_1 N}), N \geq 2 \tag{3.3.10}$$

Where N is the number of cylinders per gate in the channel region. The outer-channel region is a more open structure than the inner channel region, thus we can use the simplified equation for $N \geq 2$,

$$C_{of,m} = \frac{2\alpha}{\eta_1} \cdot C_{of,e} + (1 - \frac{2\alpha}{\eta_1}) \cdot \frac{\pi k_2 \epsilon_o L_{sd}}{\frac{1}{3} cosh^{-1}(\frac{\sqrt{(2h)^2 + (0.56L_{sd})^2}}{d})} \tag{3.3.11}$$

$$\alpha = exp(\frac{N - 3}{\tau_2 N}), N \geq 3 \tag{3.3.12}$$

Both η_1 and α are functions of N. η_1=1 for $N = 2$ and α=1 for $N = 3$. τ_1 and τ_2 are fitting parameters which describes how fast the electric flux of the adjacent cylinders decreases with increasing distance. τ_1 and τ_2 are empirically set as 2.5 and 2, respectively.

3.3.3 Gate to drain/source capacitance

The gate to gate capacitance (C_{gtg}) is another major component of the gate capacitance. We separate C_{gtg} into two components : the gate to gate fringe capacitance per unit length ($C_{gtg,fr}$) and the gate to gate plate capacitance per unit length ($C_{gtg,nr}$). $C_{gtg,nr}$ is due to the normal electrical filed between the two parallel plates (wrap around gate). These are conceptually illustrated in Fig. 3.6.

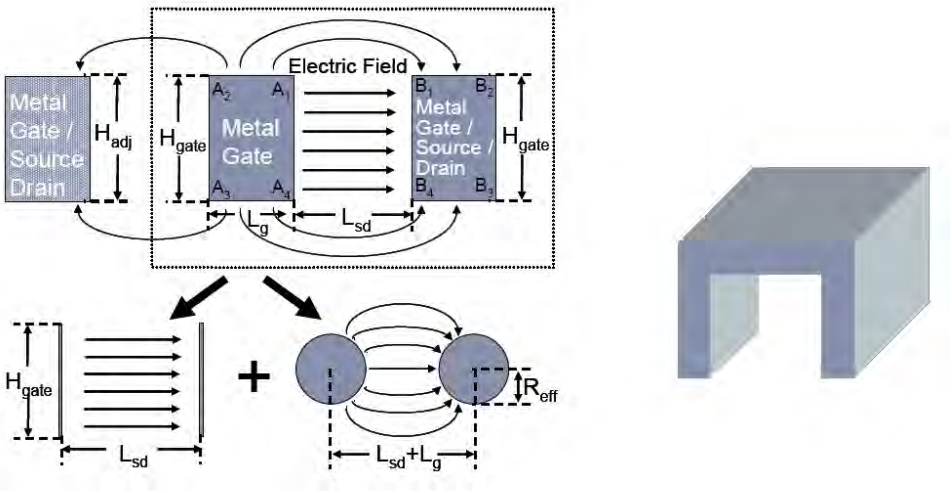

Figure 3.6: Conceptual illustration of gate to drain/source capacitance of CNTFET.

The total gate to gate capacitance per unit length is the summation of $C_{gtg,fr}$ and $C_{gtg,nr}$. Due to the presence of gate in three sides of CNT, the modified equation for wrap around gate can be obtained as,

$$C_{gtg} = 3\frac{k_2\epsilon_o H_{gate}}{L_{sd}} + \alpha_{gtg,sr} \cdot \frac{\pi k_2 \epsilon_o}{ln(\frac{2\pi(L_{sd}+L_g)}{2L_g+\tau_{bk}(H_{gate}+h+r)})} \tag{3.3.13}$$

Here, H_{gate}, L_{sd}, L_g are some physical parameters as shown in Fig. 3.6.

3.4 FEM Modeling: 3D Simulation

A 3-D device model of CNTFET with multi-CNT channel is created using COMSOL as presented in Fig. 3.7. This device is used for 3-D simulation using Finite Element Method (FEM) to develop FEM model of the device. PDE mode of COMSOL 3.4 is used to solve Poisson's equation:

$$\nabla^2 V = -\frac{\rho}{\epsilon} \tag{3.4.1}$$

ϵ is differnt for CNT, oxide and gate region.

Voltage variations in the CNTFET having $25nm$ and $15nm$ pitch are presented in Fig. 3.8 and Fig. 3.9, respectively. These reveal definite impact of wrap around gate and multi-CNT on voltage. Identical variation in current density (not shown to avoid redundancy) is also observed. Charge density can be found from current density variation. Since capacitance is the ratio of charge and voltage, average voltage can be extracted from Fig. 3.8 or Fig. 3.9. Capacitance thus obtained through this 3-D simulation required to be compared with those obtained from analytical model to validate the proposed FEM model. An attractive feature of FEM is its ability to handle complicated geometries (and boundaries) with relative ease. There are other methods for solving numerical problems. Among them, Finite Difference Method (FDM) is widely used. But FDM is restricted to handle rectangular shapes in its basic form. So, FEM is used to handle complicated structure in this work.

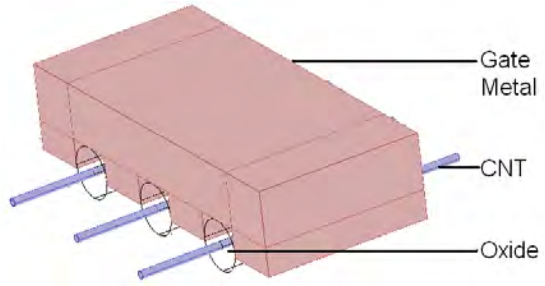

Figure 3.7: Model of CNTFET with multi-CNT channel created by COMSOL and used in 3D simulation.

3.5 Results and Discussion

Table 3.1: Parameters used in the simulation

PARAMETER	s	T_{ox}	k_1	k_2	L_{sd}
VALUE	$20nm$	$4nm$	$16\epsilon_o$	$4\epsilon_o$	$16nm$
PARAMETER	H_{gate}	L_g	a	n_1	n_2
VALUE	$12nm$	$32nm$	$0.2495nm$	19	0

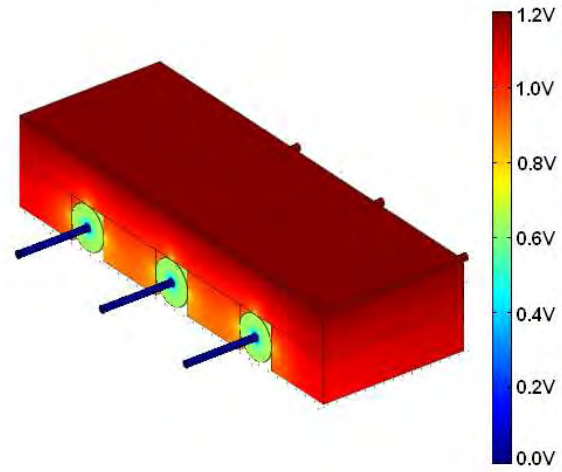

Figure 3.8: Variation of voltage in the wrap around gate CNTFET with multi-CNT having 25nm pitch as obtained from 3-D simulation using Finite Element Method.

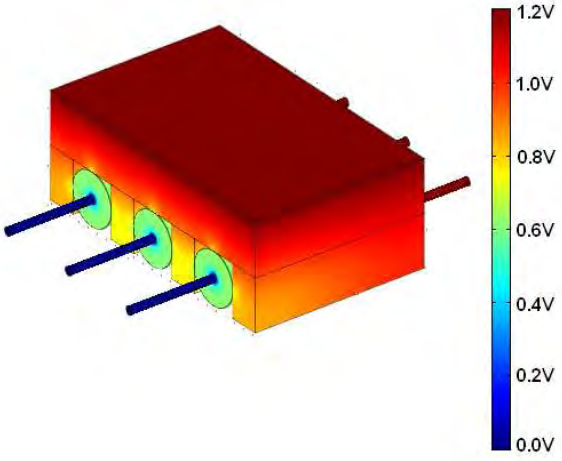

Figure 3.9: 3-D simulation result of voltage variation in the CNTFET having 15nm pitch using Finite Element Method.

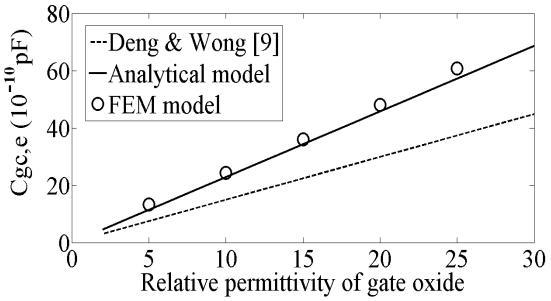

Figure 3.10: Gate to channel capacitance of end CNT for different gate dielectric. Proposed FEM model is in excellent agreement with analytical model.

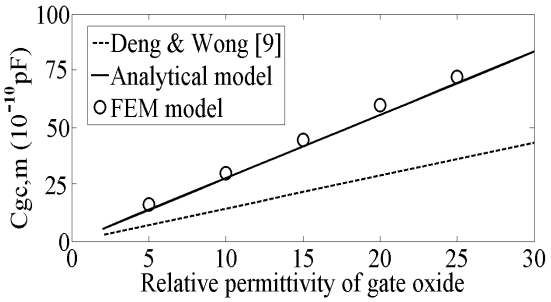

Figure 3.11: Gate to channel capacitance of mid CNT for different gate dielectric. Proposed FEM model is in excellent agreement with analytical model.

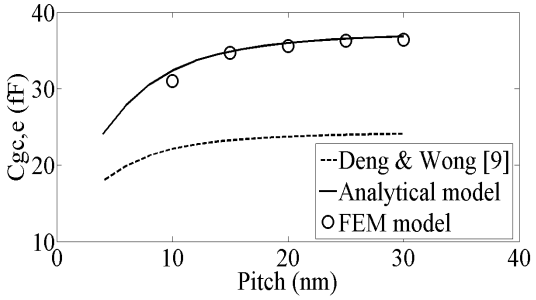

Figure 3.12: Gate to channel capacitance of end CNT as a function of pitch. Improvement over top gate device and agreement between FEM model and analytical model is apparent.

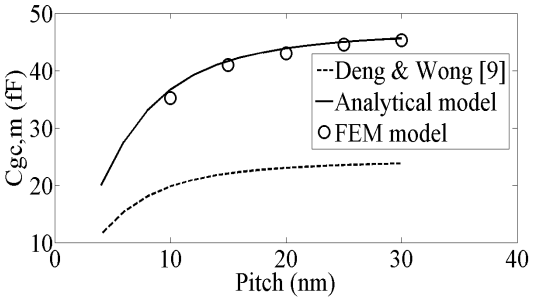

Figure 3.13: Gate to channel capacitance of mid CNT as a function of pitch. Improvement over top gate device and agreement between FEM model and analytical model is apparent.

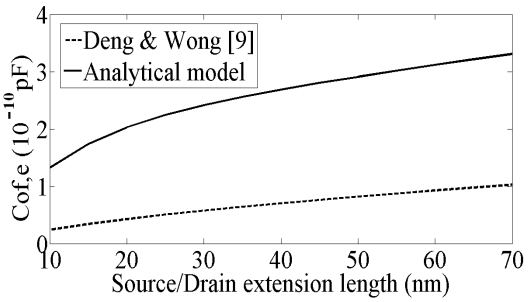

Figure 3.14: Variation of gate outer fringe capacitance of end CNT with source/drain extension length.

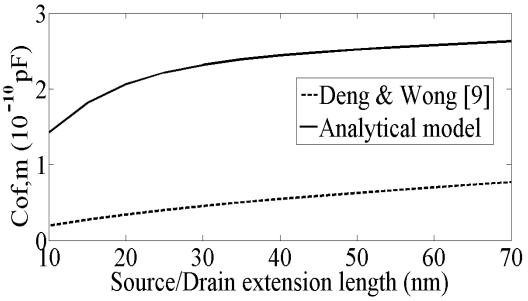

Figure 3.15: Variation of gate outer fringe capacitance of mid CNT with source/drain extension length.

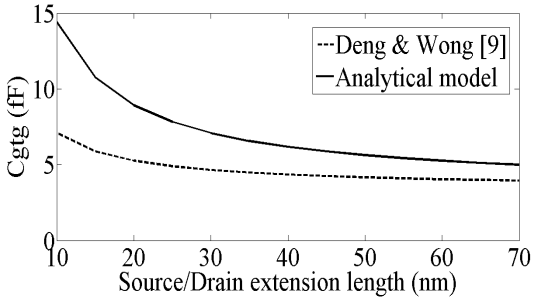

Figure 3.16: Variation of gate to source/drain capacitance with source/drain extension length.

Various parameters used in the calculation are given in Table 3.1. n_1 and n_2 (shown in the table) are used to calculate the diameter of the carbon nanotube [34]. Using the analytical expressions derived above respective capacitances are calculated. Variation of gate to channel capacitance of end CNT and mid CNT with different gate oxide material is shown in Fig. 3.10 and Fig. 3.11, respectively. While, variation of gate to channel capacitance of end CNT and mid CNT as a function of pitch (distance between two CNT channel) are shown in Fig. 3.12 and Fig. 3.13, respectively. Capacitances extracted from the proposed FEM model are also presented in Fig. 3.10 through Fig. 3.13. These figures reveal remarkable improvement of capacitances over planar top gate multi-channel CNTFET [38] and excellent agreement between the proposed 3-D FEM model and the analytical models of various capacitances of the wrap around gate CNTFET with multi CNT channels.

Effect of source/drain extension length on gate outer fringe capacitance of end CNT and mid CNT are shown in Fig. 3.14 and Fig. 3.15, respectively. While, variation of gate to gate (source/drain) capacitance with source/drain extension length is shown in Fig. 3.16. Results for planar top gate device [38] are also exhibited in Fig. 3.14 through Fig. 3.16 for comparison. In all respects wrap around gate CNTFET with multi-CNT channel is found to provide enhanced capacitances than planar top gate

CNTFET.

3.6 Conclusion

Wrap around gate CNTFET with multiple CNT channel is theoretically investigated and found to have better electrical characteristics than top gated device. 3-D simulation is performed using Finite Element Method to develop an accurate 3-D model of the device. Remarkable improvement in gate capacitance is obtained with respect to planar top gate identical device. Analytical models for various capacitances are also derived from the expressions for top gate multiple conducting channel CNTFET. The capacitances extracted from the proposed FEM model exhibited excellent agreement with the analytical models and hence validated the proposed model. Wrap around gate CNTFET with enhanced gate capacitance strengthens its potentiality for future generation high speed device.

Chapter 4

Temperature Effects

Temperature distribution of wrap around CNTFET with multi-cnt is presented in this paper. For predicting the device characteristics, temperature modeling is necessary. Temperature distribution is changed due to multi-cnt as voltage of adjacent cnt affects temperature of mid cnt. Again it is also changed by temperature dependent thermal conductivity of single walled carbon nano tube (SWCNT). Current flow is changed both due to multi-cnt wrap around structure and due to the temperature change. So, temperature has a great impact on current modeling and thus on device characteristics. All these issues are considered in this paper using finite element method.

4.1 Introduction

For a device with multiple conducting channels, a planar gate structure with high-k gate dielectric material is a general structure. But wrap around structure has several advantages regarding fabrication process and for better channel control. Though there are some simple analytical model ([32], [33]), but there have been no analytical models available for wrap around CNTFET with multi-CNT. Various capacitance modeling of wrap around CNTFET with multi-CNT is presented in [39]. Besides

these, temperature distribution profile should also be accounted as in the limit of ballistic or near-ballistic transport, the drive current of device highly depends on the temperature.

Top gated CNTFET modeling was previously performed ([34], [35]). Even 2D model was performed([36], [37]). But none has considered wrap around gate modeling where three dimensional effect is present. Generally SWCNT is used in these devices. SWCNTs have attracted much interest in the scientific society due to their excellent electrical, thermal, and mechanical properties. Unlike aluminum and copper, the thermal conductivity of SWCNT exhibits an extremely nonlinear behavior over the temperature zone of interest. In [40], temperature of top gated CNTFET with single cnt was measured using 1-D heat conduction equation. Again, in [41], temperature of metallic SWCNT was measured using analytical equation. But temperature distribution is changed for multi-cnt as voltage of adjacent cnt affects temperature of mid cnt as well as for temperature dependent thermal conductivity of SWCNT. Drain to source current is changed both due to multi-cnt wrap around structure and due to the temperature change. These important issues are still missing in literature. All these issues are considered in this paper. Proposed model provides more insight in temperature distribution than [40], where these issues were not taken into account and it was also for top gated structure. Again, COMSOL 3D simulation is performed by Finite Element Method (FEM).

4.2 Theory

Structure of wrap around gate multi-cnt CNTFET and its capacitances is presented in [39]. In this work, we consider a wrap around gate structure with multiple cylindrical conducting channels and high-k gate dielectric material on a substrate with a different

dielectric constant as illustrated in Fig. 4.1. The diameter of the cylinder is d. The normal distance between the gate and the cylinder center is denoted by h, and the distance between the centers of the two adjacent parallel conductors is denoted by s.

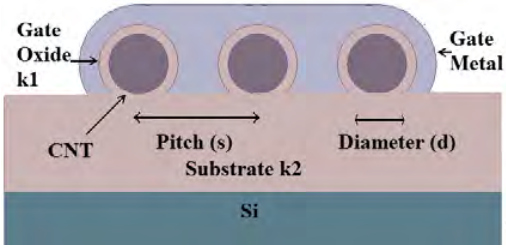

Figure 4.1: Cross sectional view of CNTFET with multi cnt

Modifying the expression used in previous model ([40], [41]) of Joule-heating equation with a temperature-dependent thermal conductivity along the length of the SWCNT:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k(T, L)\nabla T) - \frac{p}{A} + \frac{g(T - T_0)}{A} = 0 \tag{4.2.1}$$

where ρ is the density and C_p is the specific heat capacity. $A = \pi db$ is the cross-sectional area; d and b are the diameter and the tube wall thickness of the SWCNT respectively. g is the CNT-substrate thermal coupling parameter. p is the per-unit-length joule heating rate and it is a key parameter that relates the CNTFET current to the phonon scattering. It is found from the voltage and contributed current from all subbands of substates. Temperature-dependent thermal conductivity (k) depends both on temperature and length of cnt. T_0 is the initial room temperature. From this equation, temperature distribution in carbon nano tube is found.

For gate oxide and for metal contact, Joule-heating equation used in comsol software:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-k \nabla T) = Q \tag{4.2.2}$$

Here, Q is the heat source term and it is equal to zero because cnt is the only heat source here that conducts current. From this equation, temperature in the gate oxide and gate metal is found.

4.3 Finite Element Method: 3D Simulation

We have used finite element method for simulation of CNTFET. We have used COMSOL to create a 3D device model of CNTFET with multi-CNT (Fig. 4.2). Partial differential equation is numerically solved in this software. After simulating by finite element method, different types of temperature distribution is shown to clearly visualize three dimensional temperature distribution.

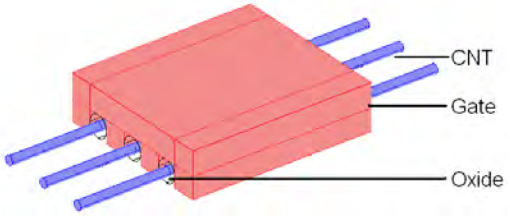

Figure 4.2: COMSOL Model of CNTFET with multi cnt

4.4 Results and Discussion

Parameters used here are shown in Table 4.1. Boundary temperature distribution of CNTFET with multi cnt is shown in Fig. 4.3. Slice temperature distribution is shown in Fig. 4.4. Temperature distribution along CNT length is given in Fig. 4.5 and temperature distribution from channel to top of gate is shown in Fig. 4.6. This

Table 4.1: Parameters used in the model

TERM	a	s	g	$C_p(cnt)$
VALUE	$0.2495nm$	$6.4nm$	$0.18W/m-K$	$4186J/kg-K$
TERM	L_d	L_g	L_s	$\rho(cnt)$
VALUE	$16nm$	$32nm$	$16nm$	$1350kg/m^3$

temperature variation will affect the current flow in the cnt as transmission co-efficient will be changed.

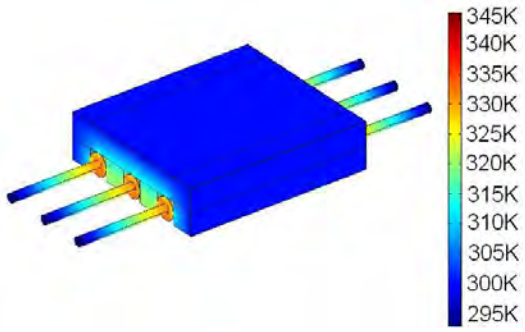

Figure 4.3: Boundary temperature distribution of CNTFET with multi cnt

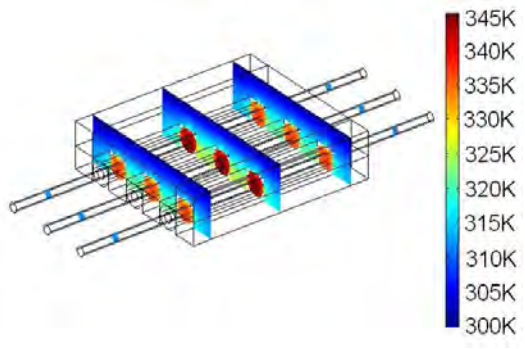

Figure 4.4: Slice temperature distribution of CNTFET with multi cnt

Here, finite element method (FEM) is performed by using comsol. The most attractive feature of the FEM is its ability to handle complicated geometries (and boundaries) with relative ease. There are some other methods for solving numerical problem. Among them, finite difference method (FDM) is widely used but in its basic

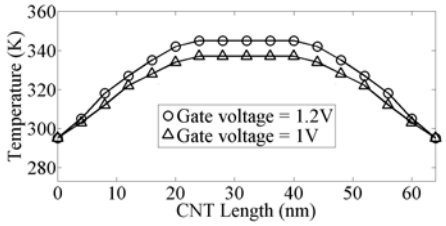

Figure 4.5: Temperature distribution along CNT length

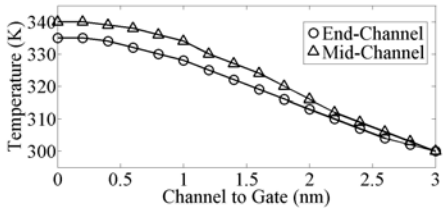

Figure 4.6: Temperature distribution from channel to top of gate for gate voltage=1.2V

form it is restricted to handle rectangular shapes.

Maximum temperature is found at the channel region as it is less doped and has high resistance. Due to this resistance, power is lost as form of heat. Again temperature in drain and source is less than channel region as they are highly doped and have less resistances (Fig. 4.5). As a result power (voltage multiplied by current) is high at drain and so do energy. This energy contributes as a heat source. Gate metal having least resistance has the lowest temperature (Fig. 4.6) as no current is present here and it can not be treated as a heat source.

4.5 Conclusion

Nonlinear temperature distribution of CNTFET with wrap around structure is presented in this paper. Temperature distribution has nonlinearity for multi-cnt as voltage of adjacent cnt affects temperature of mid cnt and also due to temperature dependent thermal conductivity of SWCNT. Highest temperature is found in

the mid of channel region. Temperature decreases both along the cnt and along the channel-oxide-gate metal region from the maximum temperature of mid channel region. Temperature has a great impact on current modeling. Thus this paper can be helpful for accurate modeling of wrap around CNTFET.

Chapter 5

Conclusions and Suggestions

5.1 Conclusions

Wrap around CNTFET has gate around it except the bottom portion and it is easier to fabricate. Wrap around model has several benefits than top-gated model as in the previous model, channel is more accurately controlled. Multiple CNT under a single gate contribute to better current conduction.

For predicting the device speed, capacitance modeling is necessary. Along with gate to channel capacitance, there are fringing capacitance as well. Again screening effect is present due to multiple CNT. All these capacitance have been modeled. Due to lack of experimental data of our proposed model, finite element method (FEM) model is presented to validate our proposed analytical model. 3D structure is created using comsol software that can work on the principle of finite element method. Analytical model and FEM model are in excellent agreement that validate our model. Our model is also compared with previous top gated structure and shows improved result.

Ballistic transport of charge is present in CNT as there are various sub-bands with different number of states and this contributes to current. Self-heating effect can deteriorate device performance like I-V characteristics than expected simulated

result. Non-uniform temperature distribution performed by finite element method is presented here. Temperature in different region of CNT channel as well as drain and source extension region are presented in this paper that can be helpful for predicting the actual device characteristics.

5.2 Future Works and Suggestions

Due to time constraint and opportunity, it is explicitly assumed that wrap around gate can be taken as a tri-gate for capacitance modeling. Moreover, effects that may be dominating for very small CNT length are not discussed here. Thus future work can be:

(i)Semi-circular structure may be included in future work where polar form of equations should be used.

(ii)Quantum mechanical and short channel effect for CNT should be explored and effects on CNTFET current, temperature and capacitances can also be included in later work.

I hope, these issues will be found in near future.

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Appendix

Code for gate to channel capacitance variation with gate oxide material :

```
clc
clf
clear all

a=0.2495e-9;
s=20e-9;
pi=3.1416;
h=6.63e-14;
epsilon=8.85e-12;
Tox=4e-9;
n1=19;
n2=0;
d=a*sqrt(n1^2+n1*n2+n2^2)/pi;
r=d/2;
h=Tox+r;
k_1=(2:2:30).*epsilon;%8.617e-5;
k_2=4*epsilon;%8.617e-5;

lambda_1=(k_1-k_2)/(k_1+k_2);
C_gc_inf=(2*pi*k_1*epsilon)/(acosh(2*h/d)+(1/3)*lambda_1*log((2*h+2*d)/(3*d)));
Z_1=lambda_1*log(((h+d)^2+s^2)/(9*r^2+s^2))*tanh((h+r)/(s-d));
Z_2=log((s^2+(r-h+sqrt(h^2-r^2))^2)/(4*s^2+(r-h+sqrt(h^2-r^2))^2));
Z_3=log((s^2+2*(h-r)*(h+ sqrt(h^2-r^2)))/(s^2+2*(h-r)*(h-sqrt(h^2-r^2))));
C_gc_sr=(4*pi*k_1*epsilon)/(Z_3+Z_2+Z_1);
```

```
C_gc_e=(C_gc_inf.* C_gc_sr)./(C_gc_inf+C_gc_sr);
C_gc_m=2*C_gc_e-C_gc_inf;

C_gc_infw=(2*pi*k_1*epsilon)/(acosh(2*h/d)+lambda_1*log((2*h+2*d)/(3*d)));
Z_1w=lambda_1*log(((h+d)^2+s^2)/(9*r^2+s^2))*tanh((h+r)/(s-d));
Z_3w=log((s^2+2*(h-r)*(h+ sqrt(h^2-r^2)))/(s^2+2*(h-r)*(h-sqrt(h^2-r^2))));
C_gc_srw=(4*pi*k_1*epsilon)/(Z_3w+Z_1w);

C_gc_ew=(C_gc_infw.* C_gc_srw)./(C_gc_infw+C_gc_srw);
C_gc_mw=2*C_gc_ew-C_gc_infw;

figure (1)
plot(k_1/epsilon,C_gc_ew*10^22,'--','LineWidth',2,'MarkerEdgeColor','k')
xlabel('Relative permittivity of gate oxide');
ylabel('Cgc,e (10 -10 pF)');
hold on
plot(k_1/epsilon,C_gc_e*10^22,'-','LineWidth',2,'MarkerEdgeColor','k')
gnew=5:5:25;
extra11=[1.33e-21 2.44e-21 3.6e-21 4.8e-21 6.07e-21];%found from 3D simulation
plot(gnew,extra11*10^22,'o','LineWidth',2,'MarkerEdgeColor','k')
hold off
figure (2)
plot(k_1/epsilon,C_gc_mw*10^22,'--','LineWidth',2,'MarkerEdgeColor','k')
xlabel('Relative permittivity of gate oxide');
ylabel('Cgc,m (10 -10 pF)');
hold on
```

```
plot(k_1/epsilon,C_gc_m*10^22,'-','LineWidth',2,'MarkerEdgeColor','k')
gnew=5:5:25;
extra12=[1.62e-21 3e-21 4.47e-21 6.0e-21 7.23e-21]; %found from 3D simulation
plot(gnew,extra12*10^22,'o','LineWidth',2,'MarkerEdgeColor','k')
hold off
```

Code for gate to channel capacitance variation with pitch :

```
clc
clf
clear all

a=0.2495e-9;
s=(4:2:30)*1e-9;
pi=3.1416;
h=6.63e-14;
epsilon=8.85e-12;
Tox=4e-9;
n1=19;
n2=0;
d=a*sqrt(n1^2+n1*n2+n2^2)/pi;
r=d/2;
h=Tox+r;
k_1=16*8.617e-5;
k_2=4*8.617e-5;

lambda_1=(k_1-k_2)/(k_1+k_2);
C_gc_inf=(2*pi*k_1*epsilon)/(acosh(2*h/d)+(1/3)*lambda_1*log((2*h+2*d)/(3*d)));
Z_1=lambda_1*log(((h+d)^2+s.^2)./(9*r^2+s.^2)).*tanh((h+r)./(s-d));
```

```
Z_2=log((s.^2+(r-h+sqrt(h^2-r^2))^2)./(4*s.^2+(r-h+sqrt(h^2-r^2))^2));
Z_3=log((s.^2+2*(h-r).*(h+ sqrt(h^2-r^2))./(s.^2+2*(h-r)*(h-sqrt(h^2-r^2))));
C_gc_sr=(4*pi*k_1*epsilon)./(Z_3+Z_2+Z_1);

C_gc_e=(C_gc_inf.* C_gc_sr)./(C_gc_inf+C_gc_sr);
C_gc_m=2*C_gc_e-C_gc_inf;



C_gc_infw=(2*pi*k_1*epsilon)/(acosh(2*h/d)+lambda_1*log((2*h+2*d)/(3*d)));
Z_1w=lambda_1*log(((h+d)^2+s.^2)./(9*r^2+s.^2)).*tanh((h+r)./(s-d));
Z_3w=log((s.^2+2*(h-r).*(h+ sqrt(h^2-r^2))./(s.^2+2*(h-r)*(h-sqrt(h^2-r^2))));
C_gc_srw=(4*pi*k_1*epsilon)./(Z_3w+Z_1w);

C_gc_ew=(C_gc_infw.* C_gc_srw)./(C_gc_infw+C_gc_srw);
C_gc_mw=2*C_gc_ew-C_gc_infw;

figure (1)
plot(s*10^9,C_gc_ew*10^15,'--','LineWidth',2,'MarkerEdgeColor','k')
xlabel('Pitch (nm)');
ylabel('Gate to channel capacitance of end CNT (fF)');
hold on
plot(s*10^9,C_gc_e*10^15,'-','LineWidth',2,'MarkerEdgeColor','k')
snew=10e-9:5e-9:30e-9;
extra=[3.1e-14 3.47e-14 3.56e-14 3.63e-14 3.64e-14]; %found from 3D simulation
plot(snew*10^9,extra*10^15,'o','LineWidth',2,'MarkerEdgeColor','k')
hold off
figure (2)
```

```
plot(s*10^9,C_gc_mw*10^15,'--','LineWidth',2,'MarkerEdgeColor','k')
xlabel('Pitch (nm)');
ylabel('Gate to channel capacitance of mid CNT (fF)');
hold on
plot(s*10^9,C_gc_m*10^15,'-','LineWidth',2,'MarkerEdgeColor','k')
snew=10e-9:5e-9:30e-9;
extra=[3.52e-14 4.1e-14 4.3e-14 4.45e-14 4.53e-14]; %found from 3D simulation
plot(snew*10^9,extra*10^15,'o','LineWidth',2,'MarkerEdgeColor','k')
hold off
```

Code for gate outer fringe capacitance and gate to drain/source capacitance :

```
clc
clf
clear all

a=0.2495e-9;
s=20e-9;
pi=3.1416;
h=6.63e-14;
epsilon=8.85e-12;
Tox=4e-9;
n1=19;
n2=0;
d=a*sqrt(n1^2+n1*n2+n2^2)/pi;
r=d/2;
h=Tox+r;
k_1=16*8.617e-5;
```

```
k_2=4*8.617e-5;

lambda_1=(k_1-k_2)/(k_1+k_2);
C_gc_inf=(2*pi*k_1*epsilon)/(acosh(2*h/d)+(1/3)*lambda_1*log((2*h+2*d)/(3*d)));
Z_1=lambda_1*log(((h+d)^2+s^2)/(9*r^2+s^2))*tanh((h+r)/(s-d));
Z_2=log((s^2+(r-h+sqrt(h^2-r^2))^2)/(4*s^2+(r-h+sqrt(h^2-r^2))^2));
Z_3=log((s^2+2*(h-r)*(h+ sqrt(h^2-r^2)))/(s^2+2*(h-r)*(h-sqrt(h^2-r^2))));
C_gc_sr=(4*pi*k_1*epsilon)/(Z_3+Z_2+Z_1);

C_gc_e=(C_gc_inf* C_gc_sr)/(C_gc_inf+C_gc_sr)
C_gc_m=2*C_gc_e-C_gc_inf

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
tau_1=2.5;
tau_2=2;
N=3;
L_sd=(10:5:70)*1e-9;
eta_1=exp((sqrt(N^2-2*N)+N-2)/(tau_1*N));
alpha=exp((N-3)/(tau_2*N));
Z_4=log((sqrt((2*h)^2+(0.56.*L_sd).^2+s^2))/s);
Z_5=log((sqrt(s/2))^2/s);
Z_6=eta_1*1/3*acosh(sqrt((2*h)^2+(0.56*L_sd).^2)/d);

C_of_e=(pi*k_2*epsilon.*L_sd)./(Z_4+Z_5+Z_6)
C_of_m=2*alpha/eta_1*C_of_e+(1-
2*alpha/eta_1)*pi*k_2*epsilon*L_sd./(1/3*acosh(sqrt((2*h)^2+(0.56.*L_sd).^2)/d))

Z_4w=log((sqrt((2*h)^2+(0.56.*L_sd).^2+s^2))/s);
```

```
Z_6w=eta_1*acosh(sqrt((2*h)^2+(0.56*L_sd).^2)/d);


C_of_ew=(pi*k_2*epsilon.*L_sd)./(Z_4w+Z_6w)

C_of_mw=2*alpha/eta_1*C_of_ew+(1-
2*alpha/eta_1)*pi*k_2*epsilon*L_sd./(acosh(sqrt((2*h)^2+(0.56.*L_sd).^2)/d))


figure (1)

plot(L_sd*10^9,C_of_ew*10^22,'--','LineWidth',2,'MarkerEdgeColor','k')

xlabel('Source/Drain extension length (nm)');

ylabel('Cof,e (10 -10 pF)');

hold on

plot(L_sd*10^9,C_of_e*10^22,'-','LineWidth',2,'MarkerEdgeColor','k')

hold off

figure (2)

plot(L_sd*10^9,C_of_mw*10^22,'--','LineWidth',2,'MarkerEdgeColor','k')

xlabel('Source/Drain extension length (nm)');

ylabel('Cof,m (10 -10 pF)');

hold on

plot(L_sd*10^9,C_of_m*10^22,'-','LineWidth',2,'MarkerEdgeColor','k')

hold off

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

alpha_gtg_sr=0.7;

H_gate=12e-9;

L_g=32e-9;

tau_bk=exp(2-2*sqrt((1+2*(H_gate+h+r)+L_g)./L_sd));

num=2*pi.*(L_sd+L_g);

den=2*L_g+tau_bk*(H_gate+h+r);

Z_7=log(num/den);
```

```
C_gtg=3*k_2*epsilon*H_gate./L_sd+alpha_gtg_sr*pi*k_2*epsilon/Z_7

tau_bkw=exp(2-2*sqrt((1+2*(H_gate+L_g))./L_sd));
numw=2*pi.*(L_sd+L_g);
denw=2*L_g+tau_bkw*H_gate;
Z_7w=log(numw/denw);

C_gtgw=k_2*epsilon*H_gate./L_sd+alpha_gtg_sr*pi*k_2*epsilon/Z_7w

figure (3)
plot(L_sd*10^9,C_gtgw*10^15,'--','LineWidth',2,'MarkerEdgeColor','k')
xlabel('Source/Drain extension length (nm)');
ylabel('Cgtg (fF)');
hold on
plot(L_sd*10^9,C_gtg*10^15,'-','LineWidth',2,'MarkerEdgeColor','k')
hold off
```

List of Publications :

- Md. Rakibul Karim Akanda, Quazi D. M. Khosru, “FEM Model of Wrap Around CNTFET with Multi-CNT and Its Capacitance Modeling”, *IEEE Transactions on Electron Devices,* vol. 60, no. 1, page 97-102, Jan, 2013
- Md. Rakibul Karim Akanda, Quazi D. M. Khosru, “Temperature Distribution of Wrap Around CNTFET with Multi-CNT Using Finite Element Method”, *IEEE Electron Devices Letter* (Submitted)