DRAIN CURRENT MODELING OF DOUBLE GATE UNIAXIALLY STRAINED SILICON MOSFET

A thesis submitted for the partial fulfillment of the requirement of the degree

of

Master of Science in Electrical and Electronic Engineering

By

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Certification

The thesis titled **"Drain Current Modeling of Double Gate Uniaxially Strained Silicon MOSFET"** submitted by Md. Nasir Uddin Bhuyian, Roll No.: 100706207 P, Session: October, 2007 has been accepted satisfactory in partial fulfillment of the requirement for the degree of *Master of Science in Electrical and Electronic Engineering* on August 6, 2011.

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Declaration

I thereby declared that, this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Dedication

To My Mother

Abstract

An accurate model to simulate drain current versus gate voltage characteristics is developed for double gate MOSFET and a drain current model is proposed for double gate uniaxially strained silicon MOSFET. The model can accurately account short channel effect and quantum mechanical effect. Effects of uniaxial strain in <110> direction are taken in the model by incorporating the changes in band structure and effective masses of electrons properly. To enhance electron mobility effectively tensile strain is applied in <110> direction. An accurate mobility model is used and enhancement in mobility due to applied strain is accounted. Comparison with universal mobility is also included. Finally velocity saturation effect and channel length modulation are also included in the model. I_{ds}-V_{gs} characteristics are simulated for both high and low drain bias. Comparison with reported experimental data for relaxed silicon DG MOSFET is provided. Percentage change in drain current due to applied strain is presented. From simulated results it is observed that, strain causes significant amount of changes in the drain current by enhancing electron mobility. In this work stress is given up to 5 GPa, which is the practical limit for uniaxial stress. Mobility change due to strain is shown to explain the effect of strain on drain current. Mobility is plotted as a function of effective field as well as gate voltage. It is found that, variation of effective mass due to strain is the dominant factor in improving drain current. It is also observed that percentage change in drain current due to strain is more above threshold voltage and it remains almost same for both high and low drain bias.

Chapter 1
Introduction

1.1 Introduction

Now a days MOS devices are produced in nanometer scale. Continuous scaling has enabled MOS gate dimensions to be reduced from 10 μm in the 1970's to the present day size of less than 100 nm. According to the guideline given by the ITRS (International Technology Roadmap for Semiconductor) [1], the scaling down of MOS devices has been accomplished by a decrease in the gate oxide thickness (t_{ox}) and an increase in the carrier doping density (N_s). High N_s results in poor carrier mobility and thus reduced transconductance and drive current. With the decrease of channel length, device engineers must think about short channel effects (SCE), such as high subthreshold slope, drain induced barrier lowering etc [2]. Also reduced gate oxide thickness (t_{ox}) leads to high gate leakage current I_G. To extend the scaling limit of conventional buck MOSFETs to 10 nm gate length and beyond, multiple gate MOSFETs (MUGFETs) are taking the attentions of researchers as they have excellent control over SCE and have high current driving ability [3].

Double gate MOSFET has excellent control over the short channel effects and has high current driving ability [3]. It does not require heavy channel doping to reduce SCE effects. With lightly doped channels, surface scattering is minimized, because of low transverse electric field. Thus carrier mobility in double-gate MOSFET channel is improved [4].

When multiple gate MOSFETs are used to enhance device performance by reducing leakage currents and short channel effects, still their mobility have to be increased. As silicon layer thickness decreases, effective mobility drastically degrades at lower t_{Si} values. An efficient technique to increase carrier mobility is to use strain engineering technique, which has been followed for mobility enhancement for quite a long time. Various materials were tested and studied with biaxial strain [5] [6]. Recent investigations proved that, using uniaxial strain, device mobility can be improved by a more scale than using biaxial strain [7], [8], [9]. An accurate model of Current-Voltage (I-V) is necessary for double gate uniaxially strained Si MOSFETs. In this work a drain current model for double gate MOSFET with uniaxilly strained silicon body has been proposed.

A number of models for symmetric double gate MOSFET drain current have been developed [10], [11], [12]. Our model is able to take account of the volume inversion effect, as charge sheet approximation, commonly employed in all surface potential based bulk MOSFET models is not invoked. As the silicon thickness decreases to 10 nm and below, quantum mechanical effects become significant [13], [14], [15]. With the inclusion of quantum mechanical effect, velocity saturation and channel length modulation effect, this model can simulate I-V characteristics of uniaxially strained DG MOSFET with a high level of accuracy.

1.2 Literature Review

Taur [10], [11] derived an analytical potential and drain current model for symmetric double gate MOSFET by solving Poisson and current continuity equation with gradual channel approximation. Without invoking charge sheet approximation [12], this model is derived directly from Pao-Sah integral[16] for undoped DG MOSFET. One problem with

this model is to solve an implicit transcendental equation. To avoid computational inefficiency and sporadic exceptions (e.g., divergence), associated with iterative method, which is the most universal approach to deal with implicit equations, an explicit continuous model with ultra high accuracy has been used [17], [18].

Liang et al [19] investigated short channel effects in DG MOSFETs and provided a 2-D analytical solution. Including threshold voltage shift due to SCE, the model covers threshold voltage roll-off, DIBL effects and subthreshold slope degradation in DG MOSFET. In the subthreshold regime, the electrostatics in the device body is dominated by the interelectrode capacitive coupling between electrodes. Subthreshold characteristics of DG MOSFET were discussed in [20], [21], [22]. Short channel effects were also accounted and investigated by Yang and Fossum [23].

In UTB DG MOSFET, carriers are confined in a thin silicon film, in addition to the field induced electrical confinement, necessitates the modeling of quantum mechanical effects. Various approaches have been applied to study the quantum mechanical effects, including non-equilibrium Greens function[13], density gradient model[14], [15] and Monte Carlo simulation [24], [25], [26]. Carrier-energy quantization in the generic DG MOSFETs were investigated via a physical model developed by Ge[27]. In [28] using variational approach, quantum effects were investigated. Previously different energy subbands were approximated by a uniform sine wave function peaks at the center of the silicon film[29]. But this approximation is valid only in the subthreshold region. In this work, quantum corrections have been incorporated in the analytical model by including threshold voltage shift and gate capacitance degradation due to QM effects according to [30].

Mobility is an important parameter for device simulation. A comprehensive understanding of the inversion layer mobility is presented by Takagi in [31], [32], where effects of substrate impurity concentration and surface orientation on the mobility were

explained with various scattering mechanisms. Experimental investigations [33], [34], [35], [36] and Monte Carlo simulations [37], [38] give an overview of single gate and double gate MOSFET mobility. To simulate devices with body thickness $t_{Si} \geq 4$ nm, a mobility model is given in [39]. In the present work a low field mobility model presented by Reggiani [40] is used, where four different additional effects were modeled: 1) the shrinking of the inversion-layer thickness due to structural and field confinement, 2) subband-level repopulation, 3) scattering induced by thickness fluctuations, and 4) surface-phonon scattering. All these literatures are used to model current-voltage characteristics of symmetric double gate MOSFET accurately.

To increase device speed and other properties by new alternative procedures, without scaling down further below the saturation level, several techniques were studied [41]. Strain engineering is one of the efficient techniques, which has been used for quite a long time. In the literature many studies on the application of biaxial strain in MOS devices are available [42], [43], [44]. Sun [7], Uchida [9], Rochette [45] demonstrate that uniaxial strain can improve inversion layer mobility more than its biaxial counterpart. Accurate drain current model for uniaxially strained DG MOSFET is much necessary, but little concentration is given on it.

Process of uniaxial strain in highlighted in [46], [47], [48]. Various effects of uniaxial strain on devices were studied and the underlying physics were presented by several authors [49], [50], [51]. Reliability of SiN capping layer to introduce uniaxial strain has been studied by Giusi [52]. But no literature has focused the study of I-V characteristics for double gate uniaxially strained silicon MOSFET.

Baslev [53] provided the change in the properties in Si energy bands due to uniaxial strain. His expressions for net shift of energy profiles due to the application of strain are much feasible than others e.g [54], because of their suitability for both high and low levels of stress. By changing the curvature of the band structure, strain causes change in

the effective masses [55]. By incorporating the effects of strain on band diagram and effective mass, change in DG MOSFET mobility due to strain is achieved, which leads to an efficient modeling of drain current in all regions of operation.

1.3 Problem Identification and Statement of The Problem

Bulk CMOS technology is already closed to the limits of scalability. Double gate MOSFET takes attention of researchers because with double gate and fully depleted silicon film, the greater control of the gate over the silicon channel results in suppression of short channel effects, even when the silicon film is undoped or lightly doped. It has been found that uniaxial strain can enhance carrier mobility in the channel much better than its biaxial counterpart. Drain current model for double gate MOSFET is available in the literature. Several studies show the effects of uniaxial strain on silicon band structure and effective masses. But drain current model for double gate uniaxially strained silicon MOSFET is absent in the literature.

1.4 Objective of This Work

In this work, a drain current model for double gate MOSFET with uniaxially strained silicon body will be developed. Short channel effects and quantum mechanical effects will be incorporated in the model, so that the model can give accurate result for ultrathin devices. Effective field will be calculated from the inversion charge density to get correct mobility for this work. The mobility model will take account of the shrinking of the inversion layer thickness due to structural and field confinement as well as the change due to temperature and doping density. Band splitting and effective mass variation due to strain will be included accurately so that device that device under practical level of straining can be analyzed

Tensile stress will be given to NMOS silicon body according to the convention. Stress level will be varied up to 5 GPa, which is practical limit of stress application. In this work, tensile stress will be given in <110> direction to enhance mobility in maximum proportion. Effect of velocity saturation and channel length modulation will also be included, so that the model can be used for both high and low drain bias condition.
Results obtained by using drain current model will be compared with reported experimental data for relaxed silicon body. Simulation using the proposed drain current model for double gate unaxially strained silicon MOSFET will be done and percentage change in drain current due to uniaxial strain will be given along with comparison of drain currents with relaxed silicon body and strained silicon body for various levels of strain.

1.5 Organization of The Thesis

In chapter 2 double gate MOSFET structure and drain current model will be presented. The method to solve the implicit equation to get explicit solution will be discussed for the purpose of simulation. Also necessary theories to include strain effect on band structure and effective mass will be explained from literature. In chapter 3 results from simulation will be presented. At first comparisons with reported experimental data for relaxed silicon double gate MOSFET with both low and high drain bias conditions will be given to verify the accuracy of the model. Ids-Vgs for double gate MOSFET will be simulated for different stress conditions for both high and low drain bias. Results using the model will be compared with relaxed Ids-Vgs and percentage changes in drain current due to strain will also be discussed. Change in mobility due to strain will also be given to provide physical insight about the effect of strain on drain current.

Chapter 2

Drain Current Model for Double Gate MOSFET and Uniaxial Strain

This section describes drain current model for double gate MOSFET and effects of uniaxial strain on drain current. An accurate drain current model considering quantum-mechanical effects, short channel effects, velocity saturation effect and channel length modulation is given. Effects of uniaxial strain on the drain current of double gate MOSFET is presented by explaining the changes in band diagram and effective mass due to uniaxial strain.

2.1 Double Gate MOSFET Structure

Metal-oxide-semiconductor field effect transistor (MOSFET) is a widely used semiconductor device, which has an enormous impact on every area of digital world. MOSFETs are fabricated using silicon as semiconductor, SiO_2 as insulator and metal or polysilicon as the gate electrode. Here, the electric field is controlled by the voltage applied to the gate. In a DG MOSFET, two gates are used, which give the opportunity to

reduce doping concentration (N_s). Fig. 2.1 shows the schematic diagram of a double gate MOSFET [11]. In case of symmetric double gate MOSFET, both gates have same materials and identical oxide thickness.

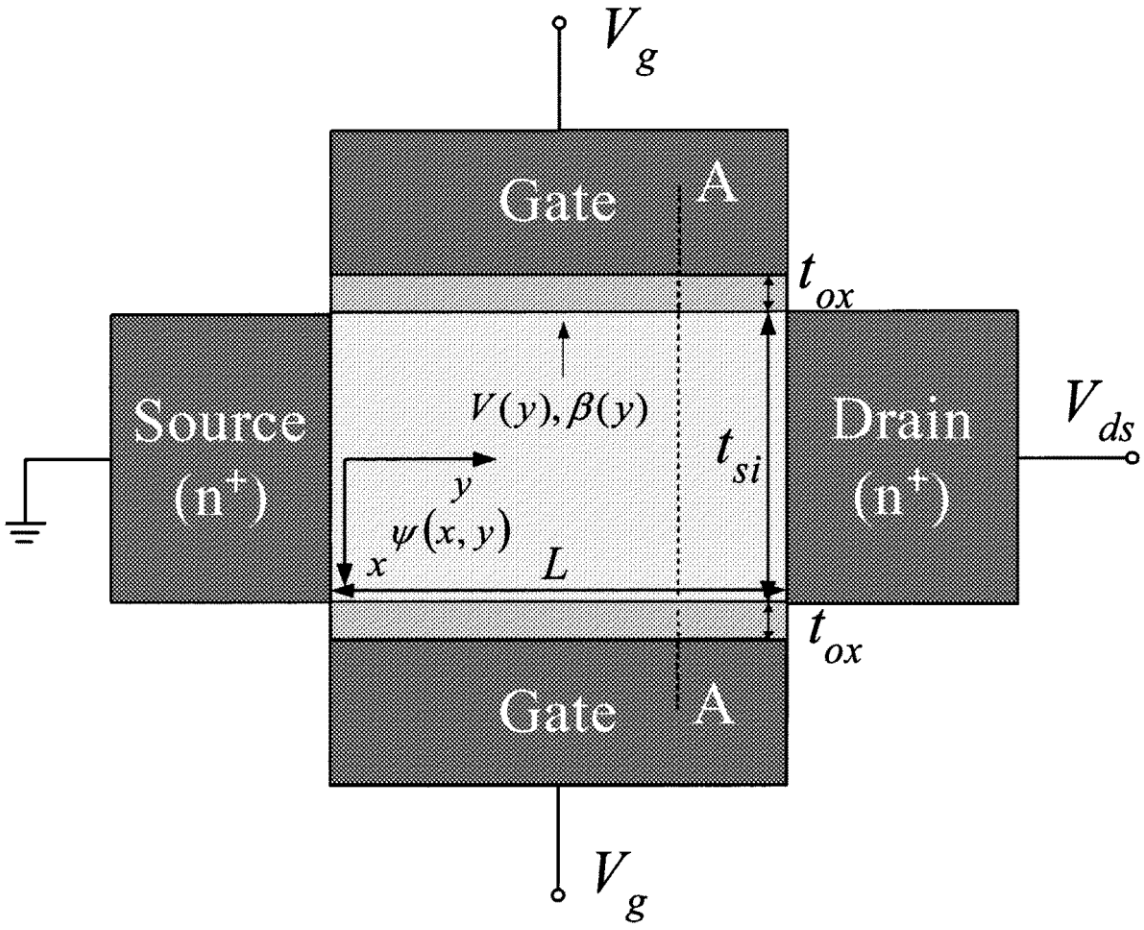

Fig. 2.1. Schematic diagram of a n-channel DG MOSFET [11].

In an n-channel MOSFET the device is fabricated on a p-type substrate, which is a single crystal silicon wafer, that provides physical support for the device. Source and drain regions are heavily doped n-type region. On the contrary in a DG MOSFET, lightly doped or undoped ultrathin (Si) bodies (UTBs) are used in place of p-type substrate, which reduces surface scattering as transverse electric fields are low. Like single gate MOSFET, here SiO_2 may be used as insulator between the gate and the substrate. Now a

days, device engineers use high-K dielectric materials as insulator. As CMOS scaling is reaching its limit, DG MOSFETs are subjected to intense research for very large scale integration (VLSI) due to their excellent control over short channel effect and high current driving ability.

2.2 Drain Current Model for Symmetric DG MOSFET:

Taur [11] derived a continuous analytical drain current (I-V) model for DG MOSFET from closed form solution of Poisson's equation and current continuity equation. In the model, silicon film is considered as lightly doped or undoped. Fig. 2.2 shows the band diagram of a DG MOSFET along a vertical cut (AA) shown in Fig. 2.1 [11]. Here the potential ψ(x, y) is defined as the intrinsic Si (midgap) level referenced to the fermi level of the n+ source.

Considering mobile charge terms only, Poisson's equation takes the following form [10]

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{q(\psi - V)}{kT}} \tag{2.1}$$

Here V is the quasi-Fermi potential, that varies laterally from source to the drain, and is independent of x. n_i is the intrinsic carrier density, K is Boltzman's constant and ε_{Si} is the permittivity of Si. Integraing equation (2.1) two times the general solution can be obtained as [10]

$$\psi(x) = V - \frac{2kT}{q} \ln\left[\frac{t_{Si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{Si} kT}}\cos\left(\frac{2\beta x}{t_{Si}}\right)\right] \tag{2.2}$$

In equation (2.2) t_{Si} is the thickness of Si film, and the dimensionless parameter β is a function of V to be determined from the following boundary condition [11]

$$\frac{q(V_g - \Delta\varphi - V)}{kT} - \ln\left[\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}kT}{q^2 n_i}}\right] = \ln\beta - \ln[\cos\beta] + \frac{2\varepsilon_{Si}t_{ox}}{\varepsilon_{ox}t_{Si}}\beta\tan\beta \qquad (2.3)$$

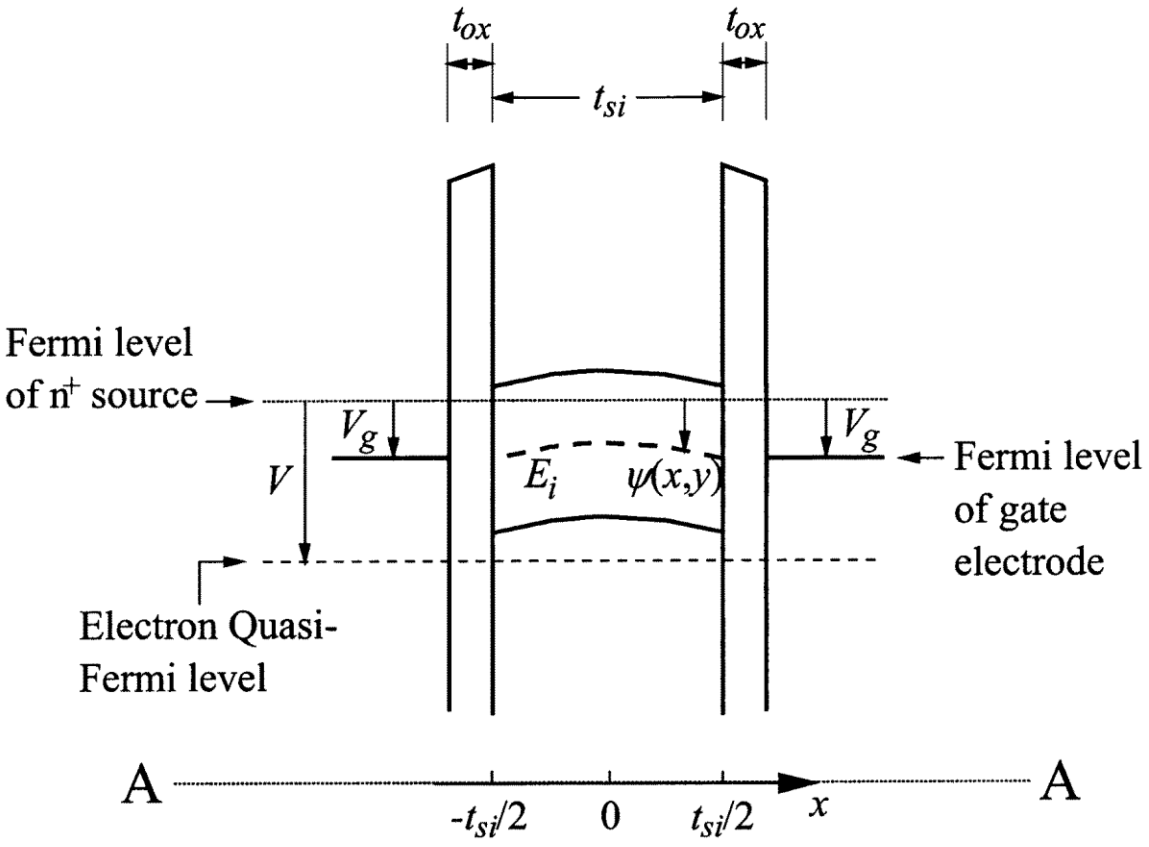

Fig. 2.2: Band-diagram along a vertical cut (AA) in Fig. 2.1 [11].

Here ε_{Si} and ε_{ox} are permittivity of Si and gate oxide respectively, t_{Si} and t_{ox} are thicknesses of Si film and gate oxide respectively, $\Delta\theta$ is the work function difference between gate electrode and intrinsic silicon for both top and bottom gate. From equation (2.3), β can be solved by varying Vg and V. For a given value of Vg, β is a function of V along the channel direction. On the other hand, for a given value of V, β changes with Vg. According to Gradual Channel Approximation (GCA), V changes along the channel(y direction) and independent of x direction. So β is also independent of x direction.
According to current continuity equation,

$$I_{ds} = \mu W Q_i \frac{dV}{dy} \tag{2.4}$$

In equation (2.4) μ is the mobility, W is the device width and Q_i is the inversion charge per unit gate area. Integrating $I_{ds}dy$ from the source to the drain and expressing dV/dy as (dV/d β)(d β/dy), Pao-Sha's integral can be written as

$$I_{ds} = \mu \frac{W}{L} \int_0^{V_{ds}} Q_i(V) dV = \mu \frac{W}{L} \int_{\beta_s}^{\beta_d} Q_i(\beta) \frac{dV}{d\beta} d\beta \tag{2.5}$$

In equation (2.5) β_s is the value of β obtained from equation (2.3), by using V=0 and β_d correspond to the value of V= V_{ds}. From Gauss's law

$$Q_i = 2\varepsilon_{Si} \left(\frac{d\psi}{dx} \right)_{x=t_{Si}/2} \tag{2.6}$$

Using equation (2.2) and (2.6), we get

$$Q_i = 2\varepsilon_{Si} \left(\frac{2kT}{q} \right) \left(\frac{2\beta}{t_{Si}} \right) \tan\beta \tag{2.7}$$

dV/dβ can be determined as a function of β from equation (2.3). Substituting these expressions in equation (2.5), I_{ds} can be found as [11]

$$I_{ds} = \mu \frac{W}{L} \frac{4\varepsilon_{Si}}{t_{Si}} \left(\frac{2kT}{q} \right)^2 \left[\beta \tan\beta - \frac{\beta^2}{2} + \frac{2\varepsilon_{Si} t_{ox}}{\varepsilon_{ox} t_{Si}} \beta^2 \tan^2 \beta \right]_{\beta_d}^{\beta_s} \tag{2.8}$$

2.2.1 Explicit Solutions for Symmetric Double Gate MOSFET

General Method

Chen [18] described a method to solve the implicit equation of MOSFET surface potential. In three steps by this method an accurate explicit solution can be obtained. In the first step, an initial estimate is made, which is an explicit continuous function of gate voltage, quasi-Fermi potential etc. The explicit function should be properly chosen, because it is the most important step. Piecewise functions can not be chosen as initial estimate, as they cause discontinuities of derivatives.

In the second step, the initial estimate is to be modified with high order correction terms. If our implicit equation is like f(x; a, b, c) = 0, where x is to be solved and a, b, and c are independent variables, and our initial approximation is g(a, b, c), using Taylor's series near g, f can be approximated as [17]

$$\sum_{n=0}^{\infty} \frac{1}{n!} \frac{\partial^n f(x;a,b,c)}{\partial x^n}\Big|_{x=g(a,b,c)} [x - g(a,b,c)]^n \tag{2.9}$$

Expanding up to third order, the correction term will be

$$f_{g0} + f_{g1} h + \frac{f_{g2}}{2} h^2 + \frac{f_{g3}}{6} h^3 + O(h^4) = 0 \tag{2.10}$$

where $h = x - g(a,b,c)$ and $f_{gn} = \left.\frac{\partial^n f(x;a,b,c)}{\partial x^n}\right|_{x=g(a,b,c)}$ and n=0,1,2,3. Though the cubic equation has exact analytical solutions, considering that h is a small quantity, the solution should be simplified into a rational form for the purpose of efficiency. Many choices of approximated rational solutions are available in the literature. According to Yu's model [17]

$$h = -\frac{f_{g0}}{f_{g1}}\left(1 + \frac{f_{g0} f_{g2}}{2 f_{g1}^2} + \frac{f_{g0}^2\left(3 f_{g2}^2 - f_{g1} f_{g3}\right)}{6 f_{g1}^4}\right) \tag{2.11}$$

After the addition of correction term, the approximate expression for x is

$$v(a,b,c) = g(a,b,c) + h(a,b,c) \tag{2.12}$$

To further improve the accuracy of the solution, another high order correction term may be added to get ultra accurate approximation of x

$$v(a,b,c) = g(a,b,c) + h(a,b,c) + w(a,b,c) \tag{2.13}$$

where $w(a,b,c)$ is the new correction term in the last step.

Explicit Model for SDG MOSFET

For drain current, the intermediary variable β has to be estimated. The implicit equation governing the boundary condition has no exact analytical solution and has to be solved approximately. With independent variables r and F, the equation is much more complicated than one with a single variable.

If β is replaced by $z \equiv \tan\beta$, the implicit equation will be

$$f(z;r,F) = \ln\left[\arctan(z)\sqrt{1+z^2}\right] + rz\arctan(z) - F = 0 \tag{2.14}$$

where, $F = \dfrac{q(V_g - \Delta\phi - V)}{2KT} - \ln\dfrac{2L_{Di}}{t_{Si}}$, structural parameter $r = 2\varepsilon_{Si}t_{ox}/\varepsilon_{ox}t_{Si}$, intrinsic Debye length $L_{Di} = \sqrt{2\varepsilon_{Si}kT/q^2 n_i}$. The range of β is $0 < \beta < \pi/2$.

Following the general method, z can be computed in three steps [17]

1) The asymptotic behavior of z are

$$z = \exp F \text{ (as } z \to 0) \qquad z = \frac{2F}{\pi r} \text{ (as } z \to \infty) \tag{2.15}$$

By using the smoothing function to connect the above asymptotic behavior

$$z_1 = \sqrt{\left(\frac{8}{\pi^2 r^2}\right)^2 + \left(\frac{4}{\pi r}\right)^2 \ln^2\left(1 + e^{F/2}\right)} - \frac{8}{\pi^2 r^2} \tag{2.16}$$

2) Compute

$$\gamma_2 = \arctan z_1$$

$$\delta_2 = 1/\left(1 + z_1^2\right)$$

$$\eta_0 = \frac{1}{2}\ln\left(\gamma_2^2/\delta_2\right) + r z_1 \gamma_2 - F$$

$$\eta_1 = \frac{\delta_2}{\gamma_2} + (1 + r) z_1 \delta_2 + r\gamma_2$$

$$\eta_2 = -\frac{\delta_2^2}{\gamma_2^2} - \frac{2 z_1 \delta_2^2}{\gamma_2} + \left(1 + 2r - z_1^2\right)\delta_2^2$$

$$\eta_3 = \frac{2\delta_2^3}{\gamma_2^3} + (6 z_1^2 - 2)\frac{\delta_2^3}{\gamma_2} + (2 z_1^2 - 6 - 8r) z_1 \delta_2^3$$

$$z_2 = z_1 - \frac{\eta_0}{\eta_1}\left(1 + \frac{\eta_0\eta_2}{2\eta_1^2} + \frac{\eta_0^2\left(3\eta_2^2 - \eta_1\eta_3\right)}{6\eta_1^4}\right) \tag{2.17}$$

3) Compute

$$\gamma_3 = \arctan z_2$$

$$\delta_3 = 1/\left(1+z_2^2\right)$$

$$\lambda_0 = \frac{1}{2}\ln\left(\gamma_2^3/\delta_3\right) + rz_2\gamma_3 - F$$

$$\lambda_1 = \frac{\delta_3}{\gamma_3} + (1+r)z_2\delta_3 + r\gamma_3$$

$$\lambda_2 = -\frac{\delta_3^2}{\gamma_3^2} - \frac{2z_2\delta_3^2}{\gamma_3} + \left(1+2r-z_2^2\right)\delta_3^2$$

$$\lambda_3 = \frac{2\delta_3^3}{\gamma_3^3} + \frac{6z_2\delta_3^3}{\gamma_3^2} + \left(6z_2^2-2\right)\frac{\delta_3^3}{\gamma_3} + \left(2z_2^2-6-8r\right)z_2\delta_3^3$$

$$z_3 = z_2 - \frac{\lambda_0}{\lambda_1}\left(1 + \frac{\gamma_0\lambda_2}{2\lambda_1^2} + \frac{\lambda_0^2\left(3\lambda_2^2-\lambda_1\lambda_3\right)}{6\lambda_1^4}\right) \tag{2.18}$$

Using z_3 as an approximation for z, an explicit solution for β can be obtained, which is given by arctan z_3.

2.3 Short Channel Effects and Quantum Mechanical Effects

2.3.1 Short Channel Effects in DG MOSFET

In a MOSFET, for very small geometries, threshold voltage V_T decreases with channel length L. This effect is called the short channel effect (SCE). If small channel length MOSFETs are not scaled properly, and the source/drain junctions are too deep or the channel doping is too low, there can be unintended electrostatic interactions between the source and the drain knows as Drain Induced Barrier Lowering (DIBL). This leads to

punchthrough leakage or breakdown between the source and the drain, and loss of gate control. To fully quantify the SCE, DIBL, threshold voltage roll-off , and subthreshold slope, the pre exponential term needs to be determined in addition to the exponential scale length.

In the subthreshold region, the mobile charge and fixed charge are negligible. In both the insulator regions and silicon regions, Poisson's equation becomes [19]

$$\frac{\delta}{\delta x}\left(\varepsilon\frac{\delta\psi}{\delta x}\right)+\frac{\delta}{\delta y}\left(\varepsilon\frac{\delta\psi}{\delta y}\right)=0 \tag{2.19}$$

Assuming source and drain junctions are abrupt, the boundary conditions are

Top gate: $\psi\left(-t_{Si}/2-t_{ox},y\right)=V_g-\Delta\phi_1,\qquad 0<y<L$

Bottom gate $\psi\left(t_{Si}/2+t_{ox},y\right)=V_g-\Delta\phi_2,\qquad 0<y<L$

Source $\psi(x,0)=E_g/2q,\qquad -t_{Si}/2<x<t_{Si}/2$

Drain $\psi\left(x,L\right)=V_{ds}+E_g/2q,\qquad -t_{Si}/2<x<t_{Si}/2$ (2.20)

Using the superposition method, neglecting high order terms, the 2-D potential expression in the subthreshold region can be obtained as [19]

$$\psi(x,y)=\frac{\Delta\phi_1-\Delta\phi_2}{t_{Si}+\frac{2t_{ox}\varepsilon_{Si}}{\varepsilon_{ox}}}x+V_g-\frac{\Delta\phi_1+\Delta\phi_2}{2}+\frac{b_1\sinh\left(\frac{\pi(L-y)}{\lambda_1}\right)+c_1\sinh\left(\frac{\pi y}{\lambda_1}\right)}{\sinh\left(\frac{\pi y}{\lambda_1}\right)}\cos\left(\frac{\pi x}{\lambda_1}\right) \tag{2.21}$$

From [19], the expressions for first coefficients of 2-D potentials are

$$b_1 = \frac{2\lambda_1^2 \tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{Si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{Si}}{2} + \frac{\sin(\pi t_{Si}/2\lambda_1)}{\sin(2\pi t_{ox}/\lambda_1)} t_{ox}\right]} \times\left(\frac{E_g}{2q} + \frac{\Delta\phi_1 + \Delta\phi_2}{2} - V_g\right) \tag{2.22}$$

$$c_1 = \frac{2\lambda_1^2 \tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{Si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{Si}}{2} + \frac{\sin(\pi t_{Si}/2\lambda_1)}{\sin(2\pi t_{ox}/\lambda_1)} t_{ox}\right]} \times\left(\frac{E_g}{2q} + V_{ds} + \frac{\Delta\phi_1 + \Delta\phi_2}{2} - V_g\right) \tag{2.23}$$

Scale length λ_1 can be solved from the following equation

$$\tan(\pi t_{ox}/\lambda_1)\tan(\pi t_{Si}/2\lambda_1) = \varepsilon_{ox}/\varepsilon_{Si} \tag{2.24}$$

By solving the potential, the drain current as a function of the gate voltage in the subthreshold region can be derived from the current continuity equation. The result includes all threshold voltage roll-off, drain induced barrier lowering, and subthreshold slope degradation. In this work, these effects are included by deriving subthreshold slope and threshold voltage shift. Threshold voltage shift can be found from the following equation [19]

$$(\Delta V_t)_{SCE} = -2\sqrt{b_1 c_1}\, e^{-\pi L/2\lambda_1} + \frac{kT}{q}\ln\left\{\frac{\sqrt{\pi}}{2D_1 L}\left[erf\left(D_1(L - y_c)\right) + erf\left(D_1 y_c\right)\right]\right\} \tag{2.25}$$

where $D_1 = \left(\pi^2 q\sqrt{b_1 c_1}\, e^{-\pi L/2\lambda_1} / \lambda_1^2 kT\right)^{1/2}$, x_c and y_c are minimum potential and function erf is the error function defined as

$$erf(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-u^2} du \tag{2.26}$$

Subthreshold current slope is given by [19s]

$$S \approx \left\{1-2B\left[1+\frac{1}{8}\left(\frac{V_{ds}}{E_g/2q+V_{ds}/2-1okT/q}\right)^2\right]\times\cos\left(\frac{\pi x_c}{\lambda_1}\right)e^{-\pi L/2\lambda_1}\right\}^{-1}\times 60mV/dec \tag{2.27}$$

where

$$B=\frac{2\lambda_1^2\tan(\pi t_{ox}/\lambda_1)\sin(\pi t_{Si}/2\lambda_1)}{\pi^2 t_{ox}\left[\frac{t_{Si}}{2}+\frac{\sin(\pi t_{Si}/\lambda_1)}{\sin(2\pi t_{ox}/\lambda_1)}t_{ox}\right]} \tag{2.28}$$

2.3.2 Quantum Mechanical Effects in DG MOSFET:

In a double gate MOSFET a thin silicon layer is used, which is beneficial to device scaling. In bulk devices electron motion is confined by the surface potential or field. In case of DG MOSFET, thin silicon film confined the electron motion, gives rise to threshold voltage shift and gate capacitance degradation.

The Poisson equation connecting the electrostatic potential ψ(x) to the electron density n(x) is:

$$\frac{d^2\psi(x)}{dx^2}=\frac{q}{\varepsilon_{Si}}n(x) \tag{2.29}$$

Instead of $n=n_i e^{q\psi/kT}$ in the classical model, n is expressed in quantum mechanical model as [30]

$$n(x) = \frac{kT}{\pi\hbar^2}\sum_i g_i m_i^* \sum_j \ln\left[1 + e^{\left(E_F - E_{ij}\right)/kT}\right]\varphi_{ij}^2(x) \tag{2.30}$$

In equation (2.30), E_F is the Fermi level, g_i and m_i are the degeneracy and density-of-state effective mass in the i^{th} valley, ħ is the Planck's constant, and θ_{ij} (x) is the normalized wave functions of the j^{th} subband in the i^{th} valley satisfying Schrodinger equation

$$-\frac{\hbar^2}{2m^i}\frac{d^2\phi_{ij}(x)}{dx^2} + \left(-q\psi(x)\right)\phi_{i,j}(x) = E_{i,j}\phi_{i,j}(x) \tag{2.31}$$

which is coupled to the electrostatic potential ψ(x). Here m_i is the electron effective mass in the i^{th} valley. Schrodinger and Poisson's equation can be solved using the boundary condition, which relates the potential and field at the silicon-oxide interfaces to the applied gate voltage [30]

$$\varepsilon_{ox}\frac{V_g - \Delta\varphi - \psi\left(x = \pm t_{Si}/2\right)}{t_{ox}} = \pm\varepsilon_{Si}\frac{d\psi}{dx}\Big|_{x=\pm t_{Si}/2} \tag{2.32}$$

Using a 1-D Schrodinger-Poisson solver, Wang [30] solved equation (2.29) and (2.31) numerically for a 1-D MOS device. Calculation of quantum and classical electron density with various gate voltages are shown in Fig. 2.3, which shows that, below the threshold voltage (0.53 V), the quantum electron concentration peaks at the middle of the silicon film and vanishes at the silicon-oxide interface, whereas the classical electron density is essentially flat within the silicon film. Above threshold voltage, quantum electron concentration has peak values at some distance away from the two silicon surfaces, where classical electron concentration shows peaks at the surfaces.

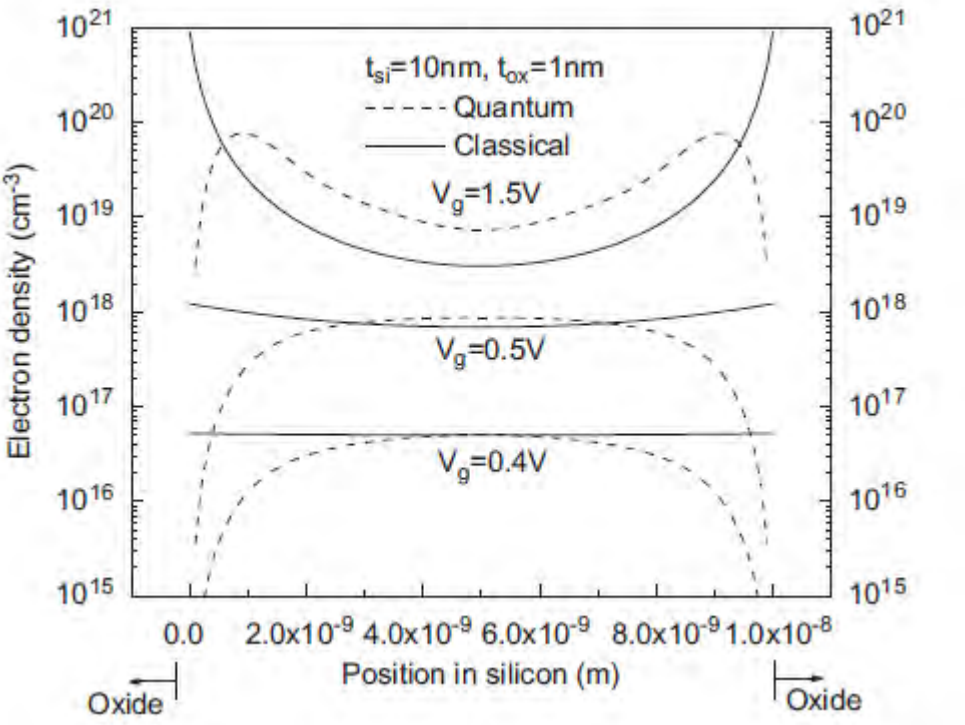

Fig. 2.3: Classical and quantum electron volume density obtained from Shrodinger-Poisson solver as a function of positions in the silicon film [30]

In case of DG MOSFET, quantization effect causes discrete subbands higher than the bottom of the conduction band and like bulk MOSFET, here electron concentration peaks away from the surface. In Fig. 2.4, mobile sheet charge density Q_i vs gate voltage is shown using the Schoridinger-Poisson solver [30]. From Wang's analysis, it is clear that, quantum threshold voltage V_t is higher than the classical value. The lower value of quantum charge sheet density implies that due to quantum effect, gate capacitance C_g should be modeled to a lower value than that using classical analysis.

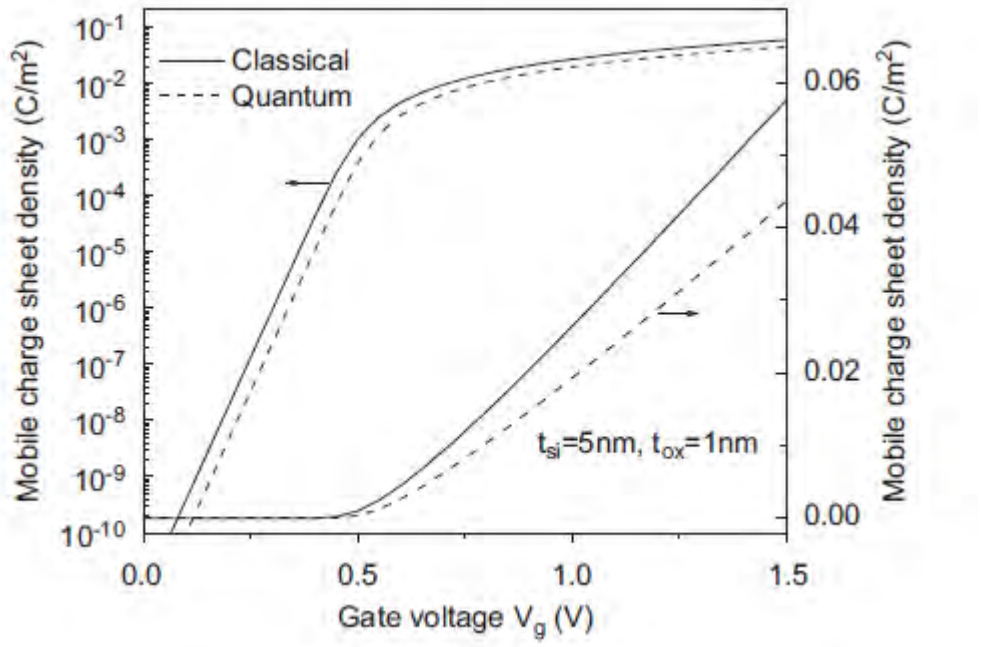

Fig. 2.4: Mobile charge sheet density vs gate voltage for a symmetrical DG MOSFET [30]

To model quantum mechanical effects in symmetric double gate MOSFET, according to Wang [30], threshold voltage shift due to quantum mechanical effect is given by

$$\Delta V_t^{QM} = \frac{\hbar^2 \pi^2}{2qm^* t_{Si}^2} \tag{2.33}$$

and the gate capacitance degradation is modeled by an increase in the inversion layer as [30]

$$\delta t_{inv} = \left(\frac{7\varepsilon_{Si}\hbar^2}{m^* q Q_i} \right)^{1/3} \tag{2.34}$$

2.4 Mobility

Mobility is a key parameter in determining the current within the device. The mobility can be simply defined as the average particle drift velocity per unit electric field.

$$\mu_n = -\frac{\langle v_x \rangle}{\varepsilon_x} \tag{2.35}$$

The units of mobility are cm^2/V-s. The negative sign in the definition results in a positive value of mobility, since electrons drift opposite to the electrical field. The current density can be written in terms of mobility as

$$J_x = qn\mu_n\varepsilon_x \tag{2.36}$$

If hole concentration is p and hole mobility is $\mu_p = \frac{\langle v_x \rangle}{\varepsilon_x}$, for both electron and hole participation, current density should be modified as

$$J_x = q(n\mu_n + p\mu_p)\varepsilon_x = \sigma\varepsilon_x \tag{2.37}$$

The parameters determining mobility are effective mass of the carriers and mean free time η. Effective mass m* is a property of the material's band structure. For example, GaAs has lighter particles, so electrons are more mobile. Mean free time between scattering depends on temperature and impurity concentration in the semiconductor.

2.4.1 Mobility in MOSFET

The mobility of carriers in the channel of a MOSFET is lower than in bulk semiconductors, because there are additional scattering mechanisms. Since carriers in the channel are very close to the semiconductor-oxide interface, they are scattered by surface roughness and by coulombic interaction with fixed charges in the gate oxide. With the increase of gate bias, carriers become more closer to the oxide-silicon interface and as a result mobility degrades with increasing gate voltage.

Electron and hole mobility at room temperature in the MOSFET inversion layer as a function of average transverse effective field in the middle of inversion layer is independent of technology or device structural parameters, which is called universal mobility. Takagi [31], [32] gave the expressions for effective field in the middle of the inversion layer. For electrons transverse field in the middle of inversion layer is given by

$$E_{eff} = \frac{1}{\varepsilon_{Si}}(Q_d + \frac{1}{2}Q_s) \tag{2.38}$$

and for holes $$E_{eff} = \frac{1}{\varepsilon_{Si}}(Q_d + \frac{1}{3}Q_s) \tag{2.39}$$

In the above equations, Qs and Qd are concentration of surface inversion charge and surface depletion charge respectively.

In addition, mobility also depends strongly on drain bias or longitudinal electric field. The carrier drift velocity increases linearly with electric field until the field reaches Esat. After this the velocity saturates at v_s and it can be no longer described in terms of mobility. These effects can be described as:

$$v = \mu E \quad \text{for} \quad E < Esat \tag{2.40}$$

and $$v = v_s \quad \text{for} \quad E > Esat \tag{2.41}$$

The maximum longitudinal electric field near the drain of the channel is approximately given by the voltage drop along the pinch-off region, (V_D - $V_D(sat)$), divided by the length of the pinch-off region, ΔL.

$$E_{\max} = \left(\frac{V_D - V_D(sat)}{\Delta L} \right) \tag{2.42}$$

2.4.2 Low-Field Electron Mobility Model

Electron mobility in single-gate (SG) and double-gate (DG) UTB-FETs has been mainly investigated experimentally [33], [34], [35], [36] and by Monte Carlo simulation [37], [38]. Reggiani et al [40] described a physically based low field electron mobility model for SG and DG FETs with undoped channels. The specialty of this model is that, it accurately predicts mobility for devices with Si thicknesses down to 2.48 nm. In this model the shrinking of the inversion layer thickness due to structural and field confinement, sub-band level repopulation, scattering induced by thickness fluctuations and surface-phonon scattering have been modeled along with the effect of doping density and temperature.

Phonon Limited Mobility

In a silicon film due to structural confinement and the application of transverse field, two energy-eigenvalue ladders are formed. Two unprimed valleys having lower energy have longitudinal effective mass in the confinement direction. Other four valleys (unprimed) have higher energy as their transverse effective masses coincide with the confinement direction. For each ladder, phonon limited mobility is defined as [40]

$$\mu_{ph,v} = \frac{q\langle \tau_v \rangle}{m_{c,v}} \tag{2.43}$$

where q is the elementary charge, the index v =1,2 identifies the unprimed and primed ladder, respectively, $\langle \tau_v \rangle$ is the average momentum relaxation time for the vth ladder, and $m_{c,v}$ is the conduction effective mass. The total phonon limited mobility can be found

from the average of the single ladder mobilities weighted with the populations of the ladders [40].

$$\mu_{ph} = \frac{n_1}{n}\mu_{ph,1} + \frac{n_2}{n}\mu_{ph,2} \tag{2.44}$$

The momentum relaxation time $\langle \tau_v \rangle$ can be calculated by averaging the mean relaxation times $\langle \tau_{i,v} \rangle$ of the *i*th subbands in the *v*th ladder, each weighted with the population $n_{i,v}$ of the same subband.

$$\langle \tau_v \rangle = \frac{\sum_i n_{i,v} \langle \tau_{i,v} \rangle}{\sum_i n_{i,v}} \tag{2.45}$$

Considering that, most of the electron population of each subband occupies the subband bottom according to Reggiani [40]

$$\langle \tau_v \rangle = \frac{C_v W_v}{m_{d,v}} \tag{2.46}$$

where the effective width W_v of the electron distribution relative to the *v*th ladder has been introduced

$$W_v = \frac{W_{Tv}}{\left[1 + \left(W_{Tv}/W_{Ev}\right)^{\beta}\right]^{1/\beta}} \tag{2.47}$$

$$W_{Ev} = W_{E0v}\left(\frac{\varepsilon_{eff}}{\varepsilon_{eff\,0}}\right)^{-\gamma} \tag{2.48}$$

and

$$W_{Tv} = \frac{2}{3}t_{Si} + W_{T0v}\left(\frac{t_{Si}}{t_{Si0}}\right)^{4}\left(\frac{\varepsilon_{eff}}{\varepsilon_{eff\,0}}\right) \tag{2.49}$$

where

$W_{T01} = 3\times10^{-10}$ cm

$W_{T02} = 3.5\times10^{-11}$ cm

$W_{E01} = 2.91\times10^{-7}$ cm

$$W_{E02} = 8.37 \times 10^{-7} \text{ cm}$$

$$\gamma = 0.29$$

For large thicknesses, $P_1=n_1/n$ is independent of the Si thickness and depends mildly on the electric field. When the thickness is reduced to about 4 nm, the electrons populate more the unprimed ladder, because of the increasing separation between the energy minima of the two ladders [40]

$$\Delta E_c = E_c^{/} - E_c = \frac{(\hbar\pi)^2}{2m_0 t_{Si}^2}\left(\frac{1}{m_{z2}} - \frac{1}{m_{z1}}\right) \tag{2.50}$$

To model phonon limited mobility accurately, the relative occupancy P_1 is modeled as a function of ΔE_c [40]

$$P_1 = p_1 + \frac{1 - p_1}{1 + p_2 \exp\{-p_3(\Delta E_c / k_B T)\}} \tag{2.51}$$

where k_B is the Boltzman constant, T the lattice temperature, p_1 the occupancy at large silicon thicknesses, and p_2 and p_3 are the fitting parameters. From experimental mobility curves, $p_1=0.55$, $p_2=400$ and $p_3=1.44$.

Coulomb Scattering and Surface Roughness Limited Mobility

In case of undoped Si channel, coulomb scattering can be neglected. Surface roughness mobility can be found from Takagi's model [32] as

$$\mu_{sr} = \mu_{sr0}\left(\frac{\varepsilon_{eff}}{\varepsilon_{eff\,0}}\right)^{-\delta} \tag{2.52}$$

where μ_{sr0} is a constant and $\delta = 2$

Scattering Induced by Silicon-Thickness Fluctuations

For Si thickness < 4nm, a strong degradation at low field is observed. Uchida [58] made a set of measurement at 25 K for different Si thicknesses from where the thickness-fluctuation-limited mobility can be obtained as [40]

$$\mu_{\delta t_{Si}} = \mu_{\delta t_{Si0}}\left(\frac{t_{Si}}{t_{Si0}}\right)^{6}\left[1 + C_{\delta t_{Si}}\left(\frac{\varepsilon_{eff}}{\varepsilon_{eff\,0}}\right)\right] \tag{2.53}$$

where $\mu_{\delta t_{Si0}}$ and $C_{\delta t_{Si}}$ are fitting parameters whose values are 0.15 cm^2/V-s and 160 respectively.

Scattering With Surface Optical Phonons

Esseni el al [59] explained scattering due to surface optical phonons are responsible for mobility degradation for very small silicon thicknesses. This effect can be modeled as

$$\mu_{sp} = \mu_{sp0}\exp(\eta\frac{t_{Si}}{t_{Si0}}) \tag{2.54}$$

where μ_{sp0} and η are fitting parameters, whose values are 1.145×10^{-8} cm^2/Vs and 10 respectively.

Complete Mobility Model

A mobility model, which will include all of the scattering mechanisms as discussed above can be found using Matthiesen's rule [40]

$$\frac{1}{\mu} = \frac{1}{\mu_{bulk}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{\delta t_{Si}}} + \frac{1}{\mu_{sp}} \tag{2.55}$$

2.5 Effects of Velocity Saturation and Channel Length Modulation

If a MOSFET is biased beyond saturation level, the channel electric field near the drain increases significantly and results in carrier velocity saturation. To evaluate velocity saturation, Gauss's law is applied to a velocity saturation region of length x, fin width W and fin height H, which is illustrated in Fig. 2.5 [60]. The channel electric field is assumed to increase linearly from x=0 to x= L-ΔL. It then increases exponentially from this velocity saturation region, where impact ionization hot carriers are generated. The vertical electric fields E_y and E_z at the silicon surfaces are same, as oxide thickness on top and two side channel is identical. If the fin is extremely narrow, the electric field at the top interface E_z becomes higher than electric fields at the side interfaces E_y. If the aspect ratio H/W<5, the electric fields at the three interfaces can be taken identical.

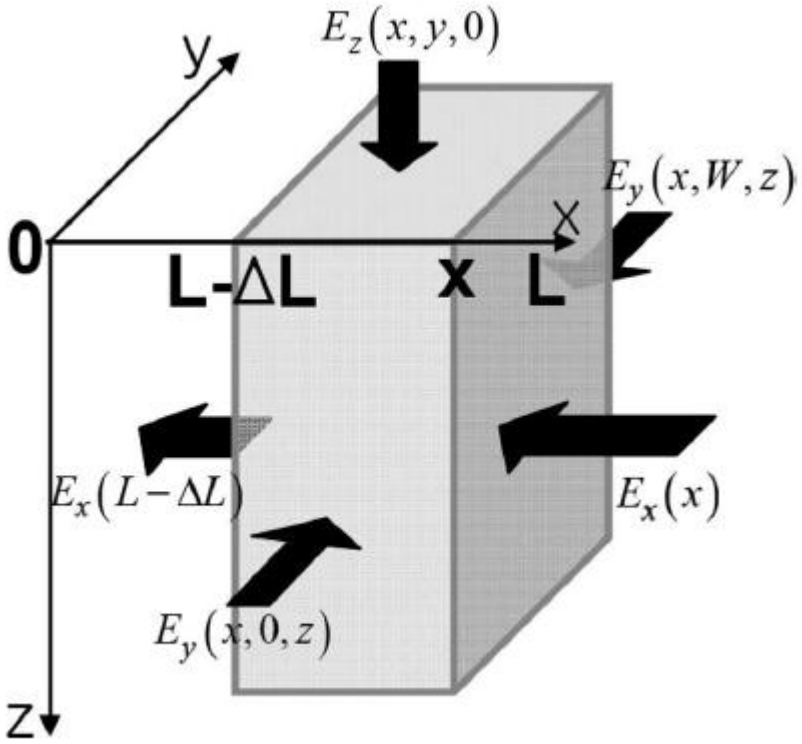

Fig. 2.5: Schematic view of the velocity saturation region [60].

Assuming that the vertical electric field at the bottom boundary $E_z(x, y, H)$ is negligible, from Gauss's law [60]

$$\{-E_x(L-\Delta L)+E_x(x)\}.W.H+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\int_{L-\Delta L}^{x}E_n(x)dx.$$

$$(2H+W)=\frac{q(N_a+N_i)}{\varepsilon_{Si}}.(x-L+\Delta L).W.H \tag{2.56}$$

Where

$$E_n(x)=\frac{V_g-V_T-V(x)}{T_{ox}} \tag{2.57}$$

Assuming that the transverse electric field E_x is uniform in the *y-z* plane, differentiating equation (2.56) with respect to x the following equation will result [60]

$$\frac{dE_x(x)}{dx}.W.H + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}.\frac{V_G - V_T - V(x)}{T_{ox}}.(2H + W) = \frac{q(N_a + N_i)}{\varepsilon_{Si}}.W.H$$

According to [60] the electric field at the velocity saturation point is continuous. So, the electric field gradient $dE_x(x)/dx$ at $x = L - \Delta L$ can be approximated to $E_{sat}/L - \Delta L$ .Also approximating the channel potential V(x) at $x = L - \Delta L$ to the saturation voltage V_{Dsat} the following equation can be obtained [60]

$$\frac{E_{sat}}{L - \Delta L}.W.H + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}.\frac{V_G - V_T - V_{Dsat}}{T_{ox}}.(2H + W) = \frac{q(N_a + N_i)}{\varepsilon_{Si}}.W.H \quad (2.58)$$

By combining equation (2.57) and (2.58) and substituting $E_x(x) = -dV(x)/dx$ a 1-D second order potential equation can be obtained as

$$\frac{d^2V}{dx^2} = \frac{V(x) - V_{Dsat}}{l^2} - \frac{E_{sat}}{L - \Delta L} \quad (2.59)$$

Where the characteristic length l for double gate MOSFET is

$$l = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\frac{W}{2}T_{ox}} \quad (2.60)$$

By solving the differential equation VSRL (ΔL) can be found from the following equation

$$\Delta L = \ln\frac{a + b + \sqrt{b^2 + 2ab + 1}}{a + b} \quad (2.61)$$

where $a = \frac{l}{L - \Delta L}$ and $b = \frac{V_D - V_{Dsat}}{E_{sat}l}$.

Due to velocity saturation, effective mobility will be changed according to the following equation [63]

$$\mu_{eff}(x) = \frac{\mu_0}{\sqrt{1 + \frac{\mu_0^2 E_{XS}^2}{v_{sat}^2}}} \tag{2.62}$$

Where, E_{XS} is the lateral field at the oxide-silicon interface.

To model channel length modulation in the post velocity saturation region, we used the formula used by Taur and Ning [61] which is

$$\Delta L = l.\ln\left[\frac{V_{DS} - V_{Dsat}}{l.E_{sat}} + \sqrt{\left(\frac{V_{DS} - V_{Dsat}}{l.E_{sat}}\right)^2 + 1}\right] \tag{2.63}$$

In the drain current equation L can be replaced by L-ΔL to model channel length modulation effect.

2.6 Theory of Strain

Strain engineering is a technique to improve device performance. The origin of strained silicon can be traced to thin Si layer grown on relaxed SiGe substrate in the late1980s. Improvement enhances in strained silicon devices mainly due to an increase in mobility as strain alters energy band structure. Two types of strain are commonly used-biaxial

strain and uniaxial strain. In case of biaxial strain, $Si_{1-x}Ge_x$ heterostructures are used in various compositions and strained Si layer is grown over relaxed SiGe layer. Uniaxial strain technique is quite new and I-V characteristics modeling of DG uniaxially strained Si MOSFET is absent in literatures. Uniaxial strain technique is explained below to provide a brief overview.

2.6.1 Uniaxial Straining Process

Uniaxial straining technique involves mechanical stress. Tensile strain is given to nMOS devices and compressive strain to pMOS devices[56]. These two types of strains are used in different proportions in different devices. In process induced strain, high-stress capping layers are deposited on the gate of MOSFET. Nitride capping layer can be used for both tensile strain and compressive strain. Another process uses SiGe layer in source and drain side. These two processes are shown in Fig. 2.6 and Fig. 2.7.

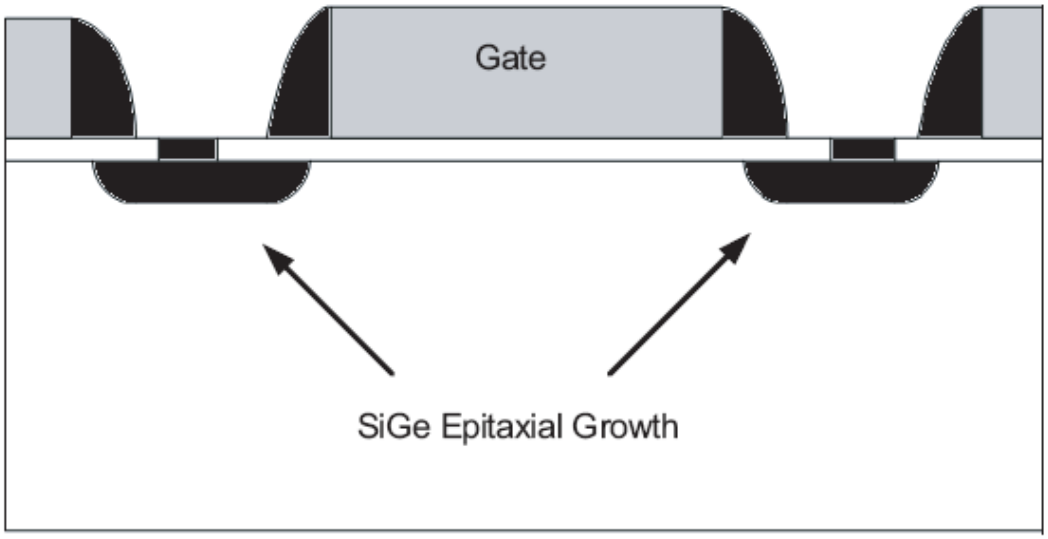

Fig. 2.6: Uniaxial straining prcess with SiGe layer in source and drain region

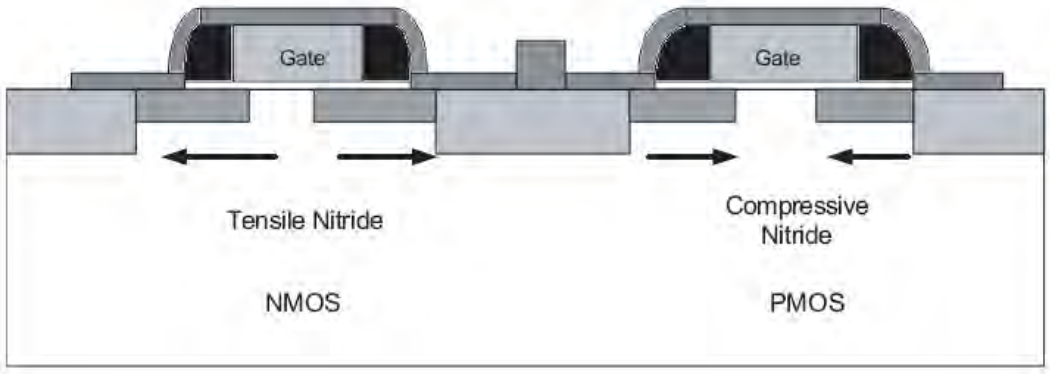

Fig. 2.7: Uniaxial straining process with nitride capping layer.

Uniaxial strain gives quite different results than that given by biaxial strain. In Fig. 2.8, biaxial straining process [8] is shown on a cubic crystal. By applying stress, the shape of x and yz plane are changed from square to rectangular, whereas xy plane remains square. Cubic crystal under <110> uniaxial compressive stress converts xy plane to rhombus shape and yz plane to rectangular shape. In this way uniaxial stress introduces sheer strain term unlike its biaxial counterpart. Uniaxial straining process is shown in Fig. 2.9.

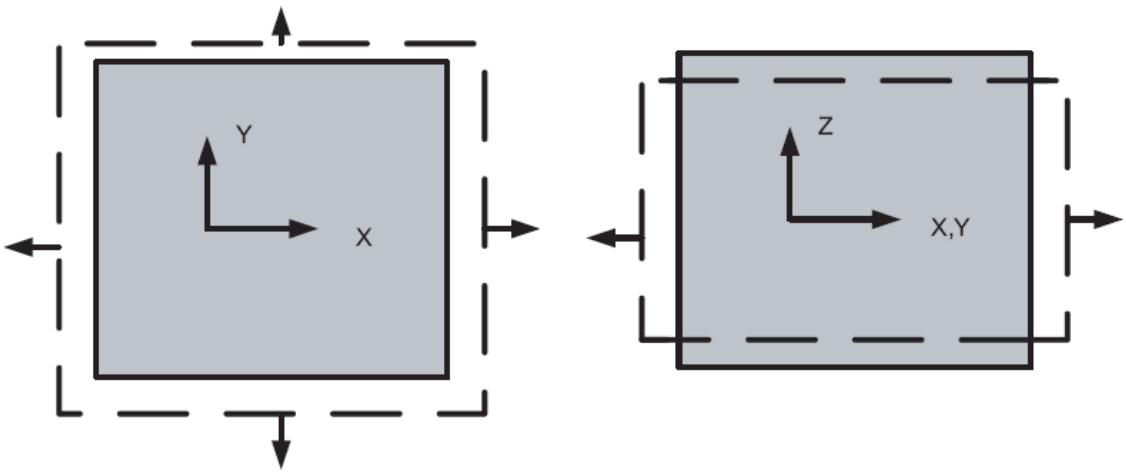

Fig. 2.8: Cubic crystal under in plane tensile biaxial strain

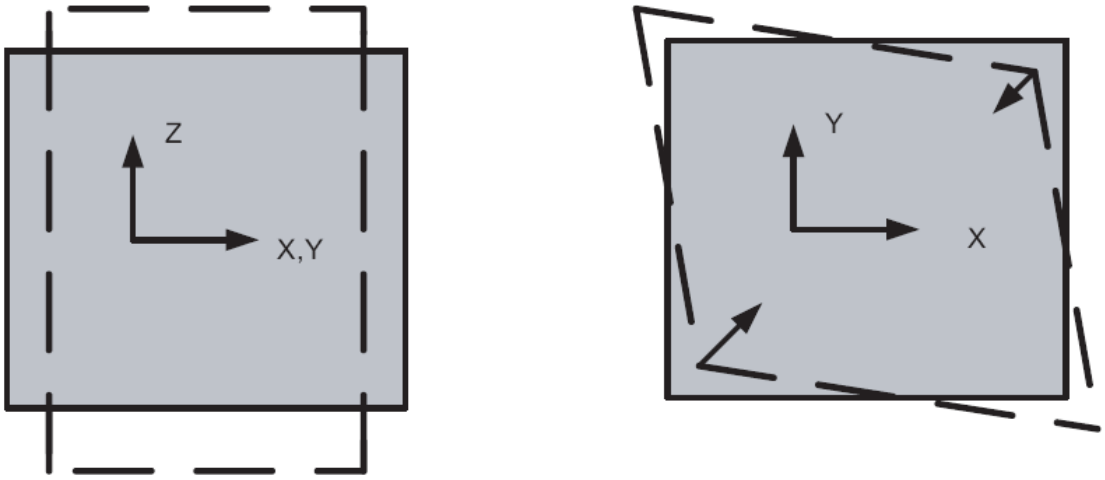

Fig. 2.9: Cubic crystal under uniaxial <100> compressive strain

Stress and strain are related by the following matrix equation,

$$\begin{bmatrix} \in_{xx} \\ \in_{yy} \\ \in_{zz} \\ \in_{yz} \\ \in_{zx} \\ \in_{xy} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{12} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44}/2 & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44}/2 & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44}/2 \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} \qquad (2.64)$$

In equation (2.64) ϵ means applied stress, ζ denotes resulted strain and x, y, z are directions of applied stress and resulted strain. In case of Si, compliance coefficients S_{11}, S_{12} and S_{44} have following values:

$S_{11} = 8.63 \times 10^{-12}\ N^{-1}m^2$

$S_{12} = -2.13 \times 10^{-12}\ N^{-1}m^2$

$S_{44} = 12.49 \times 10^{-12}\ N^{-1}m^2$

In our case, we considered <110> uniaxial stress. Here stress ζ is applied in three different directions. They are given as $\sigma_{xx} = \sigma_{yy} = \sigma_{xy} = \sigma/2$. The sheer strain term σ_{xy}, which modulates conductivity and mobility, makes the difference between uniaxial strain and biaxial strain. The presence of σ_{xy} in uniaxial straining process makes it favorable for higher mobility enhancement.

2.6.2 Change in Band Structure Due to Applied Uniaxial Strain

In bulk silicon, the conduction band can be represented by six equivalent ellipsoids as shown in Fig. 2.10. Ellipsoids 1 and 2 respond with a longitudinal effective mass (m_l) in the gate confinement direction and give rise to unprimed subbands. On the other hand ellipsoids 3 to 6 respond with a transverse effective mass (m_t) in the gate confinement direction, resulting in primed set of subbands. Normally unprimed subbands are more populated by electrons due to their higher effective mass in the direction of applied electric field and thus having lower bound-state energies in the conduction band. Strain changes band structure by lifting the valley degeneracy. For tensile strain, Δ_4 band goes up and Δ_2 moves down, while compressive strain causes Δ_2 to go up and Δ_4 to move down. In case of valence band due to tensile strain LH band goes up and H band moves down. By lifting degeneracy in conduction band and valence band strain changes band gap energy E_g. In Fig. 2.11 change in band structure due to applied tensile strain is shown.

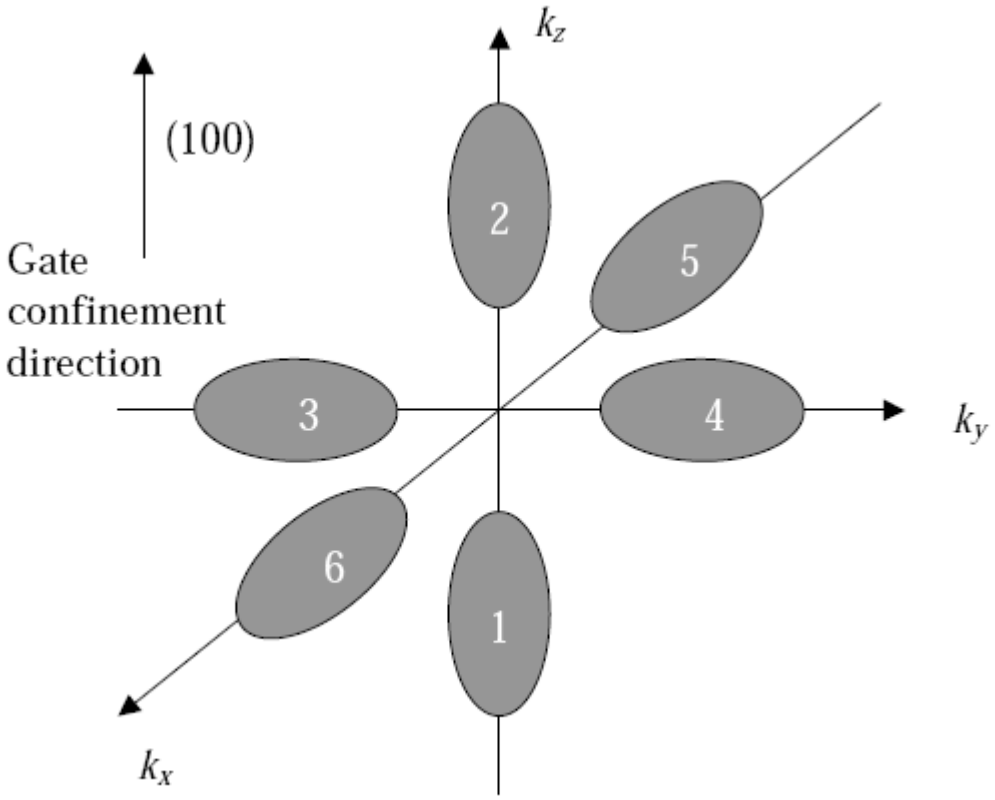

Fig. 2.10: Six fold degeneracy in conduction band of bulk silicon

To model strain effect in MOS devices correctly, the relation between strain and band splitting must be modeled accurately. Though in literature, many expressions showing the effects of strain on band structure are available, all of them are not suitable for all level of stress. In this paper, expressions by Baslev [53] are followed. Effects of uniaxial <110> strain on band splitting can be expressed by following equations:

$$\Delta E_c^2 - \Delta E_c^0 = -\frac{1}{3}(S_{11} - S_{12})\Xi_u P \tag{2.65}$$

$$\Delta E_c^4 - \Delta E_c^0 = -\frac{1}{6}(S_{11} - S_{12})\Xi_u P \tag{2.66}$$

$$\Delta E_c^0 = \Delta E_{g0} - \left|E_{\varepsilon\varepsilon}\right| - \frac{1}{3}\left(S_{11} - S_{12}\right)\Xi_u P \tag{2.67}$$

$$\Delta E_g^0 = \left(\Xi_d + \frac{1}{3}\Xi_u - a\right)\left(S_{11} + 2S_{12}\right)\Xi_u P \tag{2.68}$$

$$\left|E_{\varepsilon\varepsilon}\right| = \frac{1}{2}\left[b^2\left(S_{11} - S_{12}\right)^2 + 3\left(\frac{d}{2\sqrt{3}}S_{44}\right)^2\right]^{\frac{1}{2}}\left|P\right| \tag{2.69}$$

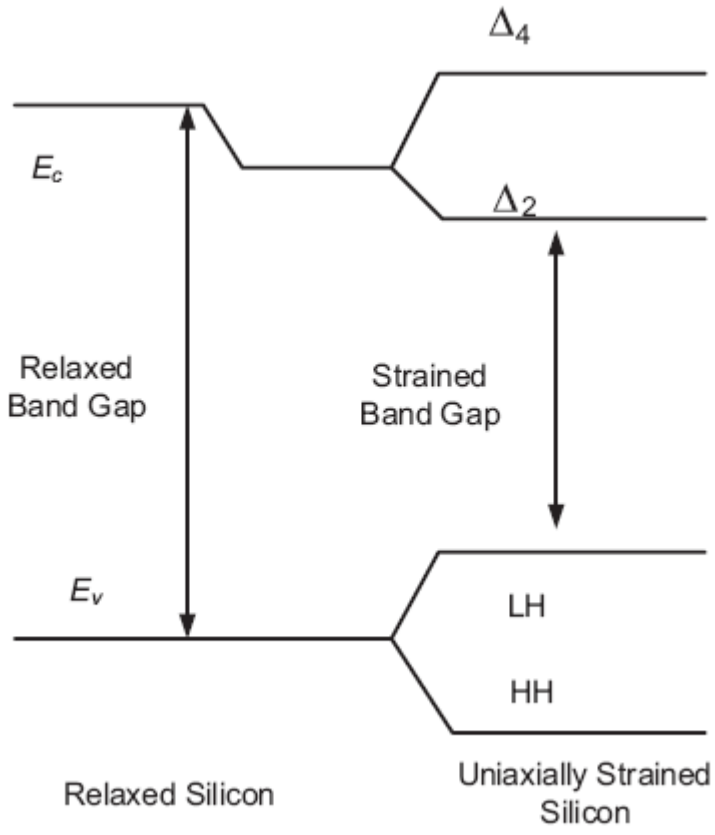

Fig. 2.11: Change in band structure due to applied tensile strain.

Here ΔE_c^0 = Hydrostatic band shifting of the conduction band

ΔE_c^i = Band splitting of the ith valley

ΔE_{g0} = Change in the energy band gap

P = Applied stress

Ξ_u = 8.6 eV

$$\Xi_d + \frac{1}{3}\Xi_u - a = 3.8eV$$

$$|b| = 2.4 \pm 0.2eV$$

$$|d| = 5.3 \pm 0.4eV$$

Equation (2.65) and (2.66) express band splitting in Δ_2 and Δ_4 conduction valleys respectively with respect to the mean position of the conduction band shift. Hydrostatic shift of the mean position of the conduction band can be found by equation (2.67). Equation (2.68) gives the change in band gap energy and finally equation (2.69) shows valence band splitting due to strain. Fig. 2.12 and Fig. 2.13 show how conduction band, valence band and energy gap change with the application of strain.

It is clear that, With tensile strain unprimed valleys (Δ_2) go to lower energy, where primed valleys (Δ_4) move to higher energy levels. Thus strain lifts degeneracy in the conduction band, which results in more electron population in the unprimed energy bands. Splitting of valence band and decrease in energy gap shown in Fig. 2.13 reveals that, carrier concentration is higher in uniaxially strained Si devices than relaxed Si devices. By increasing carrier concentration strain causes electron mobility to increase significantly.

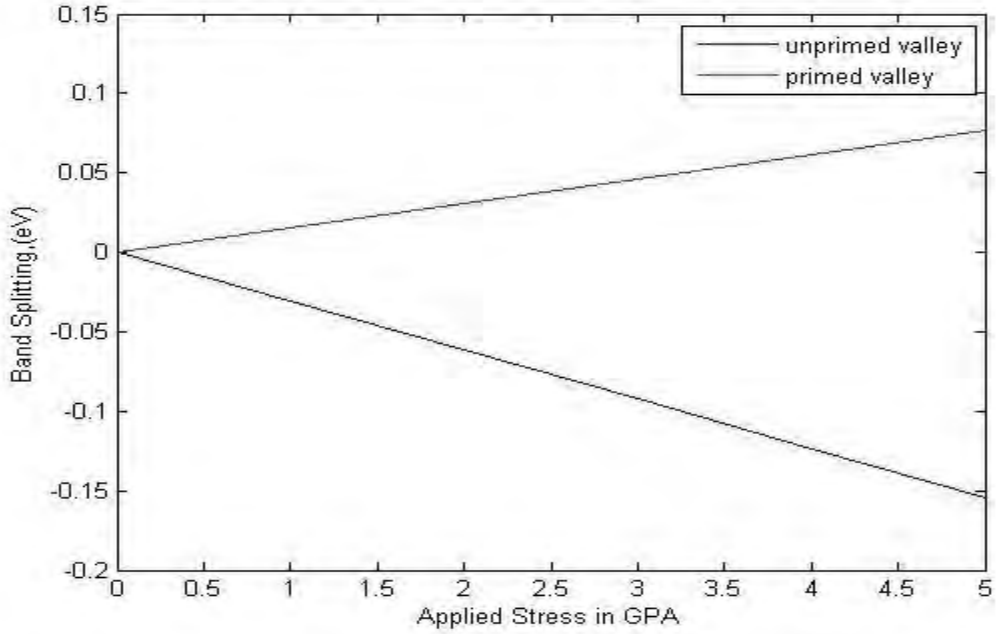

Fig. 2.12: Splitting of conduction band in silicon with the application of tensile strain.

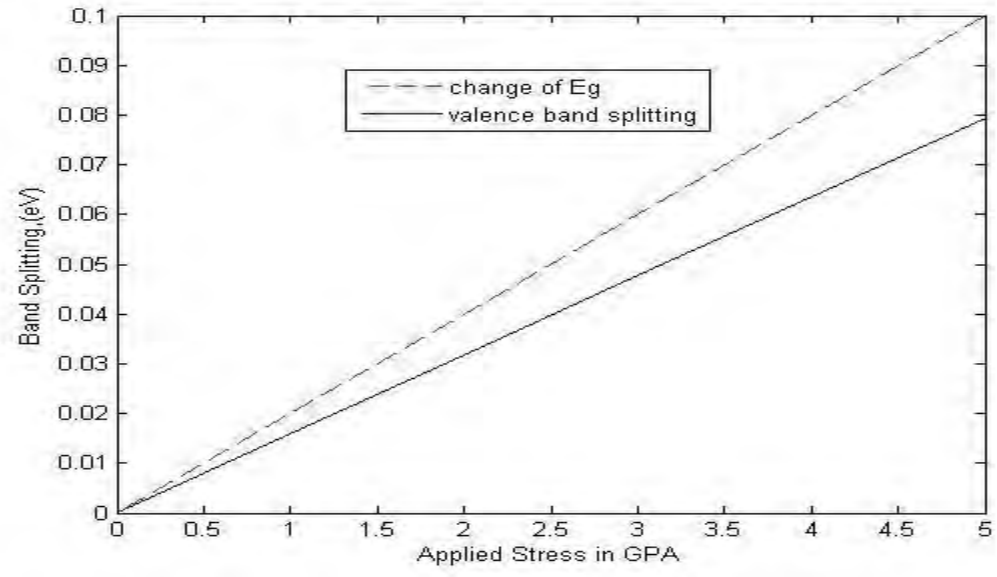

Fig. 2.13: Splitting of valence band and change in energy gap in silicon with the application of tensile strain.

2.6.3 Effect of Tensile Strain on Effective Mass

Strain changes effective mass of silicon by changing the curvature of energy diagram. Both quantization effective mass and density of state effective mass experience variations with the application of tensile strain. Here the relationships of effective masses and applied stress are presented according to Dhar [55].

$$m_x = 0.918 + 0.0236X^2 \tag{2.70}$$

$$m_y = 0.196 - 0.016X \tag{2.71}$$

$$m_z = 0.196 + 0.029X \tag{2.72}$$

In the above equations, m_x, m_y and m_z are effective masses in three crystal directions, 100, 010 and 001 respectively. Quantization and density of state effective masses can be derived by the following equations,

$$m_{d1} = \sqrt{m_y m_z} \tag{2.73}$$

$$m_{z1} = m_x \tag{2.74}$$

$$m_{d2} = \sqrt{m_x m_y} \tag{2.75}$$

$$m_{z2} = m_z \tag{2.76}$$

In the above equations, m_{d1} and m_{z1} are density of state and quantization effective masses for Δ_2 conduction band valley, where m_{d2} and m_{z2} are that for Δ_4 conduction band valley. Fig. 2.14 and Fig. 2.15 show change in quantization effective mass and in density of state effective mass with applied tensile stress given to nMOS device. Fig. 2.16 shows the effect of tensile strain on conduction mass.

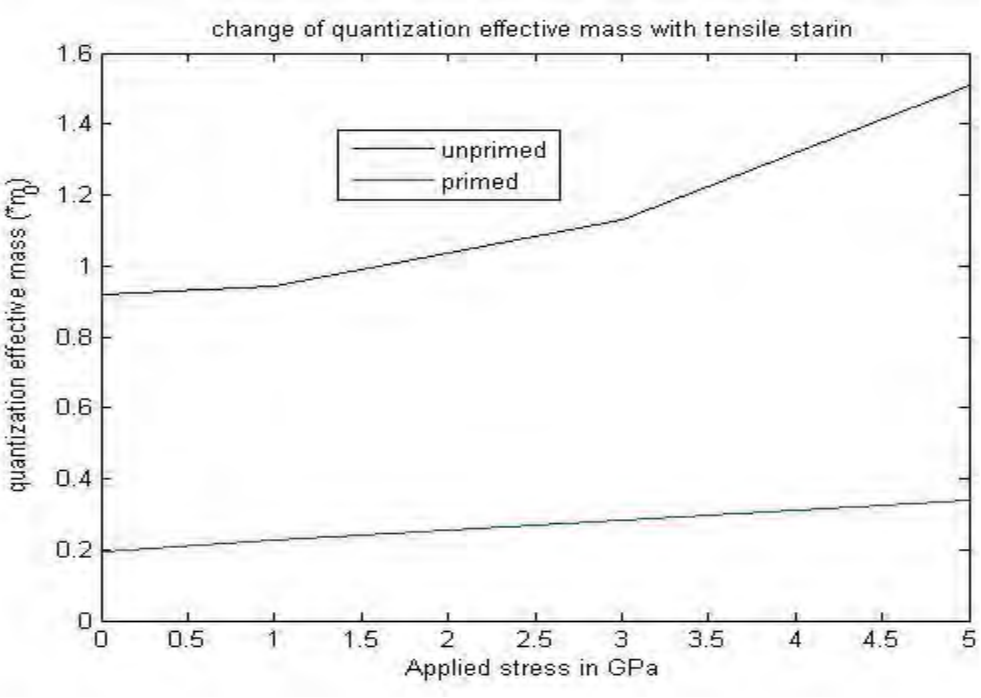

Fig. 2.14: Effect of tensile stress on quantization effective mass

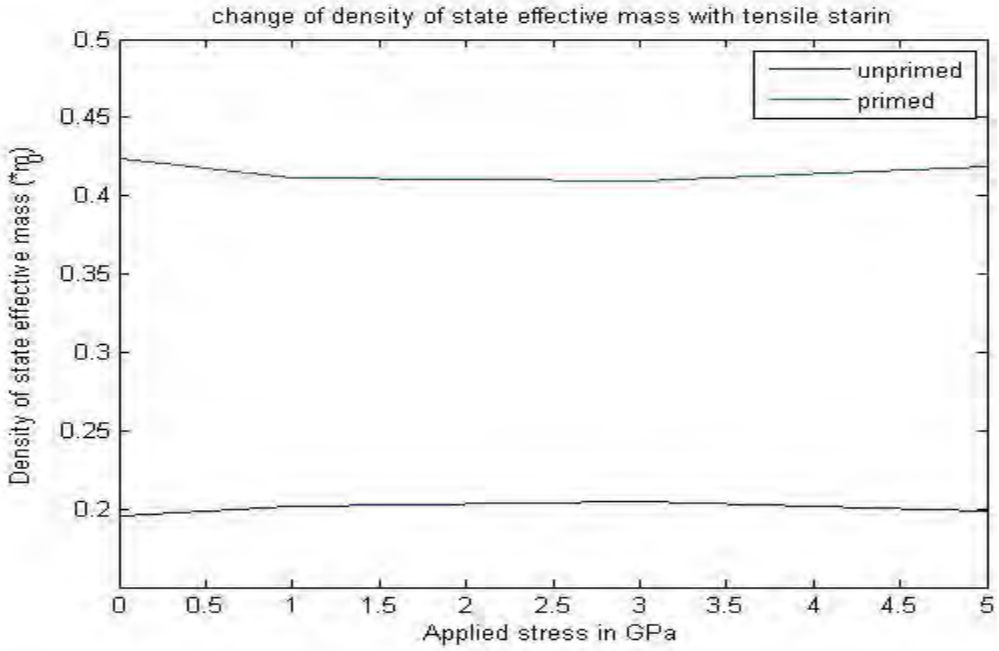

Fig. 2.15: Effect of tensile stress on density of state effective mass

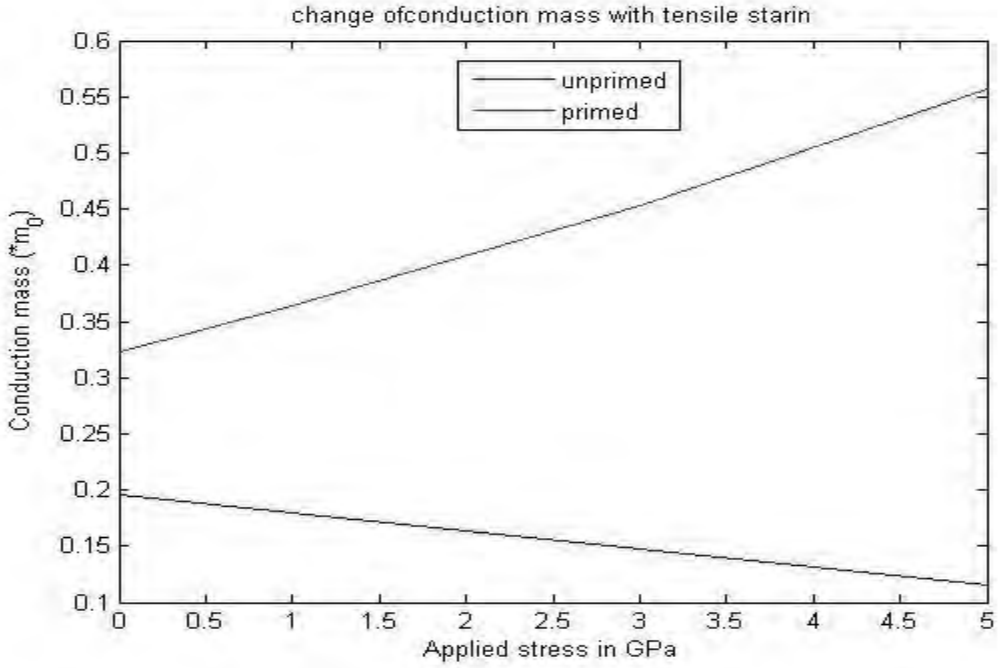

Fig. 2.16: Effect of tensile stress on conduction mass

Change in effective masses cause change in eigenenergies and in charge distribution. Mobility depends on charge distribution in the subbands. So, mobility calculation should incorporate the effect of strain on effective masses. By changing bandgap energy Eg, strain changes the intrinsic carrier concentration from its relaxed value of $1.5\times10^{10} cm^3$ as,

$$N_i = 1.5\times10^{10} \times \exp \Delta E_g \tag{2.77}$$

In this work both band splitting and effective mass variations are incorporated according to the above expressions.

2.7 Proposed Drain Current Model for Double gate Uniaxially Strained Silicon MOSFET

Equation (2.8) gives the expression of drain current for symmetric double gate MOSFET with undoped or lightly doped silicon body and equation (2.3) states the boundary condition to calculate the intermediary parameter β, which is a function of the quasi-Fermi potential V at a point along the channel. Short channel effect is modeled by including threshold voltage shift $(\Delta V_t)_{SCE}$ from equation (2.25) and subthreshold slope is obtained from equation (2.27). Equation (2.33) and (2.34) give expressions for threshold voltage shift due to quantum mechanical effect, (ΔV_t^{QM}) and change in inversion layer thickness δt_{inv} as a parameter to model gate capacitance degradation due to quantum mechanical effect. Equation (2.65) – equation (2.69) show changes in band structure of silicon due to tensile strain, whereas equation (2.70) – equation (2.76) represent effective mass variation with applied strain.

By changing energy gap, strain changes intrinsic carrier concentration, which is given by equation (2.77).

Considering the effect of strain and quantum mechanical effect, band shifting in the conduction band is given by

$$\Delta E_c = \frac{(\hbar\pi)^2}{2m_0 t_{Si}^2}\left(\frac{1}{m_{z1}} - \frac{1}{m_{z2}}\right) + \Delta E_{c0} \tag{2.78}$$

where m_{z1} and m_{z2} are given by equation (2.74) and (2. 76) and ΔE_{c0} is given by equation (2.67).

Total threshold voltage shift is given by

$$\Delta V_t = \frac{\Delta E_c}{q} + (\Delta V_t)_{SCE} \tag{2.79}$$

For uniaxially strained double gate MOSFET, the boundary condition for obtaining intermediary parameter β is given by

$$\frac{q(V_g - \Delta\varphi - \Delta V_t - V)}{kT} - \ln\left[\frac{2}{t_{Si}}\sqrt{\frac{2\varepsilon_{Si}kT}{q^2 n_i}}\right] = \ln\beta - \ln[\cos\beta] + \frac{2\varepsilon_{Si}t_{ox}}{\varepsilon_{ox}t_{Si}}\beta\tan\beta \tag{2.80}$$

By including all these effects discussed above, the equation for drain current is

$$I_{ds} = \mu_{strained}\frac{W}{L_e}\frac{4\varepsilon_{Si}}{t_{Si}^{QM}}\left(\frac{2kT}{q}\right)^2 \times \left[\beta\ \tan\beta - \frac{\beta^2}{2} + \frac{\varepsilon_{Si}(t_{ox} + (12/45)\delta t_{inv})}{\varepsilon_{ox}t_{Si}^{QM}}(\beta\tan\beta)^2\right]_{\beta_d}^{\beta_d} \tag{2.81}$$

where, $\mu_{strained}$ can be obtained from equation (2.55) by carrying out the changes in effective masses and energy gap due to applied strain in the mobility model. t_{Si}^{QM} is obtained by considering the change in the inversion layer thickness due to quantum mechanical effects. L_e is obtained by considering channel length modulation given by equation (2.63). Velocity saturation effect is considerable when $V_D > V_{DSAT}$. Due to velocity saturation mobility will be changed which is made according to equation (2.62).

Chapter 3

Simulations and Results

In this chapter simulations using the drain current model are given with physical explanation. Ids-Vgs for double gate MOSFET is given in both linear and logarithmic scales. Drain currents for various levels of strain up to practical limit are presented. Uniaxial strain is given in <110> direction for its wide practical use. Although stress can be given in other directions but for uniaxial straining process mobility enhancement occurs in maximum proportion if stress is applied in <110> direction. Mobility enhancement with the application of strain is explained. The implemented model with quantum mechanical effects and short channel effect is validated by reported experimental data.

3.1 Comparison of The Drain Current Model with Experimental Data for Relaxed Silicon Double Gate MOSFET

Figure 3.1 and Fig 3.2 shows the comparison of I_{ds} vs V_{gs} for double gate MOSFET with relaxed silicon for a low drain bias using the developed model and reported experimental data in linear scale and logarithmic scale respectively. Here silicon thickness T_{si}=30 nm, oxide thickness, T_{ox}= 2.2 nm, oxide material is SiO_2. A midgap metal gate with metal to semiconductor work function difference $\Delta\phi = -46mV$ is used for gate contact. For undoped symmetric double gate MOSFET, Fig. 3.1 and 3.2 show excellent agreement of our model with reported experimental data. For experimental data, the 30-nm thick undoped FinFET was fabricated with < 110 > channel orientation on an SOI substrate [30]. The height of the fins is 60 nm, the gate length 10μm, and the number of fins 20. TiSiN tensile metal gate with midgap workfunction is deposited on 2 nm thick oxide [62]. From the extracted data, L_{eff} for our model is 72.2 nm and W_{eff} is 167. 6nm.

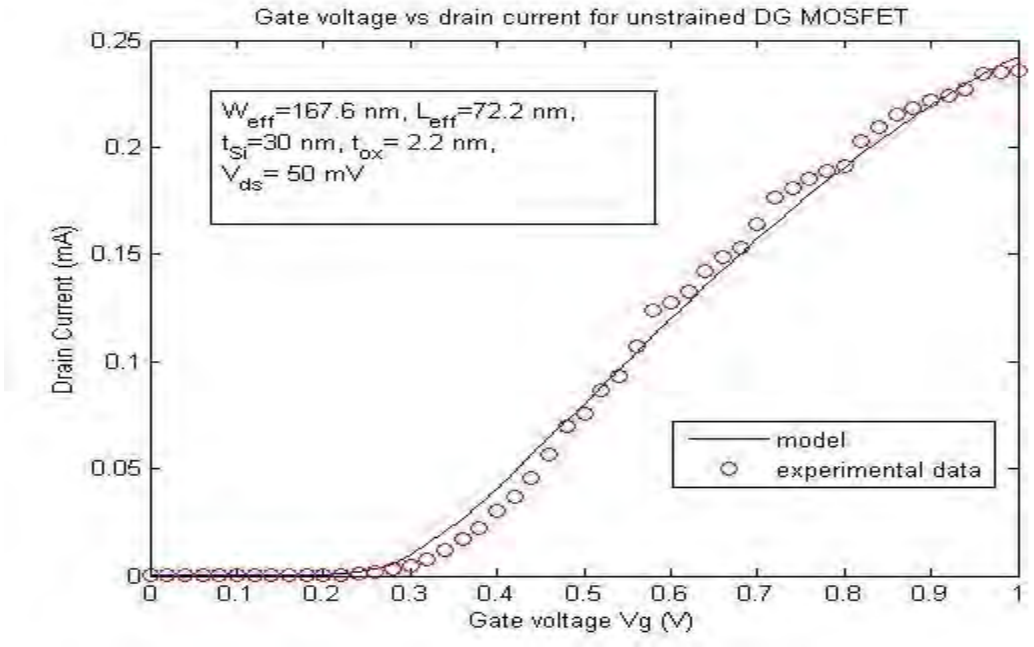

Fig. 3.1: Gate voltage vs drain current (linear scale) for relaxed silicon DG MOSFET with low drain bias (V_{ds}=50 mV)

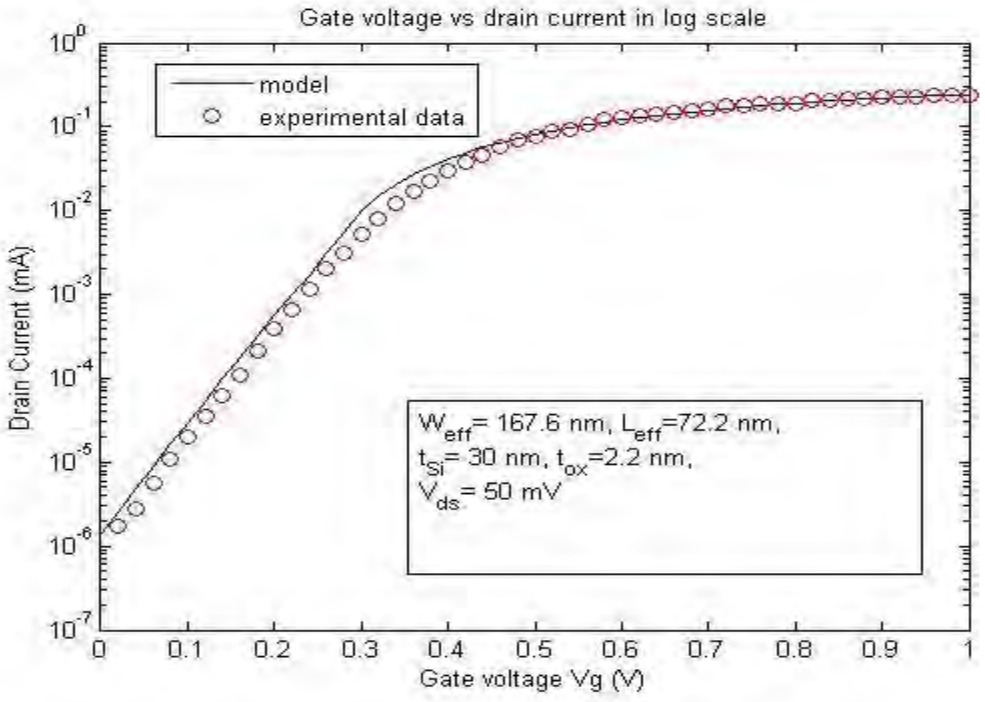

Fig. 3.2: Gate voltage vs drain current (logarithmic scale) for relaxed silicon DG MOSFET with low drain bias (V_{ds}= 50 mV)

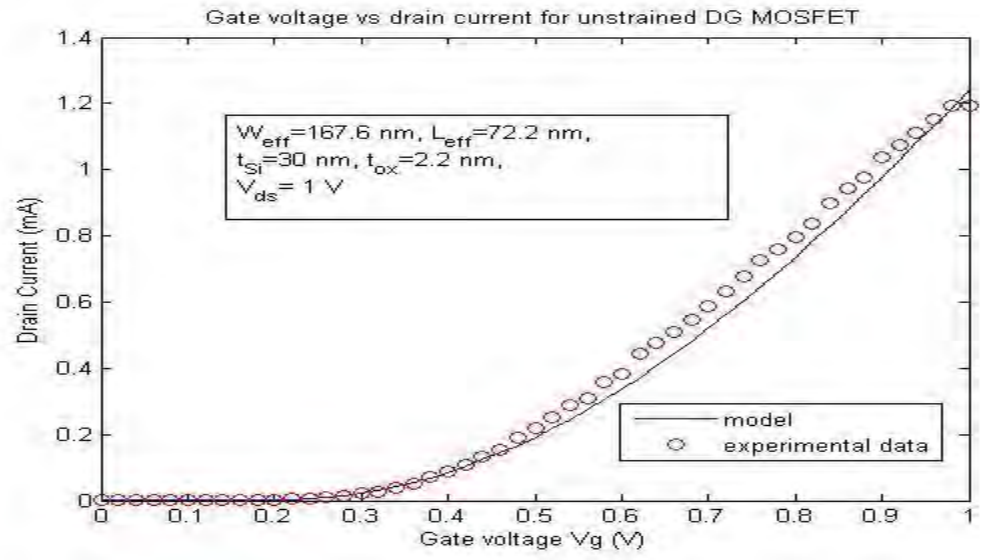

Fig. 3.3: Gate voltage vs drain current (linear scale) for relaxed silicon DG MOSFET with high drain bias (V_{ds}=1 V)

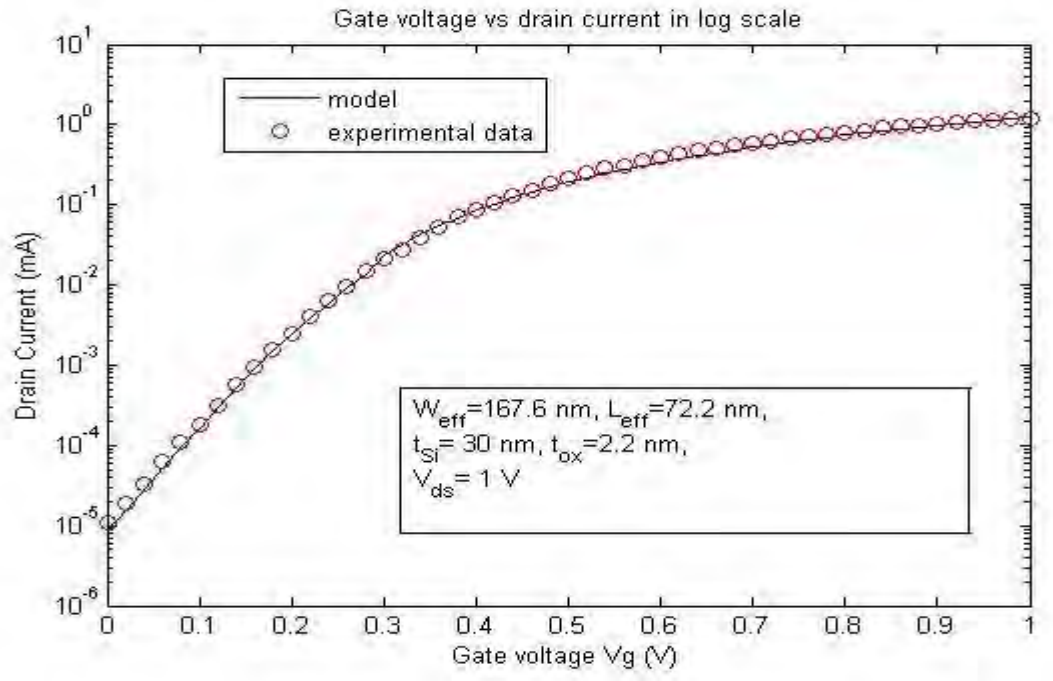

Fig. 3.4: Gate voltage vs drain current (logarithmic scale) for relaxed silicon DG MOSFET with high drain bias (V_{ds}=1 V)

Fig. 3.3 and 3.4 validates our model for high drain bias. Here same device parameters are considered for V_{ds}= 1V.

3.2 Drain Current Change Due to Uniaxial Strain.

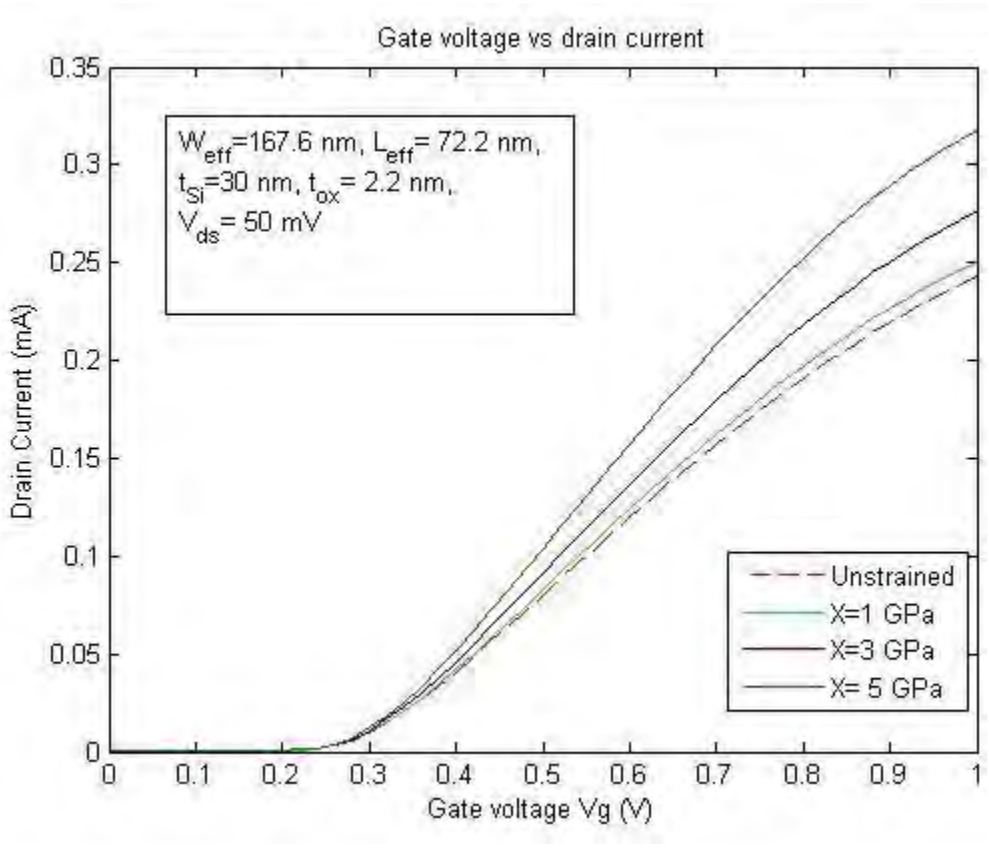

Fig. 3.5: Gate voltage vs drain current (linear scale) for relaxed and strained Si DG MOSFET with V_{ds}= 50 mV

Fig. 3.5 and Fig. 3.6 show drain current for relaxed and strained Si devices with low drain bias in linear scale and logarithmic scale respectively. Change due to strain as a percent of drain current for relaxed Si device is shown in Fig. 3.7. It is seen that with low drain bias strain can change drain current up to about 30% of drain current without strain.

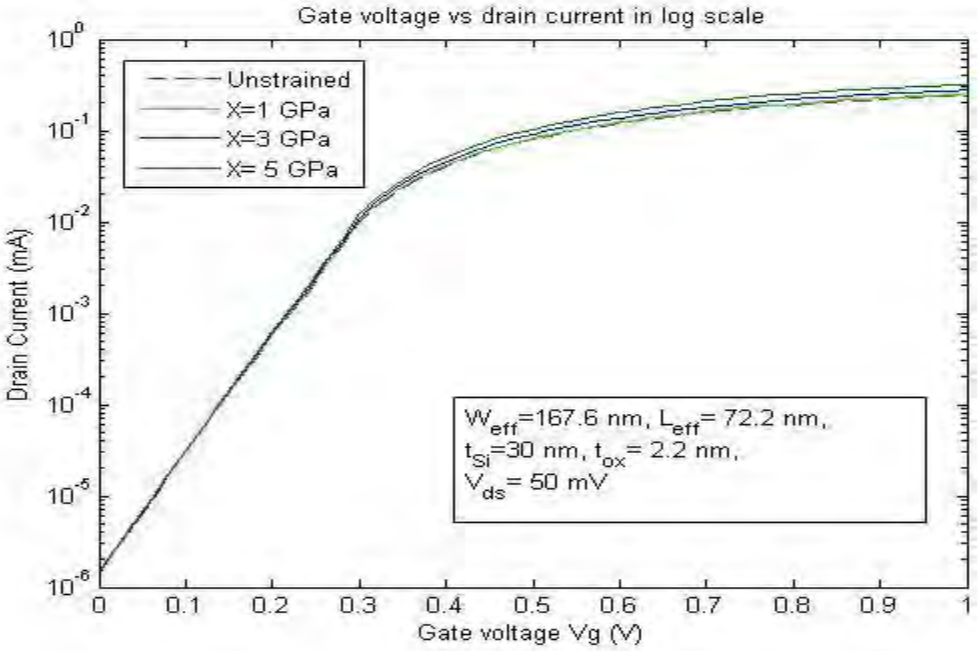

Fig. 3.6: Gate voltage vs drain current (logerithmic scale) for relaxed and strained Si DG MOSFET with V_{ds}= 50 mV

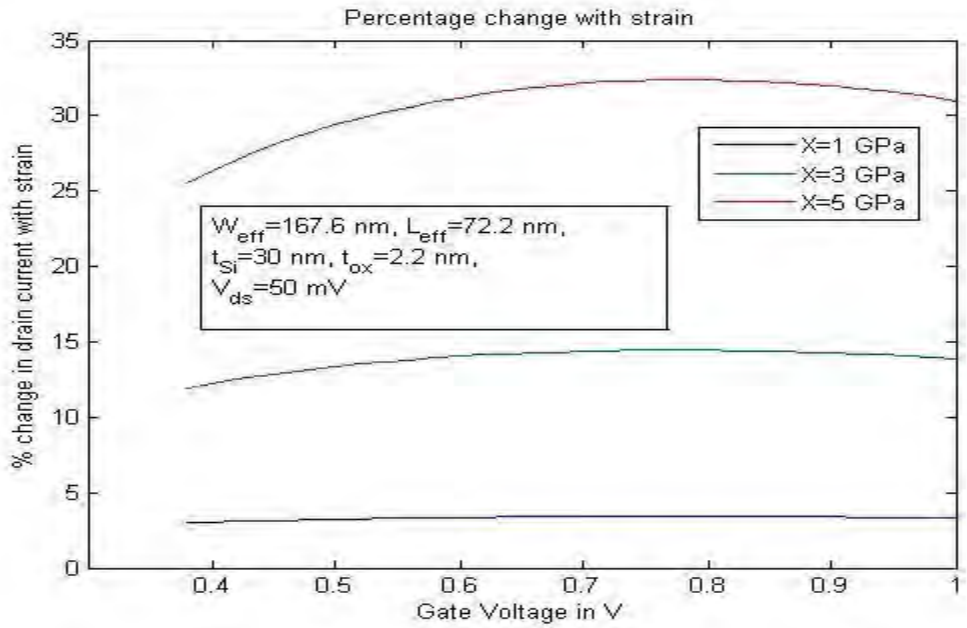

Fig. 3.7: Gate voltage vs percentage change in drain current with strain for DG MOSFET with V_{ds}= 50 mV

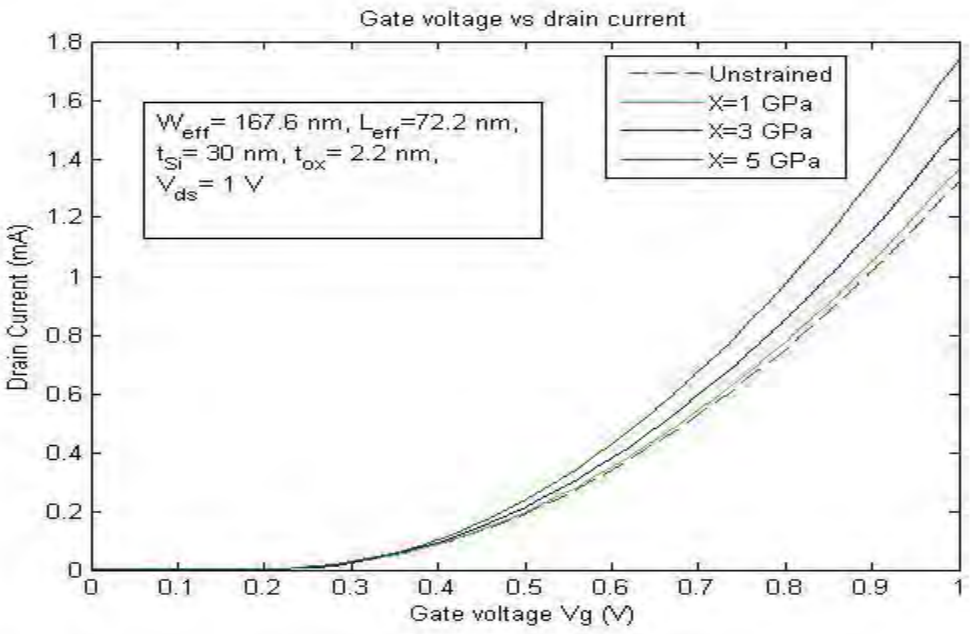

Fig. 3.8: Gate voltage vs drain current (linear scale) for relaxed and strained Si DG MOSFET with V_{ds}= 1V

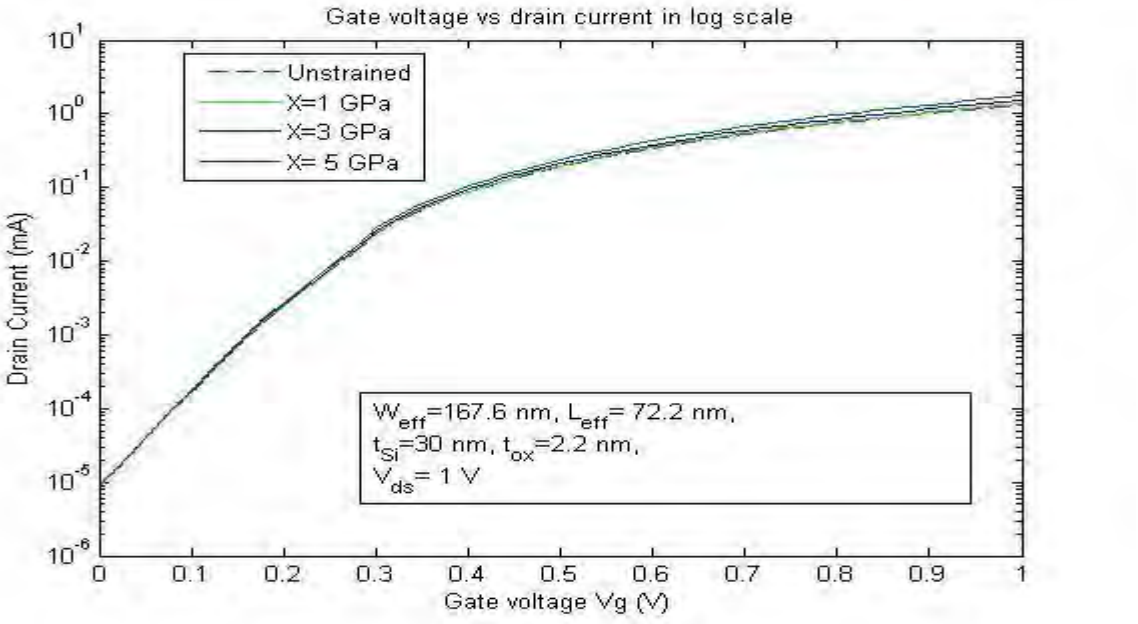

Fig. 3.9: Gate voltage vs drain current (logerithmic scale) for relaxed and strained Si DG MOSFET with V_{ds}= 1V

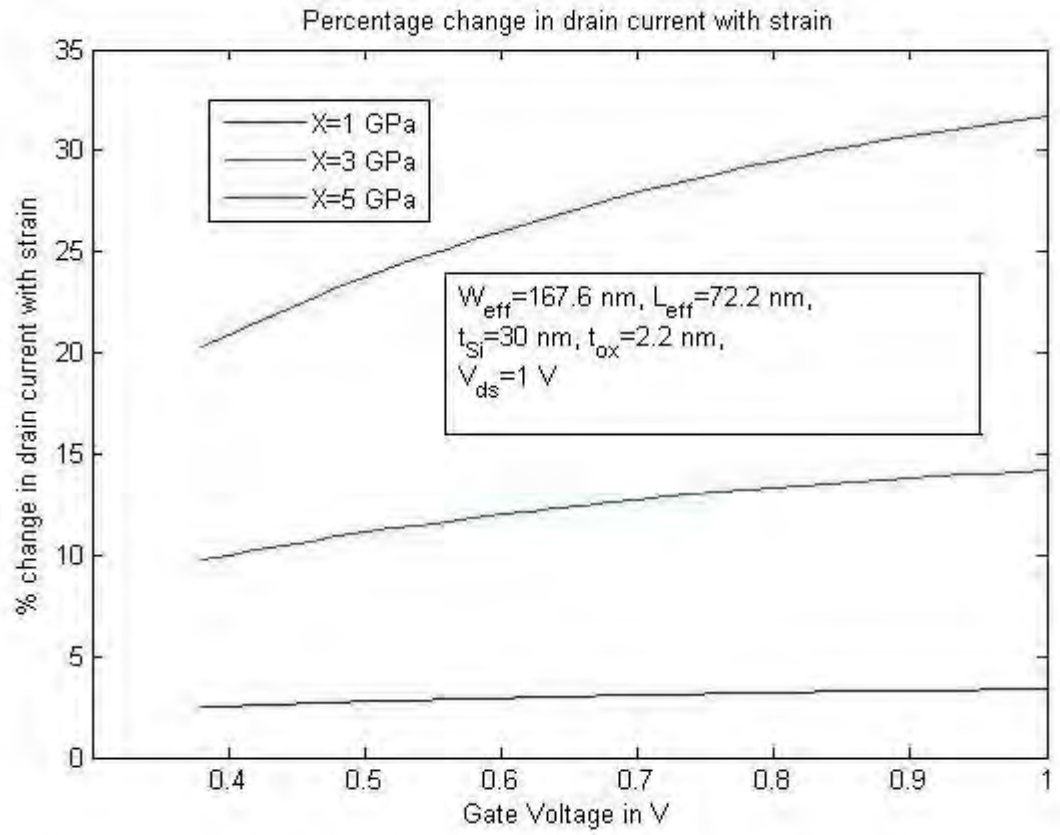

Fig. 3.10: Gate voltage vs percentage change in drain current with strain for DG MOSFET with V_{ds}= 1V

Using high drain bias percentage change in drain current due to strain is somehow same as that using low drain bias, which is clear from Fig. 3.8, Fig. 3.9 and Fig. 3.10.

3.3 Mobility Change with Uniaxial Strain

Strain causes change in mobility in the channel of MOSFET. Due to change in mobility drain current increases with the application of tensile strain. Following figures show gate voltage vs effective mobility in the channel of DG MOSFET for both low (50 mV) and high (1V) drain bias.

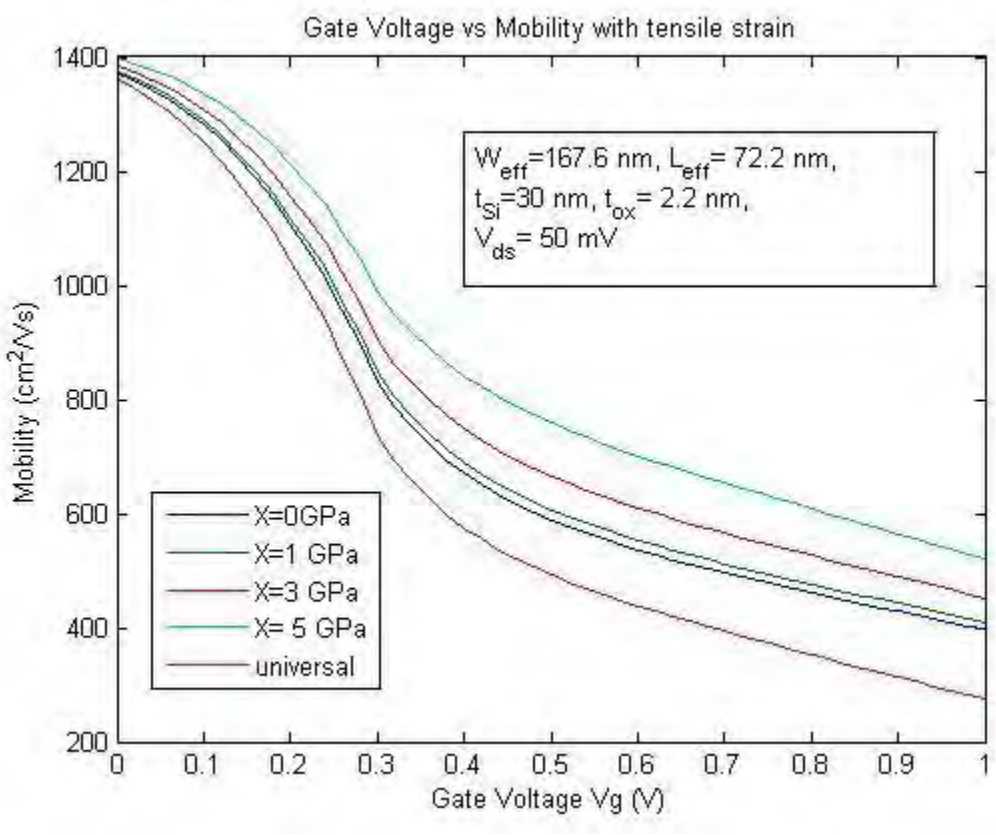

Fig. 3.11: Gate voltage Vs Mobility in relaxed and strained Si DG MOSFET with V_{ds} = 50 mV

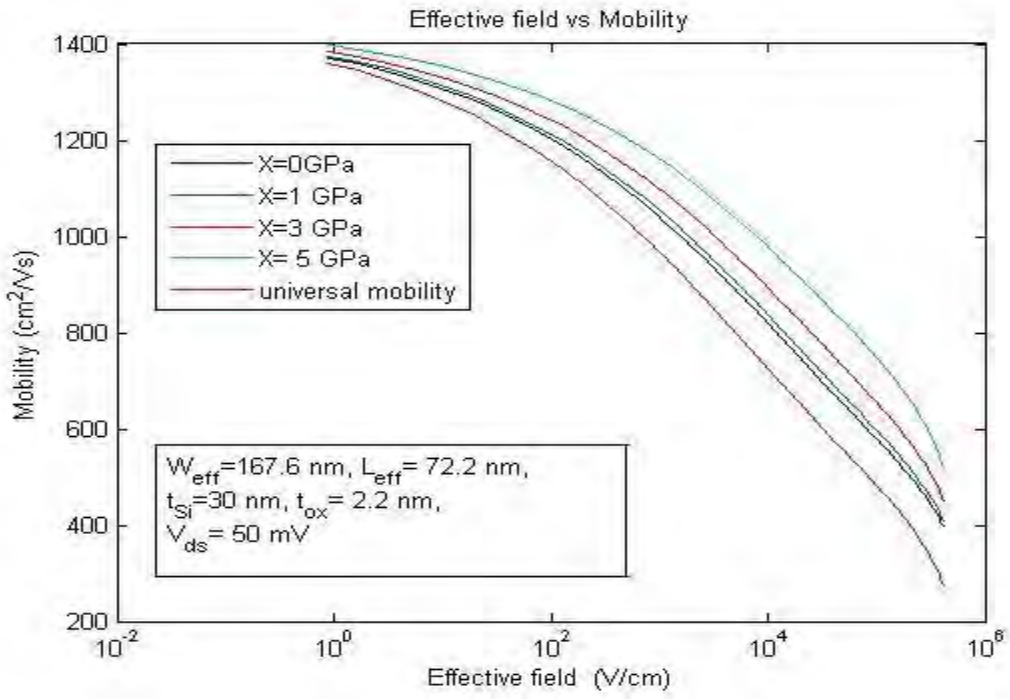

Fig. 3.12: Effective field vs Mobility in relaxed and strained Si DG MOSFET with V_{ds}= 50 mV

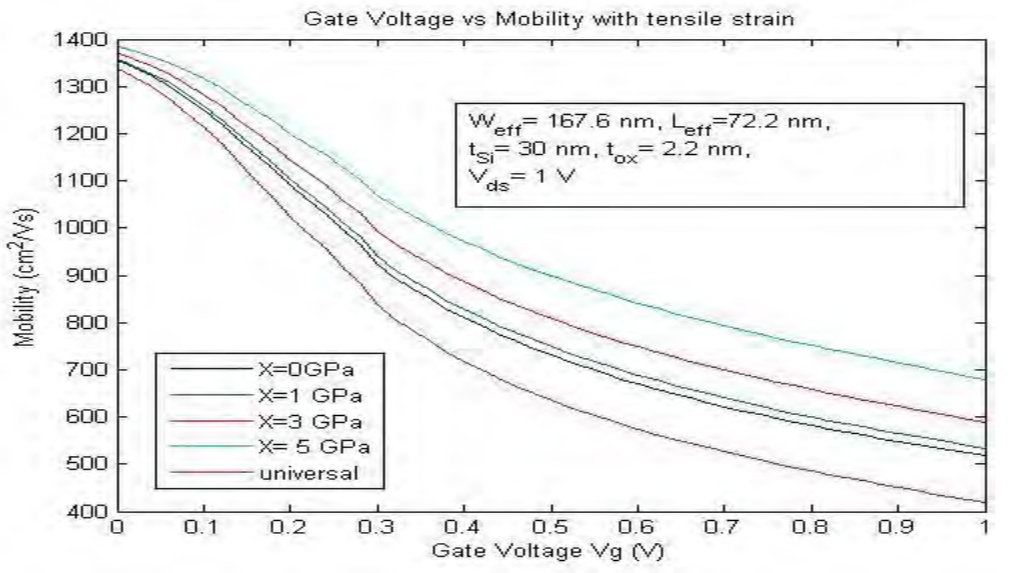

Fig. 3.13: Gate voltage Vs Mobility in relaxed and strained Si DG MOSFET with V_{ds} = 1V

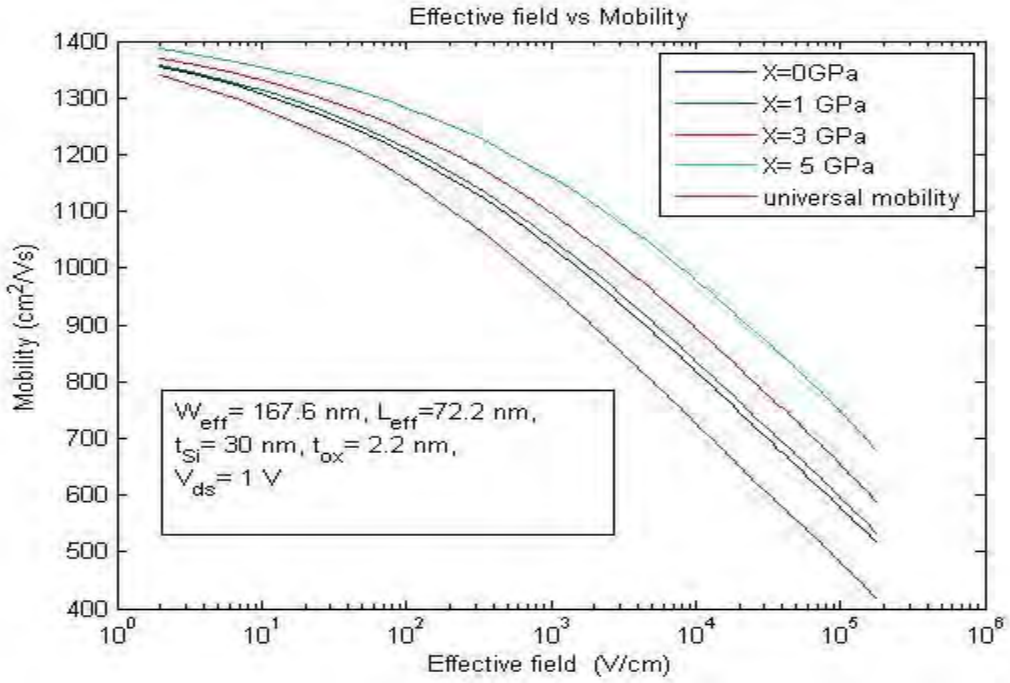

Fig: 3.14: Effective field vs Mobility in relaxed and strained Si DG MOSFET with V_{ds}= 1 V

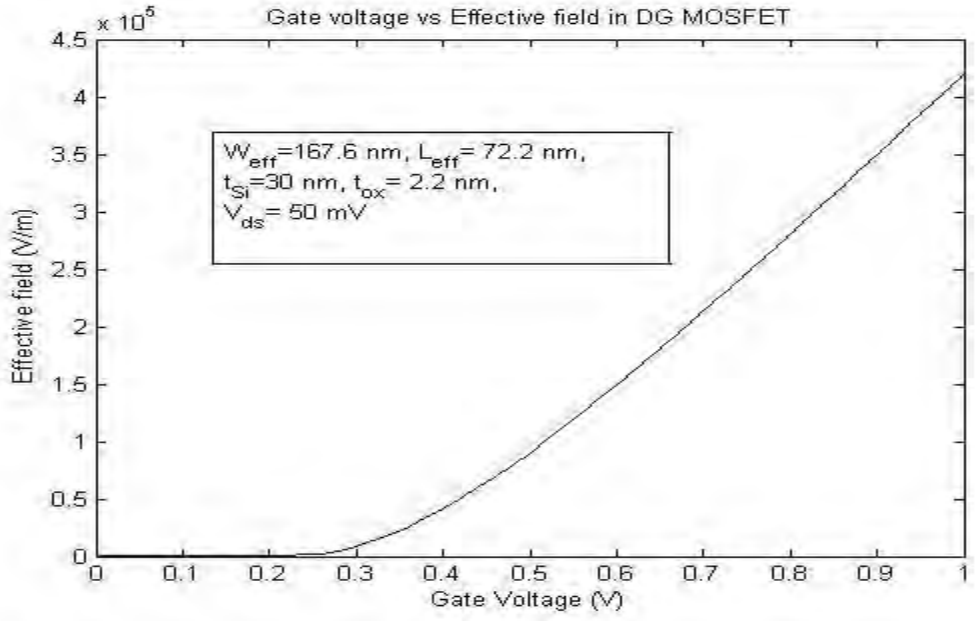

Fig. 3.15: Gate voltage vs Effective field in the channel with V_{ds}= 50 mV

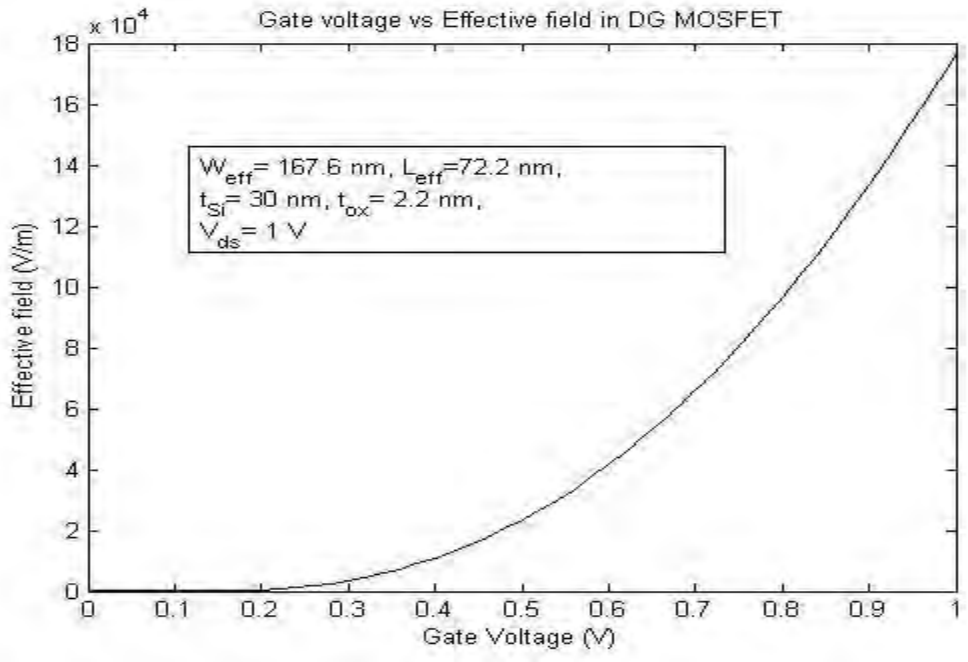

Fig. 3.16: Gate voltage vs Effective field in the channel with V_{ds}= 1V

With high drain bias inversion charge (Q_{inv}) in the channel reduces, resulting in lower effective field. As mobility decreases with effective field, we see that, using high drain bias mobility tends to increase slightly. In our work we used a low field mobility model. The effective mobility is also compared with universal mobility according to the model described by Takagi [31], [32].

To understand the physics behind mobility change due to strain, change in effective mass and band gap with strain were discussed in chapter 2. Uniaxial strain changes the curvature of the energy diagram and causes changes in all the effective masses. For unprimed subbands conduction mass decreases with strain, while for primed subbands, strain increases conduction mass. Also strain causes Δ_4 valleys to move up and Δ_2 valleys to move down. As a results more electrons moves to Δ_2 valleys due to lower subband energy.

Chapter 4

Conclusion

4.1 Contributions of The Work

- An accurate drain current model for double gate MOSFET is developed and a drain current model for double gate uniaxilly strained silicon MOSFET is proposed.
- Quantum mechanical effects, Short channel effects and velocity saturation effects are successfully incorporated in the model.
- Change in effective mass and band gap energy due to strain are included in the proposed model.
- I_{ds}- V_{gs} characteristics are simulated for both high and low drain bias.
- Results using model for double gate MOSFET with relaxed silicon body are compared with reported experimental data.
- Uniaxial strain is given in < 110 > direction for its wide practical use.
- In this work, effect of strain is observed up to 5 GPa of strain which is the practical limit for uniaxial stress.
- Percentage changes in drain currents with strain are reported using the proposed drain current model for double gate uniaxillay strained silicon double gate MOSFET.

4.2 Conclusion

Uniaxial straining technique is quite new and effective one to enhance carrier mobility to a great percentage than other conventional techniques. I-V characteristics of double gate uniaxially strained Si MOSFET is very important for understanding the output characteristics of this device. Using this model more accurate result is possible with less complexity. Detail explanation of drain current change due to strain is given. It has been seen that change due to strain is more above threshold voltage and it remains same for low and high drain bias. It is also observed that, effective mass change plays the main role in drain current change in the inversion region. Inclusion of velocity saturation effect and channel length modulation made the model highly accurate. Mobility model used in our work can account change in mobility due to silicon thickness fluctuations accurately. Threshold voltage shift and gate capacitance degradation due to quantum mechanical effect are modeled according to the literature.

4.3 Suggestion for Future Works

In this work, drain current model for symmetric double gate MOSFET using uniaxially strained Si body is discussed. Similarly for other multiple gate MOSFETs drain current model can be made for strained Si body. Because of the highly symmetric nature of SDG MOSFET, Poisson's equation can be reduced to a 1-D ordinary differential equation in Cartesian co-ordinates. Gate All Around MOSFET has also symmetric nature, and we can reduce Poisson's equation to a 1-D ordinary differential equation in cylindrical co-ordinate and can construct an analytical drain current model. The effect of strain can also be examined for gate all around MOSFET.

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