BACHELOR OF SCIENCE IN ELECTRONIC AND TELECOMMUNICATION ENGINEERING

Design a 4x4 Multiplier Circuit using Quantum Dot Cellular Automata with Binary Parallel Adder

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ABSTRACT

In Today's world, electronic circuits are being minimized day by day. CMOS technology has reached its peak level, which means transistors size can't be smaller anymore along with power consumption; delay time can't be decreased, and so on. In this case, we suggest an invention of Nano-technology named Quantum-dot Cellular Automata (QCA), another Nano-scale model for substituting traditional Complementary Metal–Oxide Semiconductor (CMOS) innovation. It is a transistor less paradigm by which we can decrease the sudden heat & power density of electronic circuits. This paper presents the 4*4 multiplier design by using a binary parallel adder with QCA. We have achieved a QCA Multiplier in which cell count has been decreased. The cell count of our proposed design is less than 2750 compared to the coplanar multiplier and the delay time is less than 8, and the area is less than 5.5 μm2. It may be utilized in digital signal processing applications and design calculators, mobiles, processors, or image processors that use digital signal processing. QCA Designer 2.3.0 was used to building and test the circuit, and the Coherence vector engine was utilized to simulate it.

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List of Abbreviation

THz	Tera Hertz
SET	Single Electron Transistor
RTD	Resonant Tunneling Diodes
MV	Majority Voter
MV3	Three Inputs Majority Voter
MV5	Five Inputs Majority Voter
MV7	Seven Inputs Majority Voter
E_k	Kink Energy
RCA	Ripple Carry Adder
CFA	Carry Flow Adder
CLA	Carry Look Ahead
QCA	Quantum Dot Cellular Automata
CMOS	Complementary Metal Oxide Semiconductor
CF CMOS	Cost Function CMOS
CF QCA	Cost Function QCA
KPI	Key Performance Indicators
CC	Cell Count
NG	No. of Gates
CO	Crossover
D	Delay
ML	Multilayer
CP	Coplanar
CZ	Clock Zone
CS	Clocking Scheme
SR	Set/Reset

Chapter 1

INTRODUCTION

1.1 Background

A quantum dot Cellular automation is a proposed invention in electronics after CMOS technology. It is a transistor-less design that allows an electronic circuit's abrupt heat and power density to be decreased. CMOS technology has achieved its pinnacle, which means that transistor sizes, power consumption, and delay time cannot be reduced any further. This age enters the world of quantum mechanics when transistors reach the Nano-scale. The traditional behaviours of matter and energy are different at such small scales. [1] Electron tunnelling is a quantum phenomenon that affects the performance of Nano transistors. When materials are extremely thin (less than a nanometer), electron tunnelling is similar to teleportation because electrons can pass directly through them. That is why today's world is focusing on new technology, one of which is QCA, which will make the road in electronics easier. QCA offers some unique characteristics, such as low power consumption, exceptionally high density, and quick operation speed. QCA passed all of the required testings to become a viable electronics technology for the future. [2]

1.2 History of Electronic Circuits

A vacuum diode was invented in 1897 by J.A. Fleming, while a vacuum triode was developed in 1902 by Lee De Forest to boost electrical impulses. During World War II, the tetrode and pentode tubes came to dominate the electronic industry throughout the world. The transistor era began in earnest in 1948 with the development of the junction transistor. Despite being a Nobel laureate, this device was ultimately supplanted by a massive vacuum tube that required enormous electricity to function. Germanium and silicon semiconductor materials were utilized in different electronic circuits to make these transistors prominent and widely accepted. Electronic devices have become more affordable, smaller, and lighter as a direct result of the invention of integrated circuits (ICs). It was possible to fit nearly a thousand components on a single chip between 1958 and 1975 with the introduction of small-scale integration, medium-large integration, and very large integration ICs. JFETS and MOSFETs, created between 1951 and 1958 and enhanced the device design process

and made more dependable and powerful transistors, maintained the trend. Digital integrated circuits, like analogue ICs, were game-changers in computer architecture. It was necessary to employ transistor-transistor logic (TTL) and I2L and ECL technologies to construct these ICs. Further development of these digital integrated circuits (ICs) utilized PMOS, NMOS, and CMOS manufacturing techniques. [3]A vacuum diode was invented in 1897 by J.A. Fleming, while a vacuum triode was developed in 1902 by Lee De Forest to boost electrical impulses. During World War II, the tetrode and pentode tubes came to dominate the electronic industry throughout the world. The transistor era began in earnest in 1948 with the development of the junction transistor. Despite being a Nobel laureate, this device was ultimately supplanted by a massive vacuum tube that required enormous amounts of electricity to function. Germanium and silicon semiconductor materials were utilized in different electronic circuits to make these transistors prominent and widely accepted. Electronic devices have become more affordable, smaller, and lighter as a direct result of the invention of integrated circuits (ICs). It was possible to fit nearly a thousand components on a single chip between 1958 and 1975 with the introduction of small-scale integration, medium-large integration, and very large integration ICs. JFETS and MOSFETs, created between 1951 and 1958 and enhanced the device design process and made more dependable and powerful transistors, maintained the trend. Digital integrated circuits, like analogue ICs, were game-changers in computer architecture. It was necessary to employ transistor-transistor logic (TTL) and I2L and ECL technologies to construct these ICs. Further development of these digital integrated circuits (ICs) utilized PMOS, NMOS, and CMOS manufacturing techniques. [3]

1.3 Why Technology is Shifting from CMOS to QCA

Due to scaling down the device to nanoscale dimensions and many quantum processes affecting the CMOS parameter values, performance might be reduced, or the device can fail. Technological constraints cannot be viewed as existing in a single dimension; rather, they must be viewed from several physical, technical, economic, and material angles. Material posture, in addition to the physical element, is important in preventing further scaling. Researchers aren't interested in changing the CMOS material composition. Standard lithographic techniques fail miserably at the nanometer scale. Unless the industry-

first examines the cost-benefit analysis, it will cease to exist. We are unable to create parts and devices for which there are no foreseeable returns. In addition, the smaller the size, the more faults there are and the more money it costs to fix them. To solve all of these problems, new technology is required. Nanotechnology-based Quantum Cellular Automata is seen as one of the most promising technologies in this situation. Thanks to this new technology, traditional transistorized designs are being replaced by nanostructures like quantum dots or metal islands. This design is based on quantum physics ideas and makes use of CMOS's vulnerabilities. [4]

1.4 Development of QCA Technology

As of right now, transistors with a width of only 14 nanometers are being mass-produced by companies like Intel. As the second most common element on our planet, silicon is used to make them. Silicon atoms have a diameter of 0.2 nanometers, making them the minor aspect known. Because modern transistors include silicon atoms about 70 bits wide, it is becoming increasingly difficult to make them smaller. The size of a transistor is rapidly approaching its physical limit. Transistors now communicate by transferring electrical impulses from one place to another. To complete a circuit, electrons move from one point to another using Quantum Dot Cellular Automata. This new silicon-free CMOS technology is a radical departure from previous iterations. Connected quantum dots arrays in QCA are commonly used to perform various Boolean logic operations, such as AND and OR. Quantum-dot cellular automata, often known as QCA, is a physical form of cellular automata that utilizes quantum mechanical phenomena. Instead of using a wide range of voltages or currents to estimate binary values, QCA technology calculates them by looking at the location of electrons. Terahertz band), density (50 Gbits/cm2), and dissipation (100 W/cm2) are all significant advantages of this approach of storage. [5]

1.5 Objective of Research

Quantum Dot Cellular Automata, a kind of Nanotechnology, is the subject of this book (QCA). A high-density, the low-power-consumption system was selected and proposed because of QCA. The primary objective of this research is to develop a QCA 4*4 multiplier that will enhance the present values of numerous of its Key Performance Indicators (KPIs).

Researchers should take note of how well-designed the study articles are. The digital logic circuit may be more efficient by reducing the number of parameters such as cell count, size, and delay time. Cell count Any multiplier design that exists now must be improved upon to meet the criterion. This can reduce the number of cells, the design area, and the simulation delay time compared to prior work, among other requirements.

1.6 Advantages of QCA

The industry standard for building Very Large Scale Integrated (VLSI) devices has been complementary metal-oxide-semiconductor (CMOS) technology for the past 40 years. There are certain disadvantages, such as the fact that switching from one CMOS material to another has not sparked the interest of researchers. In addition, the smaller the size, the more faults there are and the more money it costs to fix them. Alternative technologies like Quantum Cellular Automata (QCA) are being developed to address the inherent constraints that CMOS technology will impose over time. The advantages of QCA technology outweigh the disadvantages of traditional CMOS technology. [6]

- Research suggests that the intrinsic switching time of a QCA cell is at best.

1. In the order of terahertz.
2. In the order of megahertz for solid-state QCA
3. And gigahertz for molecular QCA due to the proper quasi-adiabatic clock switching frequency setting.

- QCA cell structure is highly symmetric, and switching speeds are breakneck.
- An extremely high density of devices.
- It can be used at room temperature.
- The ability to mass-produce electronics by self-assembly.
- Compared to CMOS technology, it is appealing because of its size, faster speed, feature, high scalability, greater switching frequency, and low power consumption.

1.7 Drawback of QCA

The distinctions between QCA and CMOS clock, such as how data is stored, how data flows are synchronized, and how QCA cells are powered, synchronize the design of a QCA circuit considerably different from that of a VLSI device. The overall timing of a QCA

circuit is primarily determined by its configuration due to the 4-phase clocking. The "Layout=Timing" Problem is a well-known example of this fact. The use of wasted buffers to synchronize the QCA circuit is one of the most severe disadvantages of Layout=Timing. This thesis will address the issues listed below, which are caused by layout=timing limitations. [7]

• Complex global floor planning**:** The synchronization of QCA circuits is critical to the proper operation of entire circuits. To synchronize a synchronous QCA circuit, several buffers are required. Because each buffer may have a varied number of clock zones and cells, each buffer's clock zone and cells should be fully defined and assigned before building a QCA circuit. This complicates global floor planning.

• Number of clocking zones and cells**:** It is evident that an increase in buffers means increased clocking zones and cells.

• Wasted Area**:** In QCA circuits, the number of cells in the first clocking zone may be greater than the number of cells in the last clocking zone. If each clocking zone has the same amount of space, the last clocking zone may waste a lot of space. Furthermore, synchronization buffers are clocked arrays of QCA cells in a specific location. As a result, most buffers may waste a lot of space. [8]

1.8 Binary Wire

The binary wire is considered the interconnection between two or more gates for flowing information, binary logic “0” or “1”. Cells are placed next to each other, forming a chain or wire shown in the figure. If one cell is polarized to logic “0”, other cells in the chain will be logic “0”. The information is transferred through the binary wire by Columbia interaction. No current flow is taken place during the information process. The cells in a binary wire can be rotated by 45º, which is called inversion binary wire. Inversion wire permits another binary wire in the same layer to pass information without interacting polarization. The correct number of cells should be taken to overcome the occurrence of accidental signal inversion. The schematic view of the inverter wire is shown in figure 1.10. When one cell in binary wire takes polarization from the previous cell and passes to the next one, this process is called the domino effect. [9]

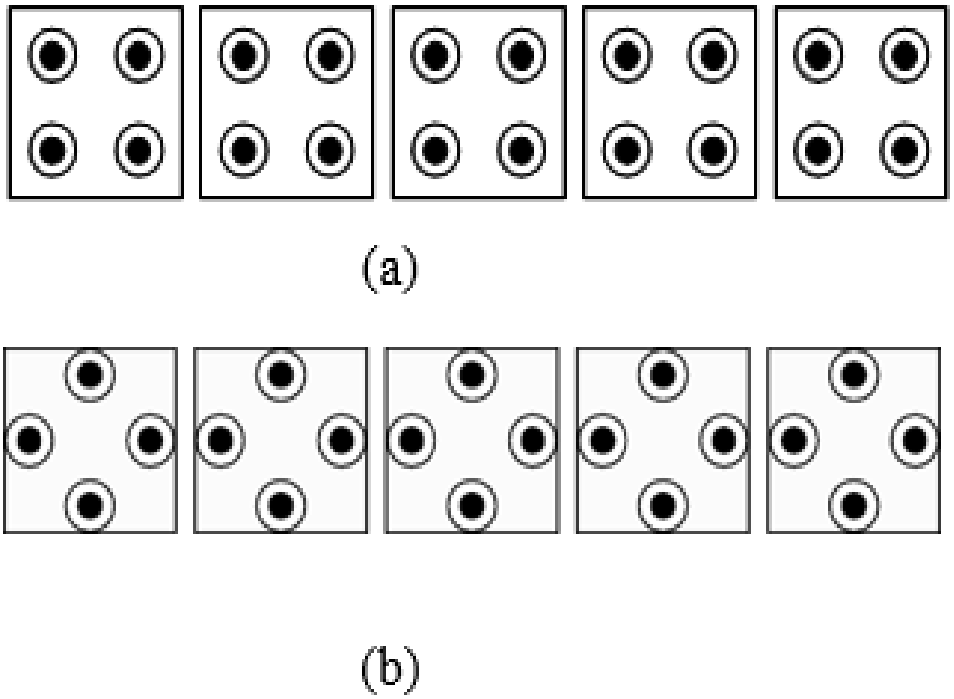

Figure 1.1 Binary Wire; (a) Normal Binary wire; (b) 45-degree rotated Binary wire [9]

Chapter 2

Background and Literature Review

2.1 QCA Basic Concept

QCA is a quantized approach to ordinary computation, not quantum computing, in the strictest sense. The use of QCA to extend the boundaries of classical calculations is being researched, as is the development of a validated method for verifying the technique's physical limitations.

2.1.1 QCA Cells and Wires

In Figure 2, you can see a nanostructure with four quantum points s. The following is a sample of my work: (a). The regions are linked together by the charge's location. [4]. To tunnel between the four quantum sites, two electrons reside in the nucleus. There is just one location where Tunnelling occurs: No Tunnelling between the cells and no lag time. Numbers 1 through 4 are arranged in ascending order, starting with the top-right dot (i=1), followed by i=2, I =3, and i=4 at the bottom-left dot (i=2). Dots are divided into a column for ease of counting. Where pi is the electrical charge at dot I, a polarization p is defined as To see how evenly the electrical cost is spread across the cell, use polarization. QCA utilizes binary information to derive conclusions about the situation.

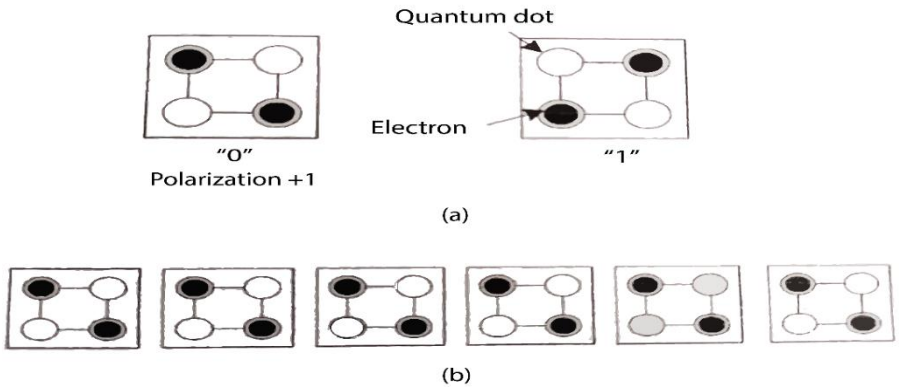

Figure 2.1 Schematics of QCA cell and wire: (a) binary QCA cells, (b) a QCA wire composed of coupled cells [9]

Each logic cell incorrectly processes the locations of two passing electrons. Despite small barriers, electrons can escape below the length control due to columbic repulsion, as seen in Figure 2.1. (a). Two charges represent binary '0' and '1' with polarization -1 and +1. There is bi-stability in quantum confinement and Columbic repulsion due to the unique electronic charge [9]. It is possible that when a cell is close to another driving cell, the polarization will be added together. Studies have demonstrated that cell interactions are

very nonlinear (even a rather polarized cell induces an almost totally polarized cell output). As a result of the interactions between neighbouring cells, data is sent along a QCA cell line. The input polarization is transferred via inter-cell Columbic repulsion in the one-dimensional cell array. It's possible to use a QCA "wire" that's a chain of cells, as illustrated in Figure 2.1(b), instead of a genuine wire. Many different kinds of logic components may be connected using this wire type. [9]. Consequently, QCA can offer "processing in a wire". Because no electrons tunnel between cells in QCA, the method transmits information without causing a current flow.

2.1.2 Types of Binary Wire

The term "binary wire" refers to the connecting of two or more gates for the flow of information, i.e. binary logic "0" or "1." Cells are connected to form a chain or wire, as indicated in the diagram. Other cells in the chain will be logic "0" if one cell is polarized to logic "0." By columbic contact, information is transferred over a binary wire. During the information processing, there is no current flow. Inversion binary wire is when the cells in a binary wire are rotated 45 degrees. Another binary wire in the same layer can use an inversion wire to pass information without interfering with each other's polarization. It is necessary to take the correct amount of cells. Output Input A B C 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 Figure 1.10 depicts the schematic perspective of an inverter wire. The domino effect occurs when one cell in a binary wire absorbs polarization from the preceding cell and passes it on to the next. [10]

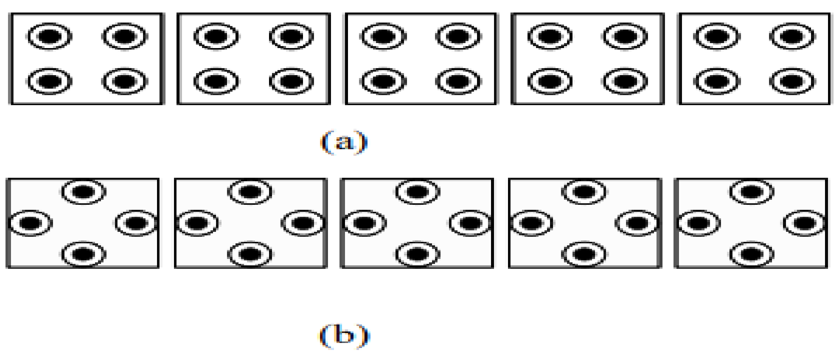

Figure 2.2: Binary Wire; (a) Normal Binary Wire; (b)45-degree rotated Binary wire [10]

2.1.3 QCA Basic Gates

Based on mutual communication between cells, essential logic components such as reverse and three-input majority door can be integrated into QCA [4]. These two holes are seen in Figure 2.2. By positioning the cells diagonally, the inverter can obtain inversion capability. A majority gate is made up of five QCA cells that perform the following task:

$$M(a, b, c) = ab+bc+ac \tag{2.2}$$

Majority gates can be readily transformed to AND & OR gates by utilizing a fixed value for one of the outputs. [4]. A two-input AND gate, for example, is created by setting one of the majority gates inputs to "0":

$$AND\ (a,b) = M\ (a,b,0) = ab \tag{2.3}$$

Similarly, an OR gate is realized by fixing one input to "1."

$$OR(a,b) = M(a,b,1) = a+b \tag{2.4}$$

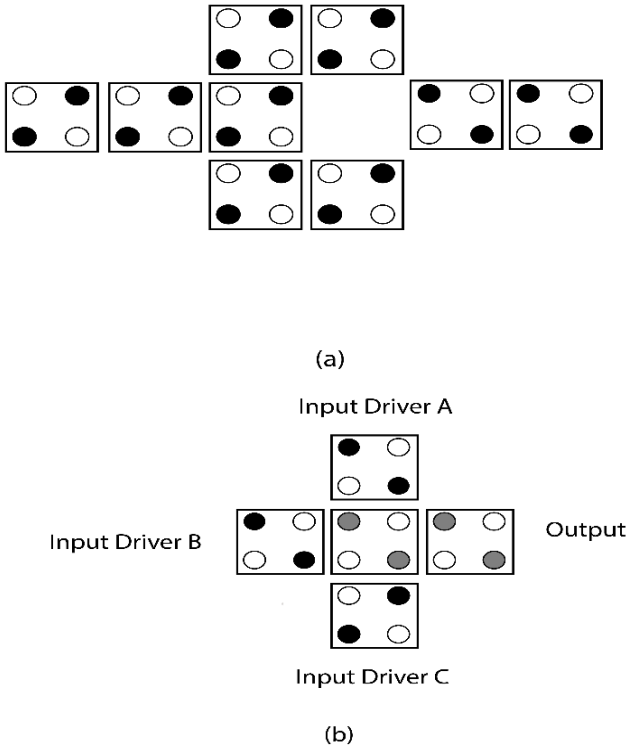

Figure 2.3 QCA basic gates: (a) inverter, (b) majority gate [9].

These two logic components, when combined with inverters, can be utilized to build any logic function.

2.1.4 Majority Voter and Inverter Gate

The majority voter (MV) and inverter gates are the two most basic gates for the QCA platform. Basic gates are used in various circuits, including multiplexers, RAM, full adders, and subtractors. The complements of the given input will be the output of the inverter gate. The majority logic of the input arguments will be the MV gate's output. A majority voter gate is not conceivable with an even number of inputs because it is impossible to reach a judgment. As a result, it can only be done with an odd number of input arguments. [11-13] the majority gate has three, five, and seven inputs. Equations (2.7) and equation (2.8) are used to describe the function of MV3, MV5 gates (2.8). By making fixed polarization of any inputs -1 and +1 (encoded logic 0 and 1), the MV3 gate can be

turned into AND and OR gates. The figure depicts the schematic perspective of MV3, MV5, AND, OR inverter gate gates. [11-13]. The MV3 gate's function,

$$fMV3\ (A, B, C) = AB + BC + CA \quad (2.5)$$

MV gate can be acted as AND gate,

$$fMV3\ (0, B, C) = BC \quad (2.6)$$

MV gate can be acted as OR gate,

$$fMV3\ (1, B, C) = B + C \quad (2.7)$$

The function for MV5 gate,

$$fMV5 = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (2.8)$$

Table 2.1: Truth Table for 3 input Majority Voter Gate

Input			Output
A	B	C	
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

2.1.5 QCA Wire Crossing

For example, it may produce a variety of signal wire crossings, which makes QCA stand out. A two-dimensional crossing and a multilayer crossing can be used in QCA technology [4]. A two-dimensional crossing was envisioned as a single QCA layout characteristic. As illustrated in Figure 2.3(a), one layer was chosen for crossover implementation, which represents essentially distinct forms of cross-overs in two dimensions. This is illustrated in Figure 2.3(a) by using half-cell displacement inverters with just two normal cells for proper signal propagation. Electrical converters might be employed in considerable numbers in two-dimensional designs as a result. Each ordinary and turned cell is utilized in a two-dimensional crossover. When the two cell types are correctly aligned, they don't interact

[4]. Prior investigations [10] have found that two-dimensional crossings are likewise affected by layout and noise. Figure 2.4(b) illustrates that a multilayer crossing [19] employs more than one layer of cells to duplicate CMOS technology's metal wire routing.

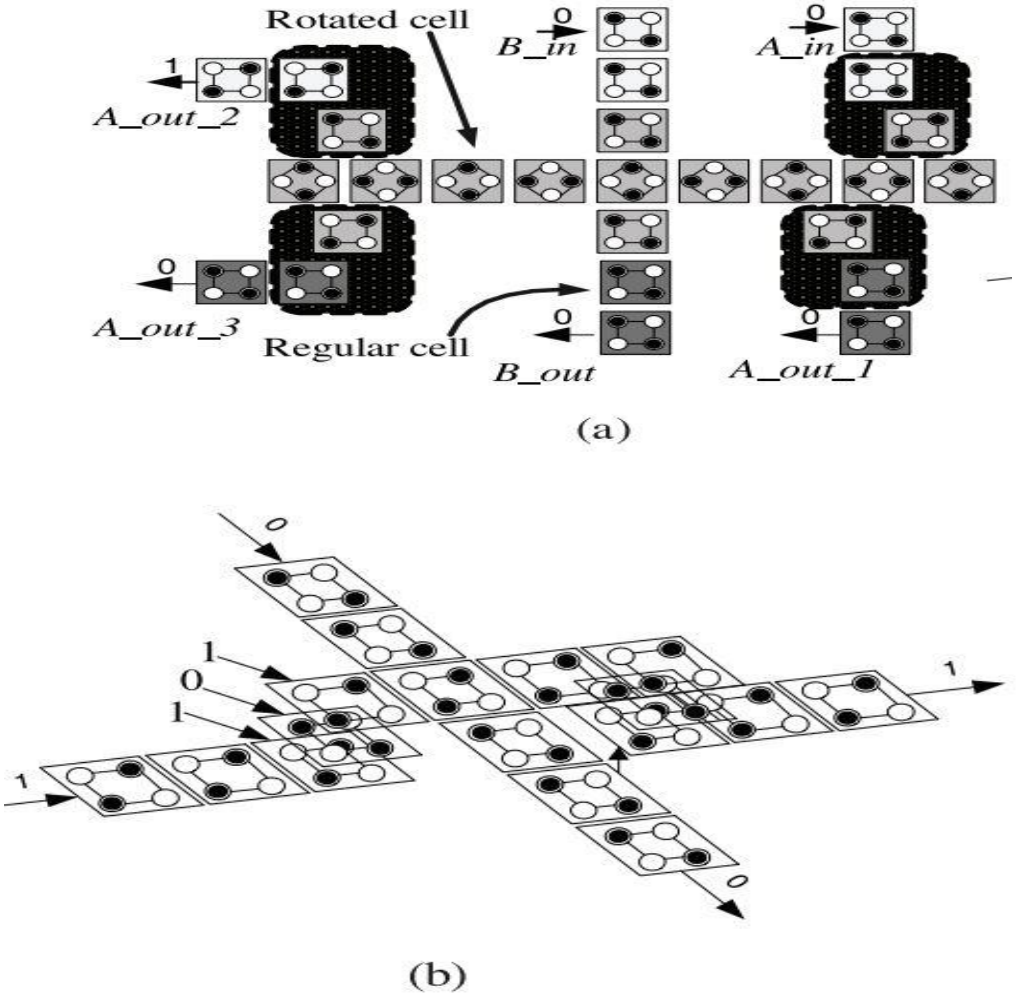

Figure 2.4 Two crossover options in QCA: (a) coplanar crossover, b) multilayer crossover [10]

Simulations suggest that multilayer crossover will yield a large number of reliable findings. Crossing many layers at once, on the other hand, is a difficult task. Because of the many layer structure, constructing a multilayer crossover is predicted to have a more excellent value than fabricating a two-dimensional crossing. A style's price depends on whether it has two-dimensional or multilayer crossovers. [11]

2.2 Clocking Scheme

It is necessary to timing QCA circuits if they are to work correctly. Switching QCA states is controlled by potential barriers that exist between quantum dots inside a QCA cell. For reducing and increasing QCA tunneling barriers, the clock is in charge. This regulates knowledge flow as well as ability provisioning in QCA. [12]

2.2.1 Typical Four-Phase Clocking

Quasiadiabatic four-phase continuation is commonly utilized in QCA circuits with deep pipes. QCA circuits. Using this shift ensures that the system is quick and stable, reducing stability concerns considerably [22]. Four distinct QCA square cells are evaluated during a quasi-Adiabatic change. There is a computation carried out inside a single continuous area of space. The output to a successor area then became frozen and consumed. At no point during measurement is there any disruption to the connected unpolarized system's successor zone. It, therefore, has no impact on the preceding zone. Figure 2.4(a) illustrates a 90° phase transition from one period zone to the next, with each QCA duration zone having four duration segments. QCA circuits use the electrical field in their cells to generate clock signals by varying the tunnelling barrier (the inter-dot border) between the dots. CMOS and carbon nanotubes both contribute to the electric field [23]. The cells are in the HOLD section if the inter-dot wall is strong in the HOLD section but weak in the RELAX part. When the distance between dots changes from medium to high or low, the cells will be released several times throughout the SWITCH or discharge portion. A person's skills can be transferred during the SWITCH chapter. One type of D-latch is used to close the HOLD section when the cells in the continuation zone are barred and to keep them barred until the next continuation zone bans them as well. Clock area delay (D-1) is a fourth of the clock cycle delay (Z-1) in QCA. [13]

$$Z\text{-}1 = D\text{-}4 \tag{2.9}$$

Where 'D' represents a clocked QCA "wire" as a series of latches and 'Z' represents clocking zone delay. As shown in Figure 2.4(b), the following relationship holds:

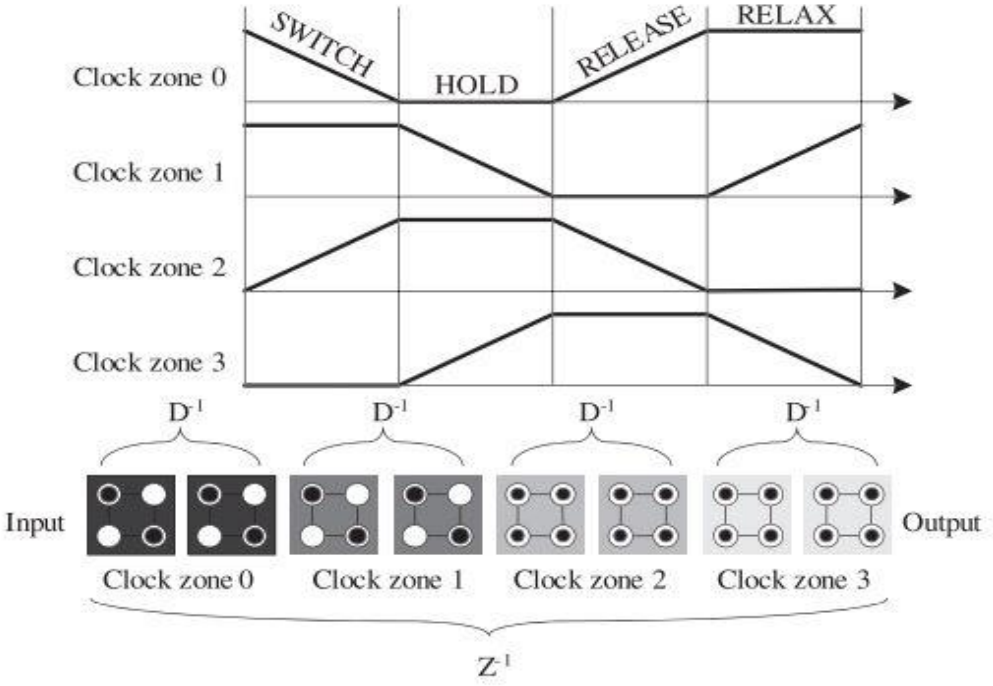

Figure 2.5 Typical QCA clocking scheme: n(a) clock signals in four clocking zones, and (b) a clocked QCA wire [12].

Although ordinary logic functions can be easily transferred to majority logic, the QCA's peculiar continuation motif makes it difficult to translate CMOS architecture into its QCA counterpart directly. Even though multiple continuation systems for magnetic QCA [24] have been proposed, four-section continuance is adopted in this book.

2.2.2 Clocking Floorplan

Two styles of continuance floorplans are utilized in QCA circuit implementations, particularly columnar regions [Figure 2.6 (a)] and zone regions [Figure 2.6 (b)]

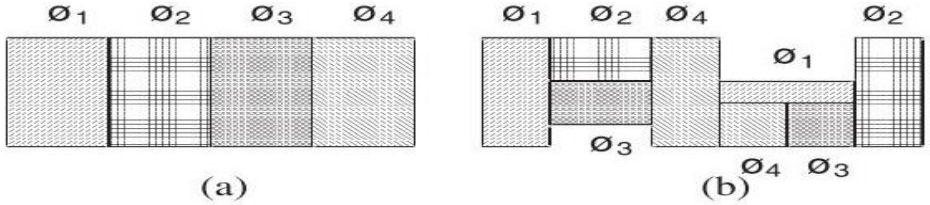

Figure 2.6 QCA clocking (a) columnar region (b) zone region [13]

In terms of physical implementation, the columnar approach is thought to be more practical. Short feedback loops and large circuit density are, however, an issue. The zone approach, on the other hand, can handle these aspects. In terms of thermal impacts, smaller continuation zones increase the lustiness of a QCA circuit. A trade-off between implementation issue logic gate potency and zone scale may exist. Smaller zones are more difficult to implement, but they are more space-efficient. The QCA temporal order zones' design significantly impacts the specific configuration of a QCA circuit. This can be asserted in general because of the "layout = timing" disadvantage [14]. The practicality of circuits is the emphasis of this work. As a result, the projected QCA architectures' long-term floorplans are designed to exploit small zones.

2.2.3 Radius of Effect

The radius at which a cell will affect other cells within the circular area drawn by that radius is known as the cell's radius of effect. The radius of influence is determined from one cell centre to the other cell centre. The radius of development is defined by d, whereas the width (height) of the cell is denoted by w, and the spacing between two cells is represented by s. [14]. The following is the radius of influence of two line cells.
The radius of effect of two line-cells is given in the following.

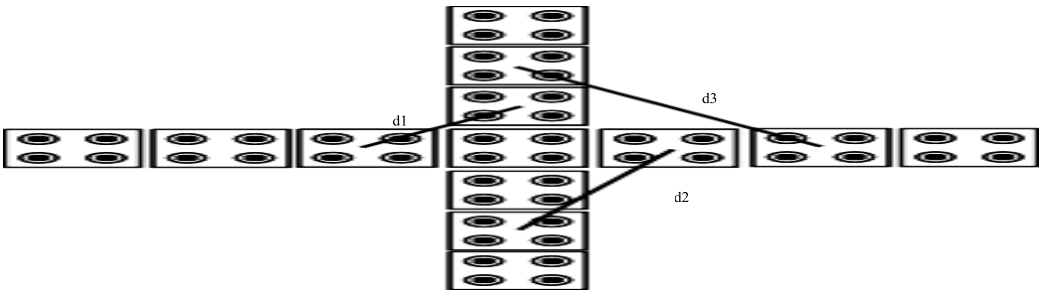

Figure 2.7 Area Drawn by Radius of Effect [14]

$$dn = w + s \quad (2.10)$$

The radius of effect of one cell to another cell next to the neighbor is given

$$dNN = 2w + 2s \quad (2.11)$$

2.3 Difficulties of QCA Based Design

Before QCA-based circuits to be considered a viable alternative to transistor-based technologies, numerous challenges must be overcome. Quantum cells should also be tiny, smaller than 20 nm, to be cost-effective. There is no engineering for meticulously processing and merging quantic cells of this scale into specified shapes at this time. Fortunately, a significant amount of time and energy is spent on size-related issues. Continuous technologies that allow small and medium transistors to produce can readily be transferred to new technologies like QCA. Second, interfaces between process circuits and I/O devices, including monitors and critical boards, are tough to create, allowing users to interact with the computer in the same way they would with any other sort of technology. This is a common constraint for new systems. It is possible to overcome the status of related nursing quantic cell manufacturing using a standard CMOS circuit determinative and to communicate information to I/O devices. There exist propagation delays in QCA systems, much like in CMOS architectures. If N is the wire cell type, an extended QCA wire may have a delay proportional to N-1.22. The short time it takes for electrons to take their new position during the tunnelling process causes this delay. [15].

2.4 Advantages and Importance of QCA Based Design

Over the traditional transistor-based style, QCA has several advantages. This design allows for terribly small feature sizes and, as a result, a high procedure density. Because the comparatively modest Columbic repulsion forces govern living creature interactions, QCA devices perform better at more minor scales where thermal energies no longer dominate the electrical forces. QCA circuits are expected to have a density of 1012 devices/cm2 with rate switch frequencies. These types will run at terribly low power levels since electricity does not flow through QCA-based circuits. The ability to implement the device densities indicated above depends on this low power value. There is no "penalty" for branching out into parallel circuits in a QCA circuit that employs continuity to restore energy to the system, as there is in old CMOS architectures. Current is divided across parallel branches of a circuit in CMOS. If some of the buffer mechanisms aren't employed, the circuit can rapidly get weakened. QCA also has an energy loss. However, it is because it is a relatively non-connected binary wire. While a system to resurrect this energy parallel branches as desired, with no detrimental consequences. Parallel units are usually synchronized via continuation. [16].

2.5 Literature Review

The collected papers listed different multipliers and some papers of full adder designing, and three papers were selected for cost function modification from the QCA circuit designs

and rules category. Those papers are reviewed here. Those papers will be helpful for this thesis work.

1.Research Paper On “Design of 4-bit serial-parallel Multiplier in Quantum-Dot Cellular Automata” 4th IEEE International conference on signal processing, computing and control, sep-2017, India, Namita, Trailokya N.S., (2017).
This paper presents an ideal configuration for a 5-input majority gate with less QCA space than existing gates. A novel Full adder QCA layout has been developed to demonstrate the applicability. The Full adder was implemented using the USE (Universal, Scalar, and Efficient) clocking technique to account for actual clock distribution. Compared to a previous superior design based on existing clocking techniques, the proposed method requires a 78 per cent reduction in area and a 45 per cent reduction in cell numbers. Compared to previous designs, this unique design exhibited significant improvements in complexity, QCA-area, and clock latency when implemented using various clock algorithms. Timing concerns and limits were investigated and explained in this article. The number of cells was lowered by 25%, while latency was reduced by 71.4 per cent [17].

2. Research Paper On “Implementation of 4x4 Vedic Multiplier using Carry Save Adder in Quantum Dot Cellular Automata” International Conference on Communication and Signal Processing, April 6-8, 2016, India, Ashvin C, Trailokya N. S., (2016)
According to QCA Technology, a 4-bit Vedic multiplier was proposed in this research (using the Urdhva Tiryagbhyam sutra). The Vedic multiplier uses a carry-save method to create partial product additions. Cell count, area, and latency are reduced by 30% in the suggested design due to a smaller 4x4 Wallace-and-Dadda multiplier. In this study, researchers used a carry-save adder to suggest a 4x4 Vedic multiplier design. To simulate this design, QCA Designer was utilized. Comparing the simulation to the Wallace and Dadda 4x4 multiplier, a 30% decrease in cell count, 60% reduction in area and 50% reduction in latency are revealed. As a result, the reduced number of cells directly contributes to the low-power use case. There is a 30% decrease in cell count, 60% reduction in area, and a 50% reduction in latency when using this method instead of the Wallace & Adder 4*4 Multiplier. [18]

3.Research Paper On “Design & Implementation of Cell Interaction Based Vedic Multiplier using Quantum-Dot Cellular Automata.” Proceedings of the 17th IEEE International Conference on Nanotechnology. Pittsburgh, USA, July 25-28, 2017, Pooja V. G., Premananda B. S., Gouthaami S. R., (2017).
This study develops a space and energy-efficient 4-bit serial-parallel multiplier based on QCA technology. First, a serial adder based on QCA is built, and then a 2-bit serial-parallel multiplier is built on top of it. By multiplying it by four, a two-bit serial-parallel multiplier is created. To assemble, analyze, and simulate QCA circuits, users utilize the QCA Designer-E software. Design circuits are assessed based on parameters such as cell count, total area, and energy dissipation. It was originally proposed that the multilayer QCA approach save 450 and 900 cells in general coplanar structures by using a single layer of

cells instead. With coplanar crossing and wires out of phase by 1800, the proposed multiplier circuits avoid all of the design problems of coplanar topologies while using all of their benefits. This study compares the area and energy dissipation of several serial-parallel multipliers.

In comparison to multilayer crossing multipliers, coplanar crossing multipliers contain fewer cells and waste less energy. There is no comparison between the speed of serial-parallel multipliers and the area efficiency of serial-parallel multipliers. QCA-based multipliers with more complex multiplication algorithms must be investigated [19]. Constructed with a high-speed adder, the comparison is given below-

Table 2.2: Comparison of Cell Interaction Based Vedic Multiplier [19]

Multiplier	Cell	Area (μm^2)
2*2	291	0.4
4*4	1959	2.39

4. Research Paper On "Design of Adder and Binary Multiplier in QCA using Coplanar Technique." 2017 International Conference on Intelligent Computing & Control.

Fixed-point numbers were utilized in this study as opposed to floating-point values in previous ones. For this reason, the multiplier has an enormous influence on CPU performance: it is a vital part of the central processing unit (CPU). This research presents the ripple carry adder (RCA) with full adder (FA) and the 4-bit by the 4-bit binary multiplier. This paper uses QCA technology, and the fewest number of cells, a 4-bit RCA Adder and a 4-bit multiplier are designed and shown. Researchers have created a parallel multiplier circuit, sometimes called a ripple carry array multiplier. Many commercial products, such as high-speed calculators, mobile phones, computers, and general processors, need a binary multiplier to function. Adder (RCA) is carried by ripple, and a complete adder was utilized (FA). Two distinct techniques have been studied: processing on wire and memory in motion. [20]

Table 2.3: Comparison of KPI values with proposed paper [20]

Multiplier	Cell	Area	Delay
4*4 Wallace	3295	7.39	10
4*4 Dadda	3384	7.51	12
Proposed 4*4	2756	5.78	8.5

5. Research Paper On "Design & Analysis of Compact QCA Based 4-bit Serial- Parallel Multiplier" 2018 Third International Conference on Electrical, Electronics, Communication, Computer Technologies & Optimization Techniques (ICEECCOT), 14-15, December 2018.

This study develops a space and energy-efficient 4-bit serial-parallel multiplier based on QCA technology. First, a serial adder based on QCA is built, and then a 2-bit serial-parallel multiplier is built on top of it. Four bits are added to the serial-parallel multiplier to make it a four-bit multiplier. To build, analyze, and simulate QCA circuits, users utilize the QCA Designer-E software. Design circuits are assessed based on parameters such as cell count, total area, and energy dissipation. Results show that using a 4-bit serial-parallel multiplier decreases the number of cells, the amount of space needed, and the amount of energy used. It was originally proposed that the multilayer QCA approach save 450 and 900 cells in general coplanar structures by using a single layer of cells instead. With coplanar crossing and wires out of phase by 1800, the proposed multiplier circuits avoid all of the design problems of coplanar topologies while using all of their benefits. This study compares the area and energy dissipation of several serial-parallel multipliers. Due to the serial entry of the multiplicand bits, a serial-parallel multiplier has a simple design, albeit at the expense of performance. In comparison to multilayer crossing multipliers, coplanar crossing multipliers contain fewer cells and waste less energy. There is no comparison between the speed of serial-parallel multipliers and the area efficiency of serial-parallel multipliers. For faster multiplication of large word sizes, QCA-based multipliers with more sophisticated multiplication algorithms should be studied. A QCA-based serial adder was used to construct a 2-bit serial-parallel multiplier. Cell count and energy dissipation were found to be less in coplanar crossing multipliers than in multilayer ones. [21]

6.Research Paper On "QCA Based FIR Serial Multiplier using cut-set algorithm." Proceedings of the 17th IEEE International Conference on Nanotechnology. Pittsburgh, USA, July 25-28, 2017.

Using the cut-set approach, this research seeks to optimize QCA-based FIR serial multipliers' design. Reduced area, clock delay, and cell count are among the work's most important contributions. The FIR serial multiplier is constructed using the zone cross over approach, and the results are compared to earlier work using the QCA cost function. Simulating the multiplier recommended by QCA Designer is second nature to it. Compared to earlier work, the suggested FIR serial multiplier is produced more efficiently using the zone cross-over option. With the new multiplier, design complexity is reduced because it is created using standard cells. There is less latency, less space taken up by the new multiplier, and fewer cells used overall. As an alternative to other serial multipliers, the proposed FIR one has been tested against various QCA implementations and shown to be superior in all respects. The cut-set algorithm is used to imitate the design's aesthetics and functionality. To build it, the cross-over method was used. They found that utilizing normal cells resulted in shorter delays, smaller areas, and fewer individual cells compared to prior research. [22]

7.Research Paper On Published online: 7 January 2020 © The Korean Institute of Electrical and Electronic Material Engineers 2020

Using only one uniform layer of cells, this work covers QCA-based combinational circuit design, such as half-adder and full-adder. A unique XOR gate is used to implement the proposed method. In reduction to the best documented XOR, the suggested XOR gate improves speed by 50% and reduces the number of cells required by 35%. According to the QCA Designer program, the proposed designs are less complex and consume less energy than earlier designs. With QCA technology, a new single layer Exclusive-OR gate design is shown in this study. In reduction to the best documented XOR, the proposed design improves speed by 50% and reduces the number of cells required by 35%. The provided gate can create improved half and full adders with a significant reduction in circuit layout area and cell count. When compared to earlier designs, the suggested XOR gate demonstrates a significant reduction of power dissipation. The proposed designs' reduced complexity makes it particularly appealing for adaptation to different circuit designs. This work proposes using only one uniform layer of cells to create a complete adder-like combinational circuit. Compared to the best-documented XOR, the proposed XOR Gate improves speed by 50% and reduces cells by 35%. [23]

8.2019 IEEE Long Island Systems, Applications and Technology Conference (LISAT).

This study uses several methods to create a four-bit QCA BCD (Binary-Coded Decimal) full adder. To create a four-bit BCD full adder, QCA Designer is utilized. When designing and fabricating a conventional microelectronic adder, Xilinx software is utilized. Simulated waveform and QCA full adder simulation results are compared for validity. In this research, a 4-bit BCD full adder is designed and simulated. The BCD complete adder's methods are implemented here. When tested in a virtual environment, the 4-bit BCD total adder worked as expected. Because of the improved design, it operates with a shorter delay than a typical ripple carry adder. The QCA full adder's functionality was verified using a 4-digit BCD full adder built-in Xilinx. Our 4-bit BCD full adder will be upgraded to a 64-bit QCA full adder in the future, and the design will be optimized to run faster and consume less space. QCA BCD full adders are expected to use less energy, have a smaller footprint, and be faster than traditional CMOS full adders. This research uses two different types of QCA cells to demonstrate the idea. 45-degree QCA cells vs typical QCA cells in the study Compared to a standard ripple-carry adder, they've cut their delay time in half. [24]

9.IEEE Transactions on Circuits and Systems II: Express Briefs (Volume: 65, Issue: 1, Jan 2018)

This paper proposes a QCA decimal full adder mainly composed of fully used majority gates (i.e., no constant inputs) and sometimes contains PUMs. QCA Designer developed and tested the circuit. Cell count, area, and latency all improved by 39%, 78%, and 12%, respectively, when the results were contrasted with those of previous research of a similar kind. A full logic set is composed of an AND gate, an OR gate, and a majority gate, all of which may be described as partly used majority gates, with one input, each 0 or 1. Many CMOS-implemented logical circuits, such as computer arithmetic circuits, are also realized

on the QCA platform. There may be better ways to use used entirely majority gates than just mapping AND/OR gates to partially utilized majority gates in related CMOS architectures. There will be fewer overall majority gates in this design, like complete binary adders with only three majority gates. DFA QCA implementations have been unsuccessful in the past, leading to inefficient designs with a considerably greater number of partially utilized majority gates than completely operated majority gates. By changing the DFA logical equations to better use completely utilized majority gates, the author came up with a DFA implementation that uses 16 utilized and only nine partially operated majority gates, along with 12 inverters. This DFA's QCA comprises 669 cells, 25 QMs, 12 QIs, 14 multilayer QXs, and six coplanar QXs, for a total of 669 cells. It has a cin-cout delay of seven clock zones and a total used area of 0.76 m2. The improvement in latency and area is 1 (4) fewer clock zones and 59% (44%) less space consumption as compared to the fastest (cheapest) previous DFA. In this QCA Decimal Full-Adder, the PUM (Partially Utilized Majority) Gate is a rare exception to the rule of utilized majority gates. [25]

10. Research Paper on Full Adder Circuit Design with Novel Lower Complexity XOR Gate in QCA Technology, Published online: 7 January 2020 © The Korean Institute of Electrical and Electronic Material Engineers 2020.

Using only one uniform layer of cells, this work covers QCA-based combinational circuit design, such as half-adder and full-adder. A unique XOR gate is used to implement the proposed design. In reduction to the best documented XOR, the suggested XOR gate improves speed by 50% and reduces the number of cells required by 35%. According to the QCA Designer program, the proposed designs are less complex and consume less energy than earlier designs. With QCA technology, a new single layer Exclusive-OR gate design is shown in this study. In reduction to the best documented XOR, the proposed design improves speed by 50% and reduces the number of cells required by 35%. The provided gate can create improved half and full adders with a significant reduction in circuit layout area and cell count. When compared to earlier designs, the suggested XOR gate demonstrates a significant reduction of power dissipation. The proposed designs' reduced complexity makes it particularly appealing for adaptation to different circuit designs. [26]

11.Research Paper on Decimal Full Adders Specially Designed for Quantum-Dot Cellular Automata.

In this work, they suggest a QCA decimal full adder, which is primarily composed of thoroughly utilized majority gates (i.e., no constant inputs) and only rarely employs PUMs. QCA Designer developed and tested the circuit. Compared to previous trials, the findings showed a 39% improvement in cell count, a 78% improvement in area, and a 13% reduction in latency. Quantum-dot cellular automata (QCA) reality was the focus of their demonstration. M arithmetic circuits in all have been reworked to some extent. The two most basic QCA components are a 3-way majority gate and an inverter. By simply replacing AND and OR gates in logical circuits with PUM gates (i.e., with a '0' and a '1' input, respectively), QCA fundamental components may be used. Due to digital processors'

newly-invigorated decimal arithmetic units, researchers have begun utilizing QCA to build decimal arithmetic circuits. The aforementioned direct mapping, for example, can quickly build many QCA decimal full adders. Only one suggestion, however, makes better use of majority gates while simultaneously replacing numerous AND and OR gates with PUMs. In order to make better use of thoroughly utilized majority gates, we changed the DFA logical equations. This resulted in a recommended DFA implementation with 16 totally utilized and only nine partially operated majority gates, along with 12 inverters. Six coplanar QXs and fourteen multilayer QXs make up the DFA QCA which has 669 cells in total. It has a cin-cout delay of seven clock zones and a total used area of 0.76 m2. Delay and area improvements over the previous DFA include 1 (4) fewer clock zones and 59% (44%) less area consumption; that is, 0.76 versus 1.86 (1.36) m2. [27]

12.Research Paper on Design and Simulation of 4-bit QCA BCD Full-adder.

This research describes the design and simulation of a four-bit QCA BCD (Binary-Coded Decimal) complete adder. To create a four-bit BCD full adder, QCA Designer is utilized. When designing and fabricating a conventional microelectronic adder, Xilinx software is utilized. Simulated waveform and QCA full adder simulation results are compared for validity. In this research, a 4-bit BCD full adder is designed and simulated. With the help of [12], the BCD complete adder was built. On the 4-bit BCD full adder, simulations showed that it worked as expected. Shorter latency than a typical ripple-carry adder is achieved by using [12]'s improved design. The QCA full adder's functionality was verified using a 4-digit BCD full adder built-in Xilinx. Our 4-bit BCD full adder will be upgraded to a 64-bit QCA full adder in the future, and the design will be optimized to run faster and consume less space. It's predicted that QCA BCD full adders would be more energy-efficient, smaller in footprint, and quicker than conventional CMOS full adders since they need less power. [28]

13.Research Paper on Design of QCA-Serial Parallel Multiplier (QSPM) with Energy Dissipation Analysis.

This letter provides an effective single-layer serial-parallel multiplier (SPM) in Quantum-dot Cellular Automata (QCA). A modified E-shaped exclusive-OR (E-XOR) gate was used to build a bit-serial adder (BSA) with a fully used majority gate (MV). The QCA cell's cell-interactive characteristics were utilized to implement the suggested E-XOR gate design. This new gate reduces cell count and area by 30% and 19% for multipliers with four, eight, sixteen, thirty-two, and sixty-four bits. It also reduces cell count and area by 29% and 24% for multipliers with four, eight, sixteen, thirty-two, and sixty-four bits, and by 32% and 46% for multipliers with 32 and 64 bits. All suggested circuits were simulated and verified with QCA Designer and a coherence vector simulation engine. QCA Pro is also used to calculate the average dissipation of switching and leakage energy. Various bit size multipliers have been provided and tested to verify the effectiveness of the proposed BSA module. There are considerable improvements in efficiency and a significant rise in cell count due to the simulation results. SPM has a 70 per cent lower design cost than the current one [14], illustrating the benefit of the suggested design. [29]

14.Research Paper on A First Step Toward Cost Functions for Quantum-Dot Cellular Automata Designs.

Several QCA-specific cost indicators are examined in this article. It is revealed that latency, the amount of QCA logic gates, and the number and kind of crossovers are all essential elements to investigate when comparing QCA systems. New cost functions for QCA circuits have been proposed. Cost functions for QCA computing arithmetic are used to assess and evaluate QCA adders. When new cost metrics are considered, previous best adders lose their allure, and various optimization aims have been shown to lead to additional "best" adders. Several QCA circuits cost indicators are examined and discussed in this research. The number of majority gates, the latency, and the number of crossings is all critical aspects of the QCA design cost function. It was decided to create a cost function family called Cost = Mk + I + Cl Tp to better evaluate QCA circuits. Adder designs have been selected as QCA representative designs. It was found that the cost metrics for coplanar and multilayer QCA adders were the same. Analyzing several QCA adders was done using CMOS cost functions and the QCA cost functions proposed. It's pointless to compare QCA designs using CMOS cost functions. Coplanar adders are preferable when taking the new metrics into account instead of the previous "best" adder. Different design goals provide additional adders, as seen by the unique measurements, which substantially influence the comparison findings. The adder to use depends on the implementation method. The weightings of various indicators may change as QCA technology improves, and new metrics may need to be considered. To enhance future QCA circuit design, this study aims to inspire more thought regarding designing acceptable cost functions for QCA circuits. [30]

15.Research Paper on Design of Baugh–Wooley multiplier in quantum-dot cellular automata using a novel 1-bit full adder with power dissipation analysis. They are published online: 24 March 2020.

An area-optimized 1-bit full adder is developed using QCA for efficient clocking and reduced cell count, and lower energy dissipation. With this new design, the number of quantum cells is reduced by 8 per cent, latency is reduced by 75 per cent, and energy dissipation is reduced by 4 per cent at 1 K compared to prior research. It is possible to build a 44 Baugh–Wooley multiplier with this new full adder architecture. Quantum cell reductions of 17.4% and a reduction in power dissipation of 2.44nW were found in simulations using the QCA Designer 2.0.3 tool when using the Baugh–Wooley multiplier built with the unique 1-bit full adder. These researchers have developed a revolutionary new one-bit full adder that uses fewer quantum cells, occupies a much smaller space, and has a propagation latency of 0.5 clock cycles. Overall, the number of cells used was up by 8%, and the area utilized was 75%. While the existing 1-bit full adder designs have a lower energy dissipation, the proposed full adder offers a 56.7 per cent improvement in energy dissipation over existing 1-bit full adder designs. Using a 1-bit full adder gives you a 44-bit Baugh–Wooley multiplier, which is faster than the current 1-bit full multiplier. The new design only needs 1638 quantum cells spread across a 1.64 m2 surface area, according to

the calculations. Even at 1 K, the multiplier dissipates just 4.10e001 eV of energy every cycle. The multiplier circuit proposed here is stable at temperatures as low as 100 K, in contrast to previously known circuits of this type. There is also 2.44nW estimated dissipation for a 4x4 multiplier design [31].

16. Research Paper on Realization of Combinational Multiplier using Quantum Cellular Automata.

Using the five quantum dot QCA cells, this study devises a new QCA structure, the QCA multiplier. The structure can multiply two binary integers of 4 bits each. This research is driven by the fact that employing QCA to create a combinational multiplier reduces its area and, as a result, its heat dissipation. The framework's effectiveness is because it uses QCA majority gates as its primitives. The block is 0.10m2 in size and has 89 QCA cells. According to this result, if the circuit in figure 7 is designed by the QCA designer, the approximate area of the circuit will be four times the area of the block, or around 0.40m2. The circuit has a substantially smaller footprint than a CMOS binary multiplier. Furthermore, if figure 8 is closely examined, it can be shown that a binary multiplier of any combination can be created by simply adding that many blocks to each level, with the number of levels corresponding to the order of multiplication. A 5X5 binary multiplier, for example, will have five levels, each having five blocks. This method effectively provides a circuit design for a binary combinational multiplier that is both efficient and effective. It is clear from the simulation results that the creation of Sout and Cout is delayed. Even if there is a delay, this approach is unquestionably more modular, systematic, and regular because the circuit is planned in blocks. [32]

17.Research Paper on Efficient Design of Baugh-Wooley Multiplier in Quantum-Dot Cellular Automata, Proceedings of the 13th IEEE International Conference on Nanotechnology Beijing, China, August 5-8, 2013.

Table 2.4: Comparison of Different QCA Multiplier Designs

Approach	Cell	Area	Latency	Throughput
4*4 Wallace [7]	3295	7.39	10	1
8*8 Wallace [7]	26499	82.18	36	1
4*4 Dadda [7]	3384	7.51	12	1
8*8 Dadda [7]	26973	82.19	38	1
Serial-Parallel (4) [5]	406	0.4935	1	1/8
Serial-Parallel (8) [5]	903	1	1	1/16
Serial-Parallel (4) [6]	-	0.1664	14	1/8
Serial-Parallel (8) [6]	-	0.6656	26	1/16
Prop. Baugh-Wooley	1982	1.8	4.75	1
Prop. Baugh-Wooley	10475	10.2	10.25	1

Baugh-Wooley multipliers are notable for their QCA design, which is detailed in this paper. Several recent majority logic results were used to develop the concept. In addition, QCA Designer simulations demonstrate the efficiency of the suggested design. With this paper, we provided the QCA implementation of the Baugh-Wooley multiplier. It is based on the

majority of logic outcomes that the designs are built on. Simulations have shown that the suggested architecture has a low area and low latency. To summarize the findings, see Table 2.3. [33]

18.Research Paper on Multipliers with Coplanar Crossings for Quantum-Dot Cellular Automata.

The design of parallel multipliers for Quantum-Dot Cellular Automata is the subject of this paper. The author designed and studied array multipliers, Wallace multipliers, Dadda multipliers, and quasi-modular multipliers. Quasi-modular multipliers, which utilise four (n/2 n/2) modules to create nn multipliers, are also considered. Coplanar layouts are used to make all of these designs. The QCA Designer simulator is used to compare the delay, area, and complexity of numerous possible operand sizes. The various 4-bit multipliers have a clock delay of 10 to 14 and cells ranging from 2956 to 3738. The latency of the 8-bit multipliers is around four times that of the 4-bit multipliers, and the cell count is nine times that of the 4-bit multipliers.

Minor delay and fewer cells characterize the 8-bit quasi-modular multipliers than the 8-bit Wallace and Dadda multipliers. All 8-bit multipliers are significantly slower and more significant than CMOS multipliers. Four-bit array multipliers are more prominent and quieter than those invented by Wallace, Dadda, and colleagues. The 8-bit array multipliers have about four times the area and cell count of the 4-bit array multipliers but twice the latency. They conclude that the essential aspect of performance is wiring. At the very least, the excessive length of several of the wires contributes to the mystery. Long connections account for 33.8% of delays, making them essential. Wallace and Dadda multipliers, which both use 8-bit multipliers, have total delays of 47.7% and 44.6%, respectively. The number of cells has an impact on delay as well. The systolic design has to be streamlined, according to these results. Given that wire crossings involve the usage of several different clock zones, their latency and area are heavily influenced by wire delay (particularly for single-layer circuits).

Table 2.5: Comparison of QCA Multipliers

Multipliers	Latency	Area	# of Cells
4*4 Array I	14	5.18 μm^2	2956
4*4 Array II	14	6.02 μm^2	3738
4*4 Wallace	10	7.39 μm^2	3295
4*4 Dadda	12	7.15 μm^2	3384
8*8 Wallace	44	87.47 μm^2	33894
8*8 Dadda	47	92.69 μm^2	34903
8*8 QMWallace	36	82.18 μm^2	26499
8*8 QMDadda	38	82.19 μm^2	26973
8*8 Array I	30	22.57 μm^2	13839
8*8 Array II	30	21.49 μm^2	15106

19. Research Paper on An efficient quantum-dot cellular automata full-adder, Scientific Research and Essays Vol. 7(2), pp. 177-189, 16 January 2012.

Two extremely fast QCA full adders are provided in this study. Five-input majority gates are used, and they have a very thick construction. There's a good idea in there somewhere. Using the supplied design principles, we were able to create a reliable QCA circuit. Compared to previous designs, the proposed QCA full adders outputs all originated from the same side of the circuit. There are no other cells around the input and output signals, so they're readily available.

To put it another way, the robust QCA full-adder proposed here beats all previous robust solutions in size, latency, and complexity. With this notion, ripple may construct adders of various word sizes (e.g. 4, 8, and 16), each with its unique functionality. A standard tool for designing and verifying QCA layouts, QCA designer, is used to verify and simulate the proposed five-input majority gates and QCA full-adders. It creates a dense network with the same latency as prior top solutions.

Instead of utilizing three-input majority gates and inverters, this design uses two-input majority gates and inverters, saving 66.6% of the area and reducing complexity by 37.80%. The new ripple-carry adders offer considerable gains in terms of area, latency, and complexity over prior designs. Using the proposed design, a recent robust 16-bit ripple carry adder improved in complexity area and delay by about 62.18, 76.27, and 70.58 per cent, as opposed to the previous robust design's 16-bit ripple carry adder.

20.Research Paper on An efficient design of Vedic multiplier using ripple carry adder in Quantum-dot Cellular Automata.

This project aims to use the Urdhva Tiryagbhyam sutra to create an 8 x 8 Vedic multiplier for QCA. The efficient 4-bit Vedic multiplier structure is used to build an 8-bit multiplier. To combine generated partial items, ripple offers adders and complete adders. The generalized structure of N N Vedic multipliers is also explored and the difficulty of the N N multiplier design. According to simulation results, the 8 8 Vedic multipliers' suggested design has a 60% cell count reduction, a 78% area reduction, and a 75% delay reduction compared to the 8 8 Wallace multiplier. Array II is 64 per cent faster and uses 18 per cent less area than the Array I multiplier while maintaining the same degree of complexity in terms of cell count.

Compared to the Array I and Array II multipliers, a generic equation is created for the number of majority gates, inverters, crossovers, and delays. The suggested architecture employs 15 cells per clock zone as a design parameter to ensure proper propagation and reliable data transfer. The results of the simulation demonstrate that the 8 8 Vedic multiplier presented is legitimate and efficient. The proposed 8 x Vedic Multiplier has a clock cycle delay of 10.75, a cell count of 13,533, and an area of 18.44 m2 based on simulation results. The simulation results are compared to those of current multipliers when it comes to cell count, latency, throughput, and area. Compared to the current Wallace multiplier, the proposed 8-bit multiplier surpasses the present Wallace multiplier in terms of cell count, area, and latency by 60%, 78%, and 75%, respectively.

Chapter 3

Proposal and Methodology

3.1 Digital Binary Multiplier

Combinational logic is used in multipliers to combine binary bits. To multiply two binary numbers, you need a binary multiplier, a digital or combinational logic circuit. This outcome is a product since it is the sum of the two integers multiplied together. The multiplicand and multiplier may be both different sizes of bits, as well. The multiplicand and multiplier bit sizes define the product's bit size. The bit size of the product is equal to the sum of the bit sizes of the multiplier and the multiplicand. Multiplication in binary follows the same procedure as multiplication in decimal. After a first step, there are two stages in binary multiplication. It begins with a single bit-wise expansion or partial product. The next step is to merge all partial derivatives into a single product or final product. Partial products or single-bit products can be generated using AND gates. These partial items may only be combined with full adders or half adders. Bit size has an impact on the schematic design of a digital multiplier. The design becomes more difficult as the bit size of the multiplier becomes more apparent. Multipliers are indispensable when it comes to digital signal processing and calculators (such as smartphones and tablets).

3.2 4*4 Multiplier

A 4-bit binary integer can be multiplied by this multiplier to get an 8-bit result since the product's bit size equals the sum of the multiplier's and multiplicand's bit sizes. It is capable of calculating up to 16 × 16 = 256 different integers. Additionally, bit number is easily calculated by taking into account a device's maximum possible output range. It is possible to get P7 with a multiplier of 44 by multiplying multiplicands of the form A3 A2 A1 A0 by multiplicand B3 B2 B1 B0. We must sum the partial products of a 44 multiplier to get the multiplier's development, which comprises four partial products. To combine them, 4-bit adders or single-bit adders might be utilized (half-adder & full-adder) [31].

3.3 Parallel Binary Adder

Parallel binary adders are used when adding several 1-bit values necessitates the use of a combinational circuit consisting of many complete adders connected in parallel. Each column can have a complete adder for addition. Due to parallelization, the number of added bits determines how many complete adders are needed for a given addition operation. You can build a parallel binary adder using just a few logic gates. Sub-modules of the logic circuit will mimic those of a half adder and a full adder. Input carry is added to the output of a single full adder. On the other hand, A Parallel Adder is a digital circuit that uses matching pairs of bits in parallel to calculate the arithmetic addition of two binary numbers more significant than one bit in length. To do this, you'll need a chain of full adders, with the output carry of each adder feeding into the carry input of the full adder after it. For an

n-bit parallel adder to work, n full adders must be used. As a result, two adders are required for a two-bit number, and so on for a four-bit value. [32]

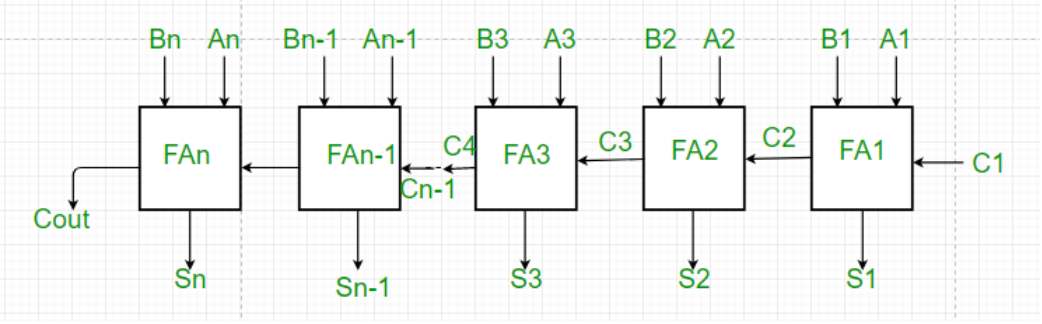

Figure 3.1: Parallel Binary Adder [32]

3.3.1 Half Adder

A half adder is a binary addition circuit for two integers. There will be two binary digits output from this device: one for total and one for carrying value, respectively. The output of a half adder is two digits since it adds two single-digit binary integers. Its name comes from an OR gate joining two half adders to create a complete adder. The short answer is, this only does half of what a full adder does.

3.3.2 Half Adder Logic Circuit and Truth Table

XOR and AND gates are needed in the most basic form of the adder to get it to work. You may also build a circuit only using AND, OR, and NOT gates. Even though the XOR IC is more popular and available, utilizing three distinct chips instead of just one may result in a more extensive circuit [33]. This is especially useful because of the three simpler logic gate ICs. Using an Exclusive-OR gate, the SUM (S) output may be generated using an AND gate to generate a Carry-out (Cout). The following is the Boolean formula for a half adder.

For the SUM bit:

$$SUM = A \text{ XOR } B = A \oplus B \tag{3.1}$$

For the CARRY bit:

$$CARRY = A \text{ AND } B = A.B \tag{3.2}$$

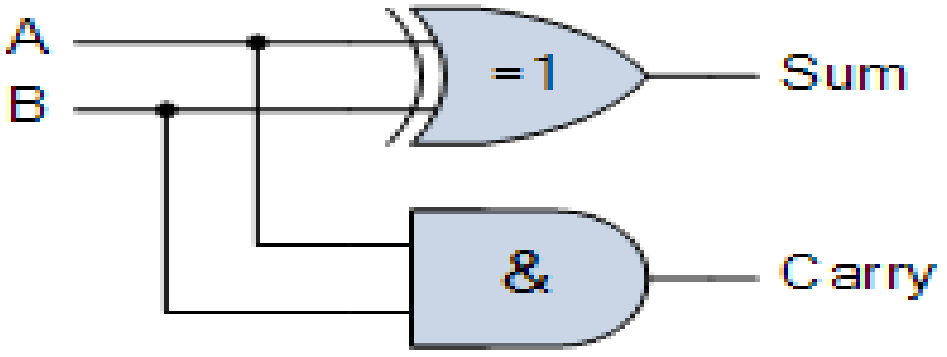

Figure 3.2: Half Adder Logic Circuit [33]

Table 3.1: Half Adder Truth Table [33]

B	A	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3.3.3 Full Adder

A full adder is a digital circuit that combines two numbers. Full adders are implemented in hardware with logic gates. An adder with three operands and a carry bit adds three one-bit binary integers. The adder generates two numbers: a total and a carrying bit. There are two types of adders: full and half. A half adder adds two binary numbers together. Adding two binary integers and a carry or overflow bit results in an adder with all eight bits. As a result, there's a total and still another carry piece. Full adders are made up of XOR, AND, and OR gates in hardware. When adding bits to a more significant number of bits, full adders are typically used. With an OR gate, you may build a full-adder out of two half-additions, such as XOR and AND.

3.3.4 Full Adder Logic Circuit and Truth Table

With three inputs instead of two, the Full Adder is an improvement over the Half Adder. As with a half adder, a complete adder is a logical circuit that adds three binary digits while also creating a carry to the next addition column. While a carry-in refers to moving money from one significant digit to another, a carry-out means moving money from one large number to another large number. When using two half adders coupled together to make a complete adder, you'll need to include an extra column in your truth table to account for the carry-in (CIN) input and sum (S) and carry-out (COUT) bits. [34]

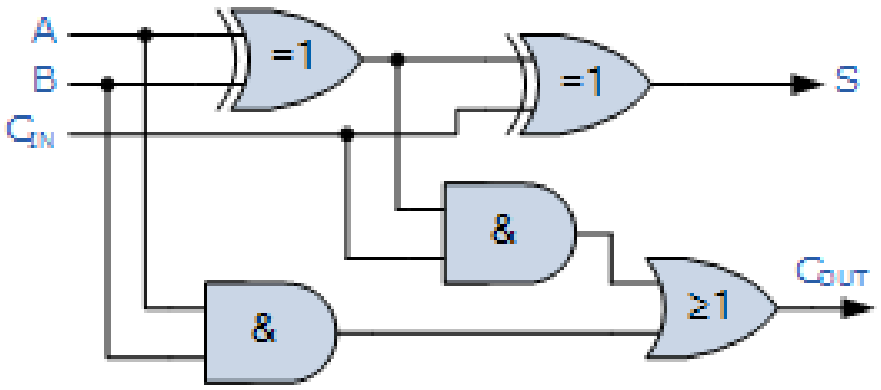

Figure 3.3: Full Adder Logic Circuit [34]

Table 3.2: Full Adder Truth Table [34]

C_{in}	B	A	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3.4 3-Bit Adder

3-bit adders have three inputs and two outputs and are referred to as such. A and B are the first two inputs, while C-IN is the third. SUM is the standard output, whereas C-OUT is the carry output. This will be done using a 3-bit adder, which will produce an X-OR of the three bits' sum, with any two being logical 1, and the carry being created as a result of this operation. To get the total, add inputs A and B together to get a partial sum, and then add that to input Cin. Cin's first two inputs will be X-ORed to produce a carry utilizing the OR operations in AB and AB's carry function. Different approaches to building a three-bit adder exist, including using a transistor-level circuit or integrating multiple gates. A 3-bit adder was utilized in our suggested design to calculate the sum of S2 and S4. [35]

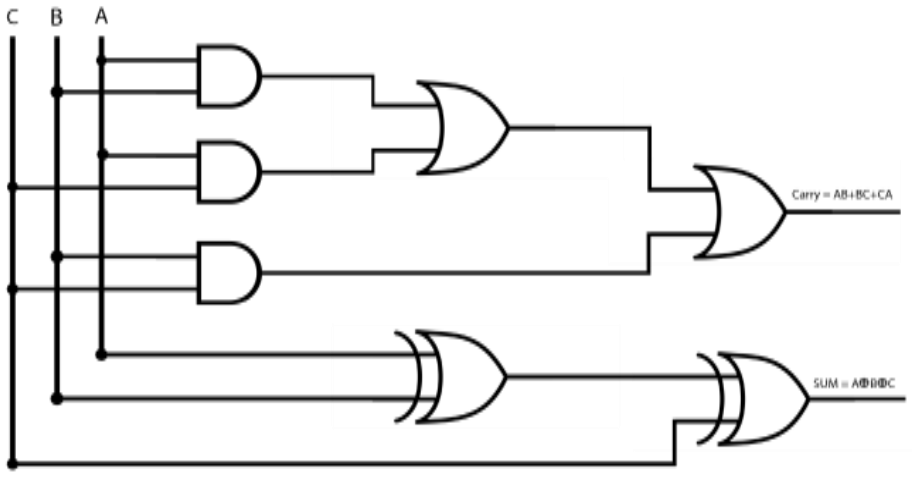

Figure 3.4: 3-bit Full Adder [35]

3.5 4-bit Adder

The 4-bit Full Adder is an adder that takes four inputs in the form of two binary values and outputs the sum and carry. A complete adder circuit was used to add two binary values, each with n bits. We've added you two 4-bit binary numbers: A0A1A2A3 and B0B1B2B3, that you must add using the complete adder. As seen in Figure 3.5, this was accomplished by cascading four complete adder circuits. To generate sum output S1 and carry output C2, the least significant bits A1B1 and carry C1 are added. The next important bits A2 and B2, are added to the carry output C2 to produce sum output S2 and carry output C3. After that, C3 is added to A3, B3, and so forth. As a result, the four-bit total output S4S3S2S1 and the final carry output Cout is produced. We used a 4-bit full adder to calculate the sum S4. [36]

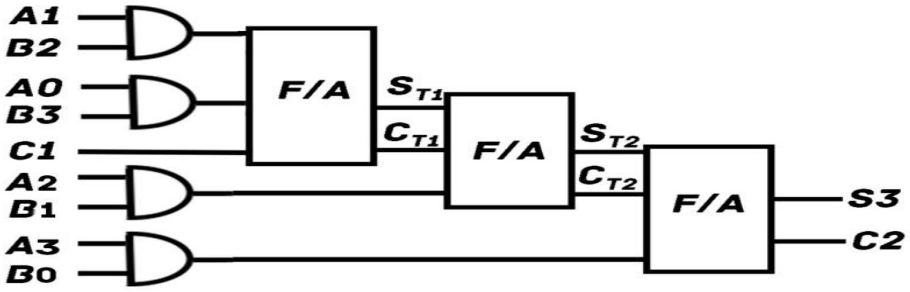

Figure 3.5: 4-bit Full adder [36]

3.6 Proposed Half Adder

Adder is half responsible for adding two logical inputs and for providing two sums and carry outputs. To assist the design attain its goal, we employed a half-adder build-up [7]. A simple adder uses simply an XOR and AND gate. The Exclusive-OR gate generates the SUM (S) output, while the AND gate generates the Carry-out (Cout) output. The sum and carry may be calculated using the following equations if the input variables are A and B:

$$\text{Sum} = A \oplus B \quad (3.3)$$

$$\text{Carry} = AB \quad (3.4)$$

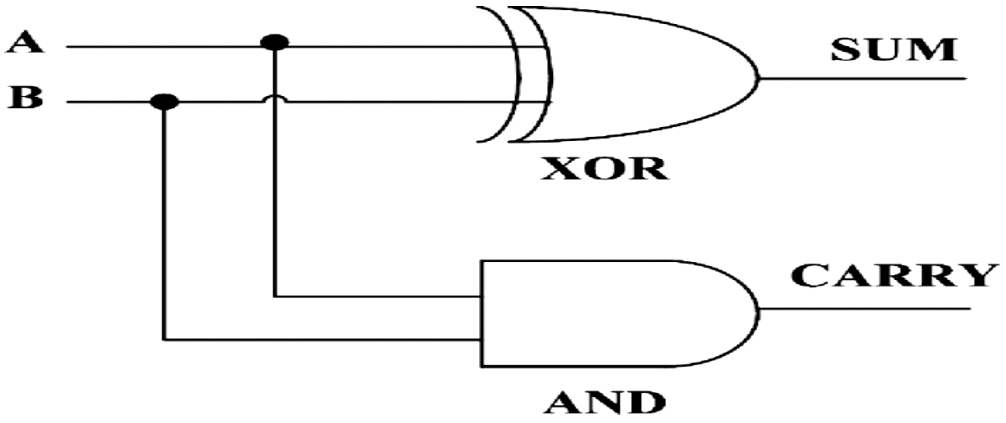

Figure 3.6(a): Half Adder Logical Diagram [7]

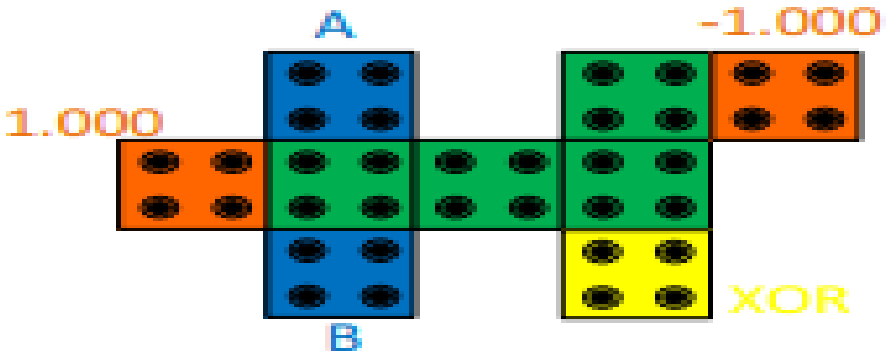

Figure 3.6(b): QCA Structure of Half Adder [7]

3.7 Proposed Full Adder

The full adder adds three logical variables and provides two outputs, sum and carry. It consists of X-OR Gate, AND Gate & OR Gate. We have used a build-up full-adder in our proposed work, and the courtesy goes to Ali.H.Majed [7]. This design of the full-adder helped us a lot to reach our target destination. If the input variables are A, B, and C in, the two outputs can be found using the following equations-

$$\text{Sum} = (A)\ \text{XOR}\ (B)\ \text{XOR}\ (\text{Cin}) \quad (3.5)$$

$$\text{Carry} = (AB)\ \text{OR}\ (B\ \text{Cin})\ \text{OR}\ (\text{CinA}) \quad (3.6)$$

The whole adder circuit has been built in this manner. A multi-input majority function can be used to build another type of full adder logical representation, and its reliability can be investigated. The suggested full adder design has been compared to other previous work in QCA. One of the significant benefits is that it is less complicated than the other complete adder. Other characteristics such as area, cell count, and delay were all qualified, but the circuit's intricacy makes it challenging to under-stable. Figure 3.7 shows a complete adder circuit that has been proposed [3.7(b)].

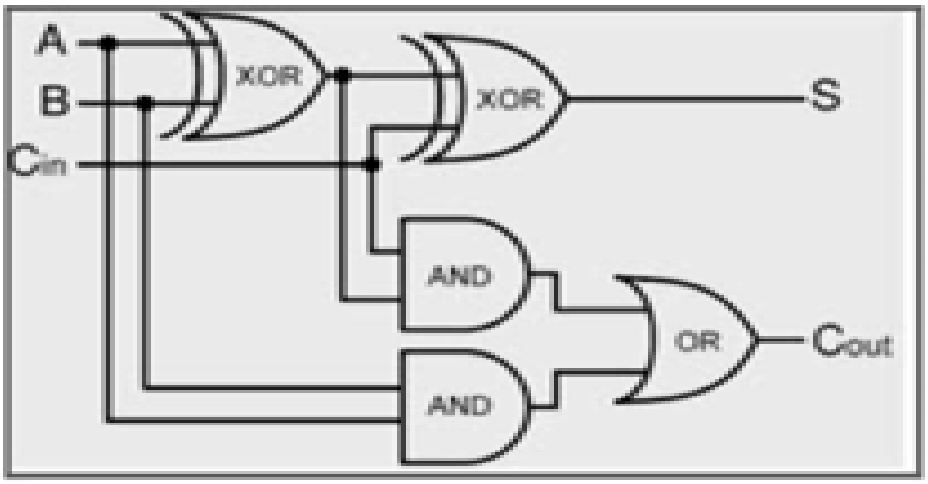

Figure 3.7(a): Full Adder Logical Diagram [7]

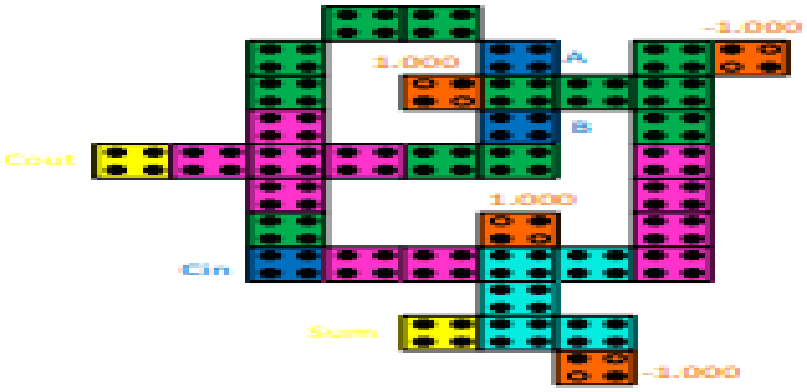

Figure 3.7(b): QCA structure of Full-adder [7]

3.8 Crossover in QCA Design

Information can be transferred from one gate to another using crossover. It functions as a link between the gates. Columbic interaction is used to transmit data. [1] Coplanar crossover, multilayer crossover, and clock zone-based crossover are three types of crossover available in QCA. [37] Each form has advantages and disadvantages. The following sections go over three different types of crossover-

3.8.1 Coplanar Crossover

Two wires cross in the same plane but are not in the same plane. There are two wires, one horizontal and the other vertical. The cells are rotated by 45 degrees, whether they are horizontal or vertical. As a design rule, the horizontal wire should have an odd number of cells. Even when the cells are crossed in the same plane and rotated by 45 degrees, the cell polarization of the horizontal and vertical wires does not interact. Because rotated cells create more space between them, energy separation in the circuit suffers. It has an impact on the maximum working temperature, entropy resistance, and switching time. There is a chance that the signal will be loosely bonded, resulting in signal discontinuity as it travels through the wires. [38]

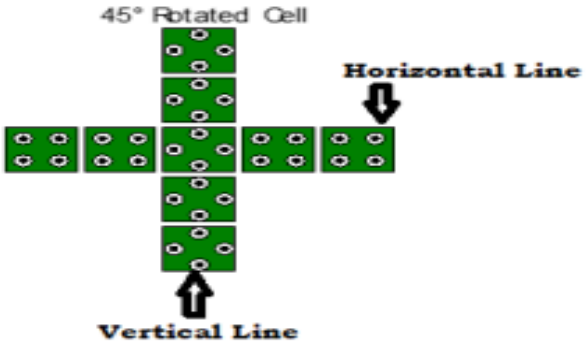

Figure 3.8: Coplanar Crossover [38]

3.8.2 Multilayer Crossover

As a bridge crossover, multilayer crossover is used. This kind does not require cell rotation. To convey information without interacting polarization, one wire is carried over another wire. This style of crossover comes at a higher price. Fabricating a multilayer crossover is tough. It has advantages such as taking up less space and reducing the likelihood of [38] unwanted crosstalk, but it has a noise problem in the crossover area. [39-40].

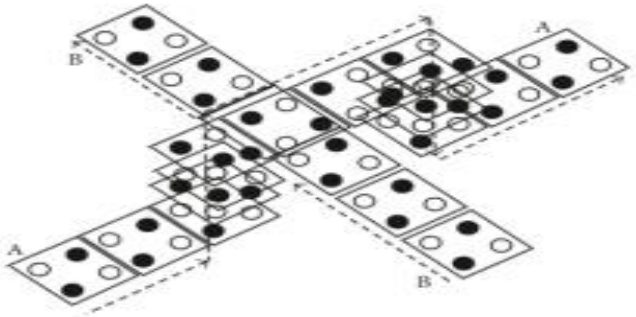

Figure 3.9: Multilayer Crossover [39]

3.8.3 Clock Zone Based Crossover

There are several issues in the previous two forms of crossover, such as loose bonding between cells owing to rotated cells, decreased energy separation and minimal switching time, and resistance to entropy. A method used for clock zone-based crossover is to arrange the horizontal and vertical wires in the same plane but in different clocking zones. The polarization of a wire in a non-adjacent clocking zone is unaffected by a wire in a non-adjacent clocking zone. On the other hand, the vertical wire should be in clock zone 2 if the horizontal wire is in clock zone 0. Two non-adjacent clocking zones should have a 180-degree phase difference. On the other hand, the vertical wire should be in clock zone 3 if the horizontal wire is in clock zone 1.

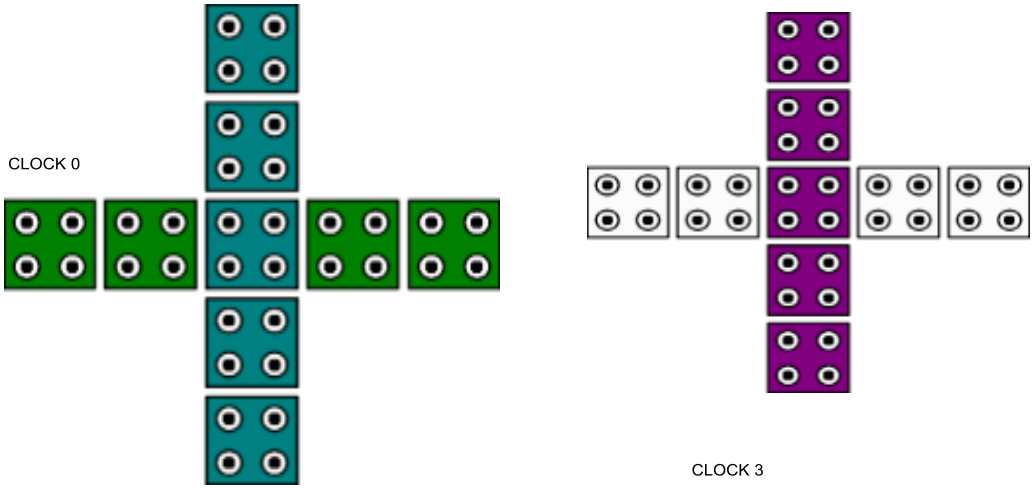

Figure 3.10: Clock Zone-Based Crossover [41]

3.9 Proposed 4*4 Multiplier

In our proposed multiplier, we have distributed the total sum into seven parts. The methodology was to design the sum individually from S0-S6, respectively. The addition of those sums implements the desired multiplier. The essential addition of the multiplier is shown in figure 3.8. To obtain the target output of the 4*4 multiplier, we have assumed input as A 0A 1A 2A 3 and B 0B 1B 2B 3. Then we have done multiplication on the assuming inputs. After accumulation, we got 16 multiplied bits, indicating the sum and carry of our target 4*4 multiplier. We must have observed that our targeted output circuit depends on the sum and carry from the figure. [33] So, we figured out those sums and reached our wanted circuit design. Here, the methodology of implementing the multiplier is the addition of 16 multiplied bits. We have found the first multiplied bit as S0. Then, the addition of the 2nd and 3rd bits provides the sum S1. The least essential bits A 1B 1 and carry C 1 are added to produce sum output S 1 and carry output C 2. Carry output C 2 is added to the next significant bits A 2 and B 2, producing sum output S 2 and carry output C 3. C 3 is then added to A 3 and B 3 and so on.

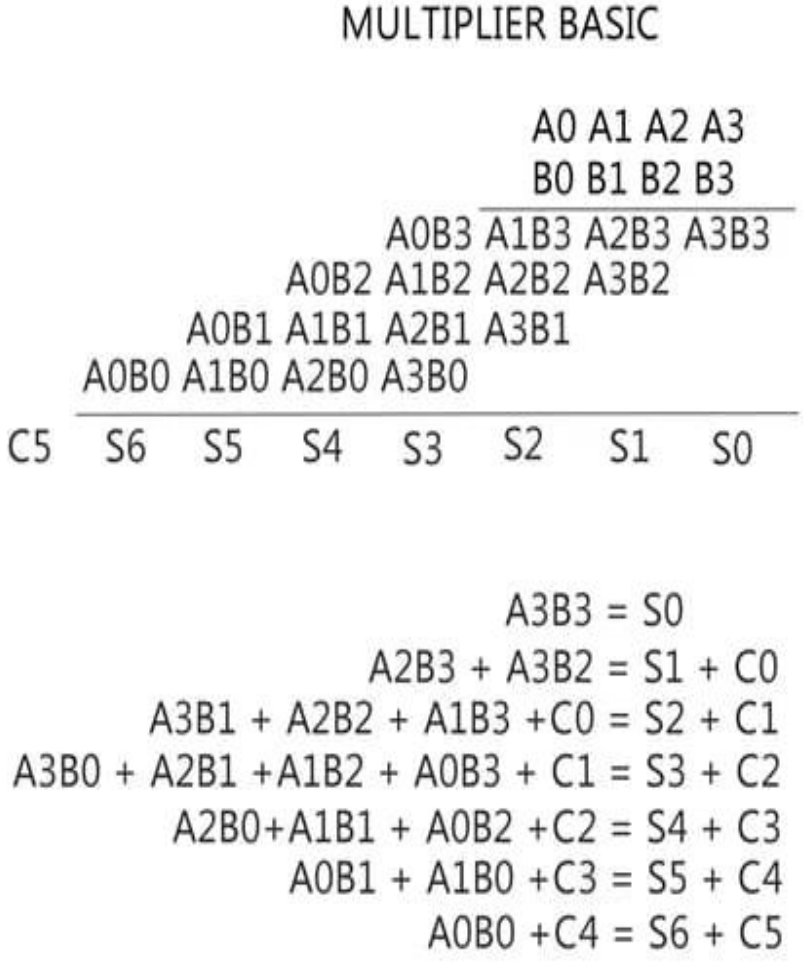

Figure 3.11: Basic Methodology of 4*4 Multiplier.

Chapter 4

Simulation and Result Analysis

4.1 Coherence Vector Engine

The coherence vector engine was utilized for the sake of simulating the process. Simple QCA circuits are frequently manufactured using this technique since it speeds up the modelling process. The bi-stable approximation is regarded as a valuable tool for determining the logical feasibility of a style. The bi-stable approximation simulation engine's quickest benefit is its capacity to model a more extensive QCA style range in a short period quickly. The arithmetic and logical feasibility of demanding QCA circuits will be enhanced in light of the anticipated developments. For precise planning, a bi-stable approximation simulation engine is employed. The multiplier circuit has undergone extensive testing, and the results show that it is pretty effective. We believe that cell displacements might compromise the simulator's security. On the other hand, simulations show that this mistake propensity is more forgiving than the other type that we usually study. The engine's main drawback is that it needs a manufacturing method that accurately inserts cell clusters. To me, the most encouraging feature of this theory lies in its impossibly exact placement. As a result, once the technology is available, this design may be worth experimenting with in the future. The QCA Designer machine has specific problems. As a result of this, the simulation's overall signal quality suffered. When a signal loss occurs in a circuit, the QCA continuation mechanism should mostly make up for it. Every style's cells are near together due to the absence of adjustability. Simulations that allow the cells to be split and therefore have greater flexibility of movement are needed before the predicted style can be known as an enhancement. Depending on how many cells are near an output, QCA Designer generates different results. Simulations on a multiplier with input and output cells beyond the array's boundaries were the most obvious example. According to the simulation findings, if the output is to be in one of the corners, that's where it should be. The planning of the multiplier was altered to get precise results. [42]

4.2 Experimental Setup

To obtain the target output of the 4*4 multiplier, we assumed input as A0A1A2A3 and B 0B 1B 2B 3. Then we have done multiplication on the assuming inputs. After doing multiplication, we got 16 multiplied bits. The additions of those bits have been added by binary parallel adders like a 3-bit adder and a 4-bit adder to produce the sum and carry of our desired multiplier.

4.2.1 QCA Design of S0

S0 is the multiplication of bits A 3 & B 3. From figure 3.8, we find out S0 is just A3B3. To design the sum in the QCA, we have taken inputs as A3 and B3 and linked them by creating an AND gate.

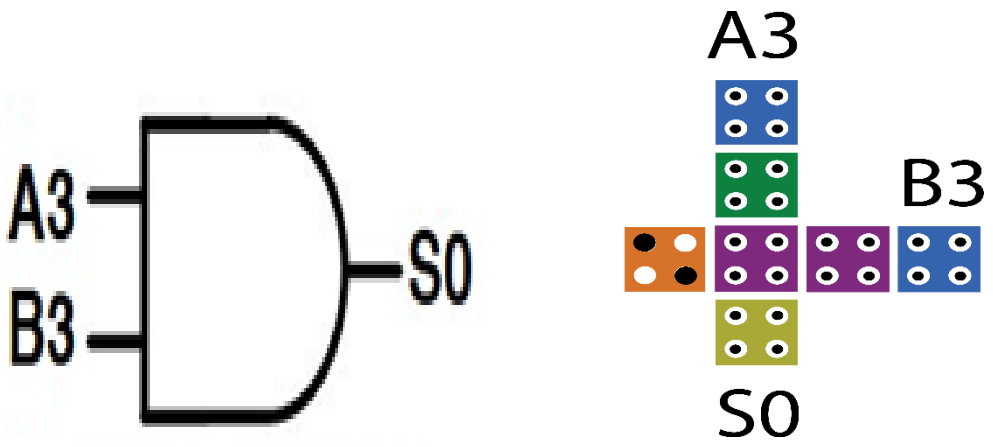

Figure 4.1(a): And Gate with S0 ,(b): QCA Design of S0.

4.2.2 QCA Design of S1

S1 is the addition of A2B3 and A3B2. With a half Adder, we get sum S1 and carry C0. Circuit Diagram for S1 is given in figure 4.2(a), and in 4.2(b), QCA design for S1 is provided.

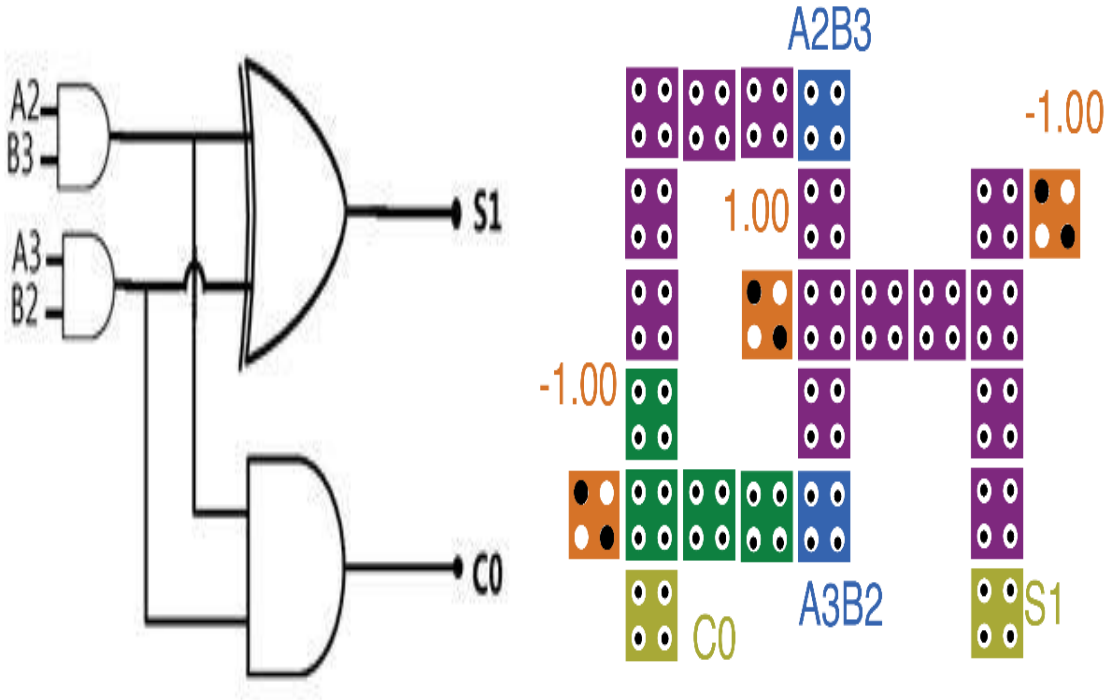

Figure 4.2(a): S1 output with Half-Adder, (b): QCA Design of S1.

4.2.3 QCA Design of S2

S2 is the addition of A3B1, A2B2, A1B3 and C0 (carry of S1). At first, we used a full Adder to add A3B1, A2B2, and C0, where we get a Sum (St) and a Carry (Ct). Then we used another full Adder in the addition of A1B3, previous Sum (St) and Carry (Ct) to get S2**,** and we also got a carry C1. Circuit Diagram for S2 is shown below-

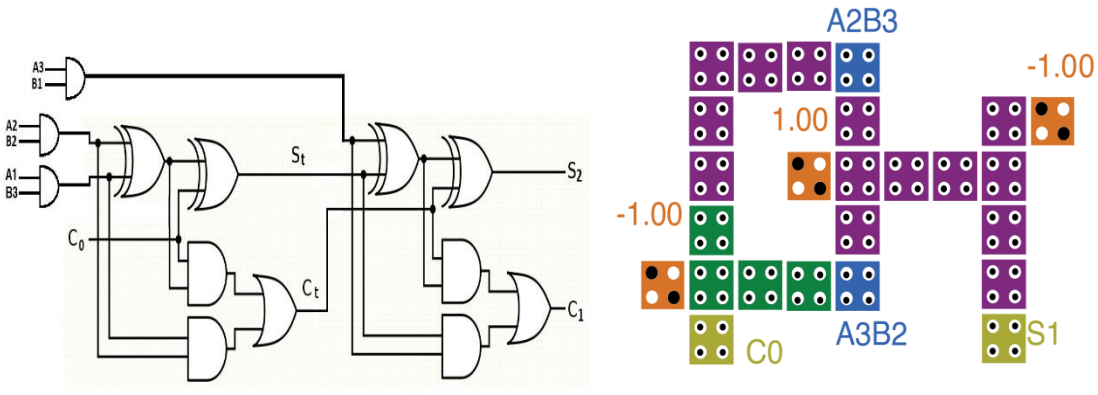

Figure 4.3(a): Full Adder with S2 and C1, (b): QCA Design of S3.

4.2.4 QCA Design of S3

Here, S3 is the addition of A3B0, A2B1, A1B2, and A0B3 and carry C1. Adding A1B2, A0B3 and C1 is done with a full adder in input and got two outputs that we called sum (St1) and carry (Ct1). Then we use another full adder to add A2B1, St1 and Ct1 in input and get two outputs called sum (St2) and carry (Ct2). One more use of full adder in A3B0, St2 and Ct2 in input provides the output of sum S3 and carry C2. Circuit diagram is shown below-

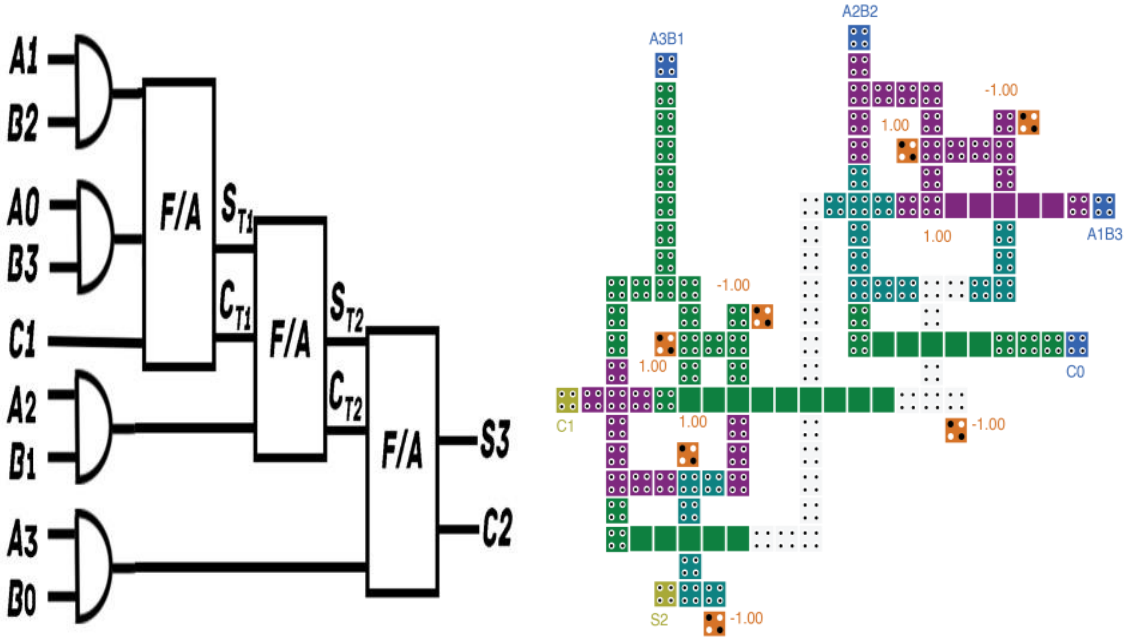

Figure 4.4(a): Without Full Adder S3 and c2, (b): QCA Design of S3.

4.2.5 QCA Design of S4

Here, S4 is the addition of A0B2, A1B1, and A2B0 and carry C2. At first, we used a full Adder to add A1B1, A0B2 and C2**,** where we get a Sum (St) and a Carry (Ct). Then we used another full Adder in the addition of A2B0, previous Sum (St) and Carry (Ct) to get S4, and we also got a carry C3. Circuit Diagram for S4 is shown below-

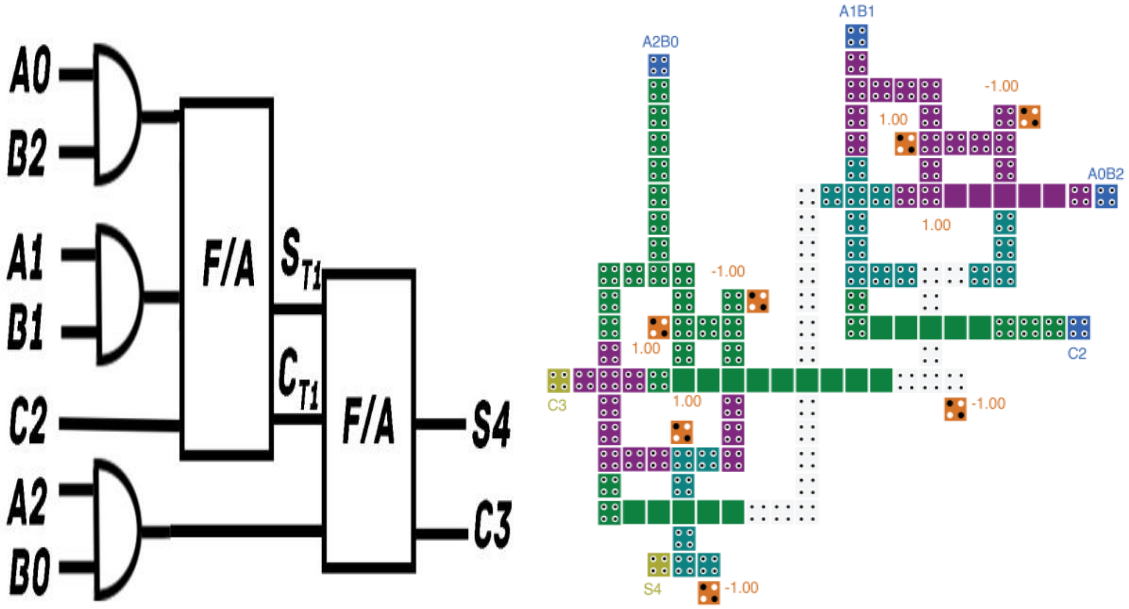

Figure 4.5(a): Full adder with S4 and c3, (b): QCA Design of S4.

4.2.6 QCA Design of S5

S5 is the addition of A0B1, A1B0 and C3. S5 is the addition of A0B1, A1B0 and C3. With the use of a Full Adder, we get sum S5 and carry C4. Circuit Diagram for S5-

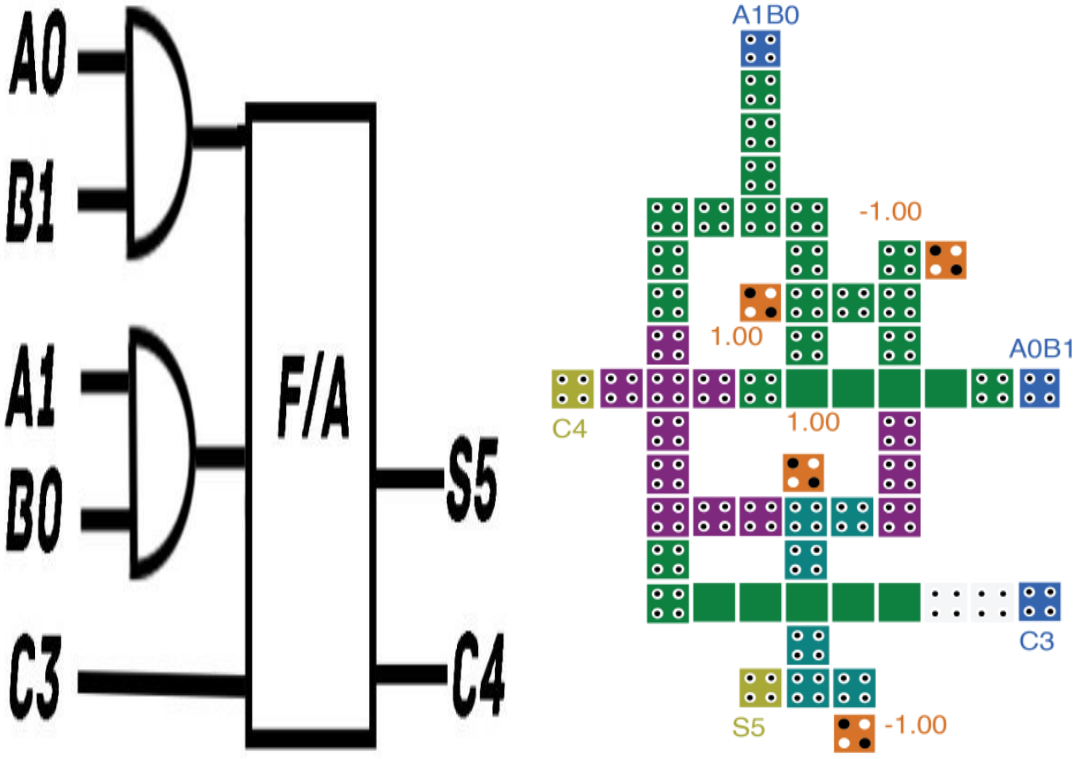

Figure 4.6(a): Full adder with S5 and C4 ,(b): QCA Design of S5.

4.2.7 QCA Design of S6

After getting S5, we have to add A0B0 and C4 to get S6 and also get C5. For S6, we use a Half-Adder with A0B0 and C4 in input and get S6 and C5 as output; circuit diagram is shown below-

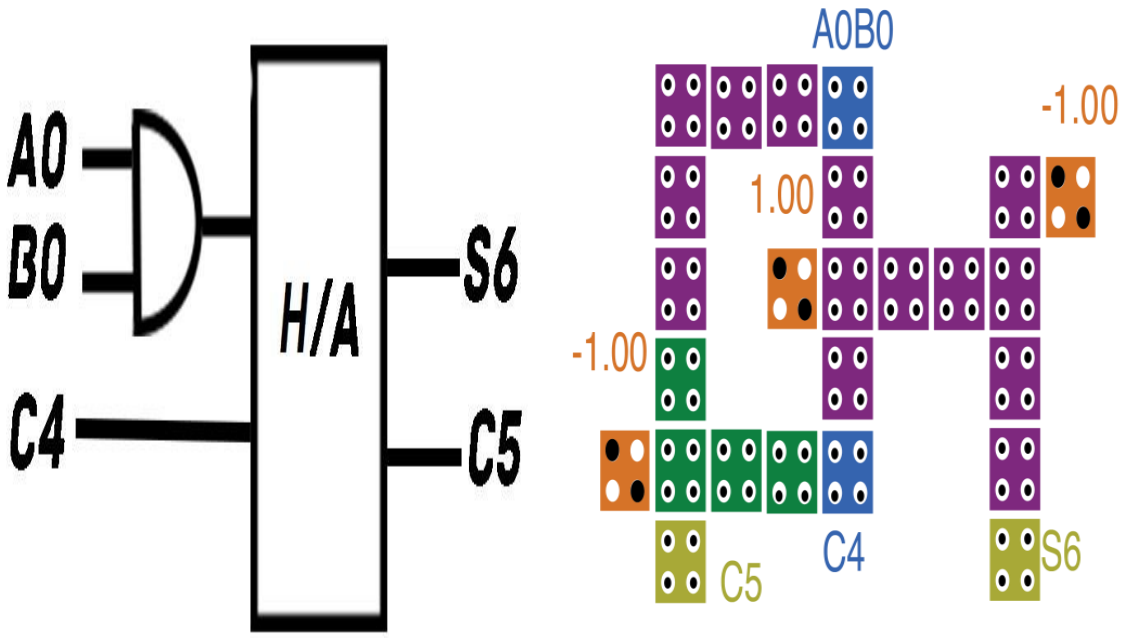

Figure 4.7(a): Half Adder with S6 and C5, (b): QCA Design of S6.

4.3 Proposed Design of 4*4 Multiplier

This paper has tried to design a 4* 4-bit multiplier via Quantum Dot Cellular Automata. In this case, we designed the circuit using the QCA 2.0.3 version. The cells in our design are expected to have a height of 18 nm, a width of 18 nm, and a diameter of 5 nm, while the quantum dots have a diameter of 5 nm. The cells are also arranged in a grid with a cell centre-to-centre distance of 20 nanometers. For simulation, the coherence vector engine was employed. Simulations suggest that this tendency of error is more forgiving than the other style we frequently examine. The engine's principal limitation is that it requires a technique of production that correctly places cells. The most promising aspect of this thesis is that it has such a precise positioning that it is impossible to achieve at this time. As a result, once the technology is available, this style may be worth experimenting with in the future. Because the transistor size can no longer be reduced, CMOS technology has been a source of concern for nanotechnology.

Besides, Conventional lithographic processes can no longer cope in the Nano-scale range. We followed the same steps as the schematic diagram but in a different order. Our circuit was designed using a binary parallel adder and a 3-bit and 4-bit complete adder. To obtain the target output of the 4*4 multiplier, we have assumed input as A 0A 1A 2A 3 and B 0B 1B 2B 3. Then we have done multiplication on the assuming inputs. After multiplication,

we got 16 multiplied bits, indicating the sum and carry of our target 4*4 multiplier. We have done multiplication among the bits and divided them into seven parts as a sum and their carry. Figure 4.8 (a) shows the multiplier's schematic diagram, whereas figure 4.8 (b) shows the 4*4 multipliers proposed design (b).

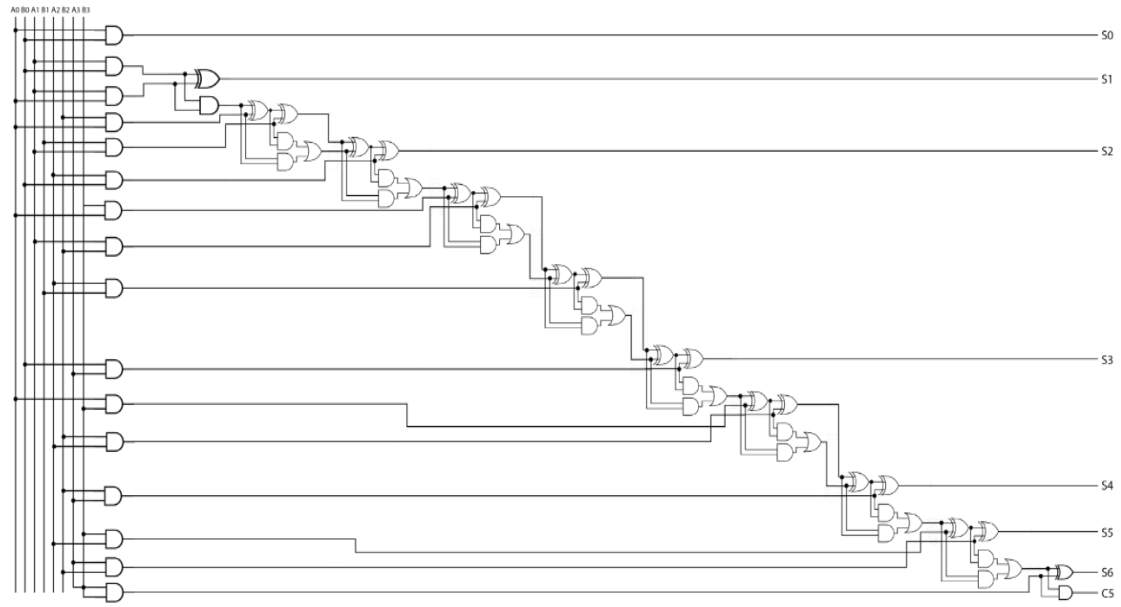

Figure 4.8(a): Schematic Diagram of 4*4 Multiplier.

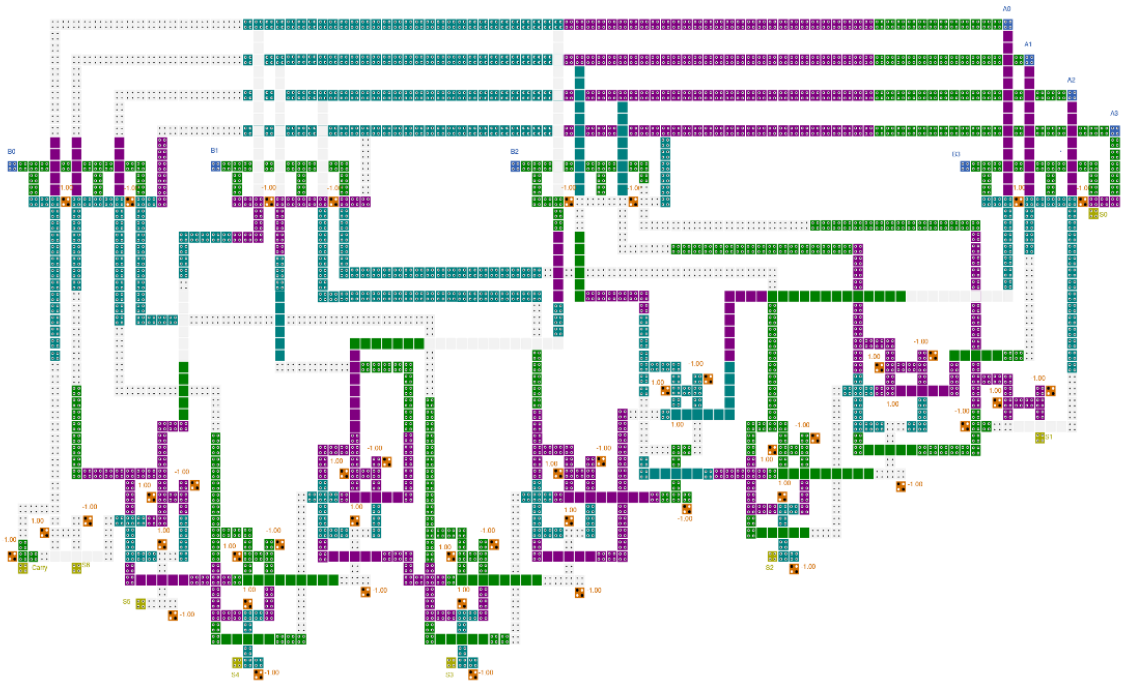

Figure 4.8(b): QCA Design of 4*4 Multiplier.

4.4 Key Performance Indicators (KPI)

The impacts of factors on QCA circuit performance are defined by key performance indicators (KPI). These are the parameters that determine how circuit performance behaves. The correlation between circuit performances is readily evaluated using a one-to-one indicator comparison of KPI. This paper chooses critical performance indicators (KPI) and includes them in a complete literature assessment. [43]

4.5 Reasons of Inclusion KPI in QCA

Key Performance Indicators (KPI) are chosen after a thorough investigation. According to the study, KPIs have a significant impact on circuit performance. Two types of circuits are chosen: RAM and a one-bit full adder. KPI can be used to evaluate the circuit's inherent behaviour.

It can also evaluate how all KPIs relate to one another. i.e. it can illustrate any fluctuation in performance as a result of changing any circuit parameter. A one-to-one parameter comparison of KPI is explored in a comparative study, which analyzes the correlation between circuit performances. The following are the reasons for using Key Performance Indicators in a comparative study:

4.5.1 Justification for Cell Count

The energy dissipated by the QCA cell is relatively minimal. Small circuits, such as one-bit RAM and full adder circuits, do not consume a lot of power, but huge circuits with many cells, such as 16, 32, and 64-bit full adder, subtractor circuits, do. As a result, in a comparative study, cell count/number of cells is more essential. [44]

4.5.2 Justification for Number of Gates

The majority voter gate is well known for dissipating a considerable amount of irreversible power. In QCA, the inverter gate adds to the circuit's complexity. The greater the number of gates, the more excellent the power dissipation.[45]

4.5.3 Justification for Clocking Scheme

In most circumstances, the clocking schemes employed in QCA circuit design are overlooked while justifying circuit performance. However, with the QCA platform, it is a significant signal. In QCA technology, clocking schemes such as free, 1D, 2D, and USE (Universal, Scalable, and Efficient) are available. With a feedback channel, the clocking method ensures proper signal flow. Among all possible clocking schemes, the USE clocking method has the shortest routing feedback path. The thermodynamic effects are eliminated by using the 2D, USE clocking method. Temperature sensitivity is considerable, and the lengthy binary wire prevents operation at high temperatures. [46]

4.5.4 Justification for Number of Clock Zone and Area

In CMOS, the clock zone is calculated as 14 cycles of delay unit. Delay is a critical metric for assessing circuit performance. Even if all indicators are at a reasonable level, the performance of a circuit with more clock zones, delay, will be degraded. As a result, a small number of clock zones is highly valued in circuit design.

4.5.5 Justification for Number of Clock Zone and Delay

In CMOS, the clock zone is calculated as a fraction of a cycle of the delay unit. When evaluating circuit performance, the delay is a crucial factor to consider. Even if all indicators are at a reasonable level, the performance of a circuit with more clock zones, delay, would suffer. So, for circuit design, a small number of clock zones is highly valued.

4.5.6 Justification for Area

A circuit becomes more efficient when the number of gates is reduced. When the number of gates in a circuit is lowered, the cells inside it become closer together, and their polarization interacts owing to radius effects. As a result, the circuit's operation is disrupted. Thermodynamic effects occur when the distance between gates increases to overcome radius effects, and the number of clock zones increases due to the lengthy binary wire. To eliminate radius effects and long binary wires, area optimization is critical. [47]

4.5.7 Justification for Set/Reset Ability

The ability to set/reset is a crucial parameter in a RAM circuit. A RAM circuit's Set/Reset capability is essential when choosing the optimal RAM circuit for QCA technology. The significance of these cost functions with KPI in QCA circuit performance analysis is investigated using QCA and CMOS cost functions. In the data collection section, the relationship between these cost functions and KPI will be clearly illustrated. The relationship between KPI and these cost function equations can be seen as a flow chart. [48]

4.6 Total Number of Clock Zone (CZ)

The total number of clock zones necessary for the circuit is determined as the total number of clock zones required. The number of clock zones used from input to output is used to compute delay. The number of clock zones determines the amount of uncertainty. The area of the circuit will grow as the number of clock zones grows. Concerning the adjacent clocking zone, each clock zone has a phase difference of /2. In total, four clocking zones produce a phase difference of two. Each clocking zone has a 14-cycle delay, while four clocking zones have a one-cycle delay. The following is a formula for calculating the number of clocking zones. The number of clock zones from each input (Cin) to output (S0) in the diagram is ten. Figure (b) simulation results demonstrate that each clock zone produces 14 cycles, with a 2.5 cycle delay for ten clock zones. [49]

4.7 Simulation Result

The simulator accepts 2n amount of inputs. As the proposed multiplier is distributed in seven parts of sum, it contains 27=128 amount of inputs. The simulation result of this vast number of inputs is divided by us into two parts. They are provided in Figures 4.9(a) & 4.9(b), respectively.

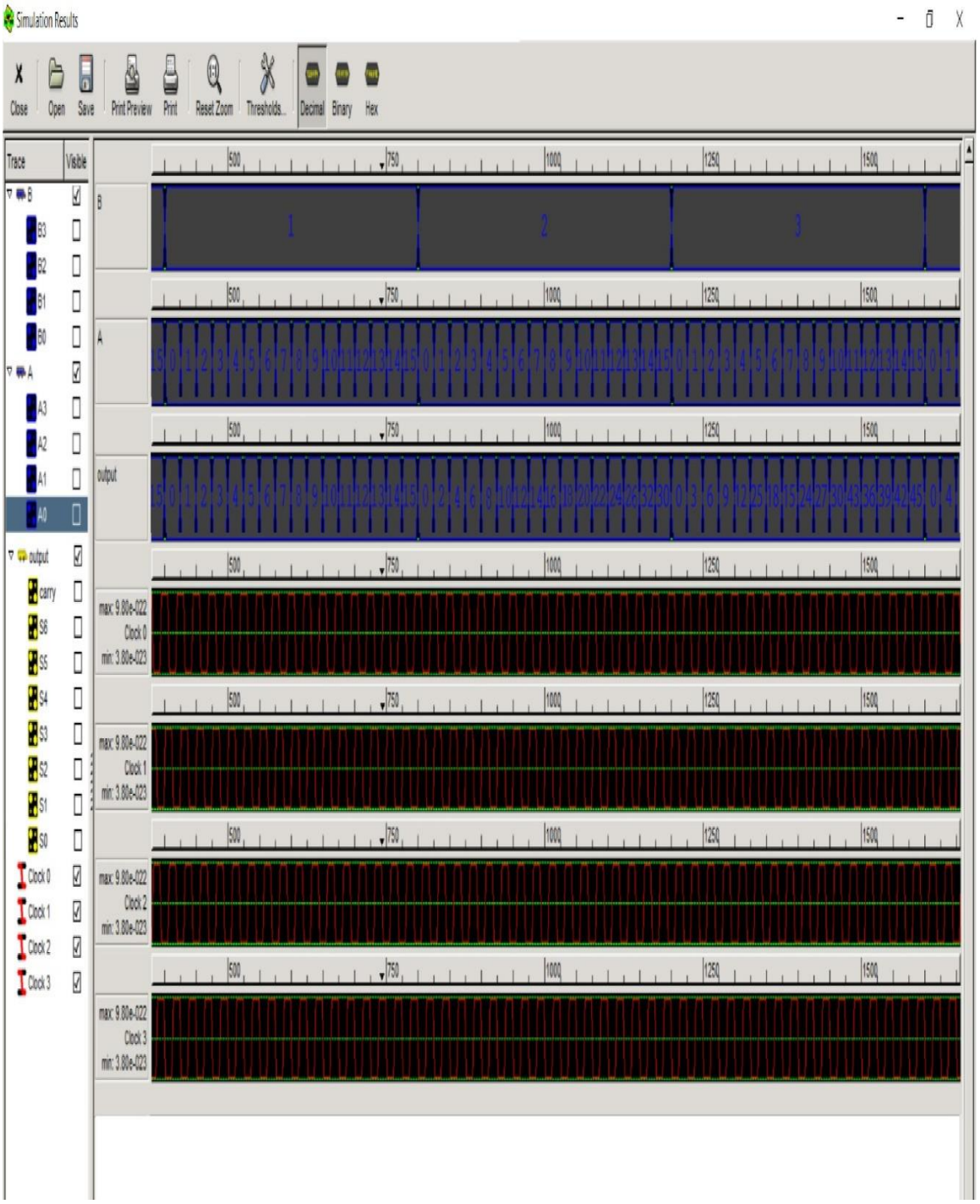

Figure 4.9(a): Simulation Result of 4*4 Multiplier (1-3).

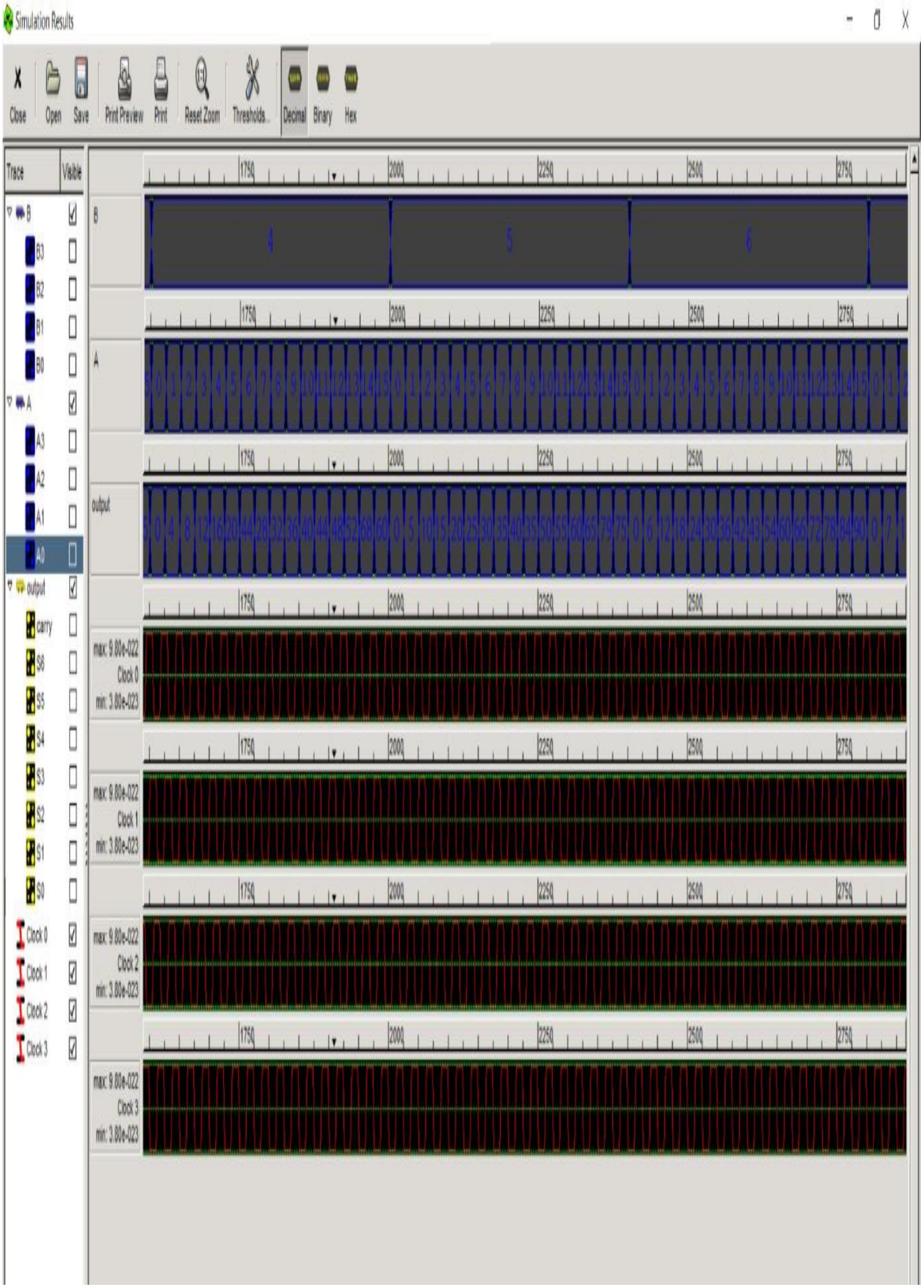

Figure 4.9(b): Simulation Result of 4*4 Multiplier (4-6).

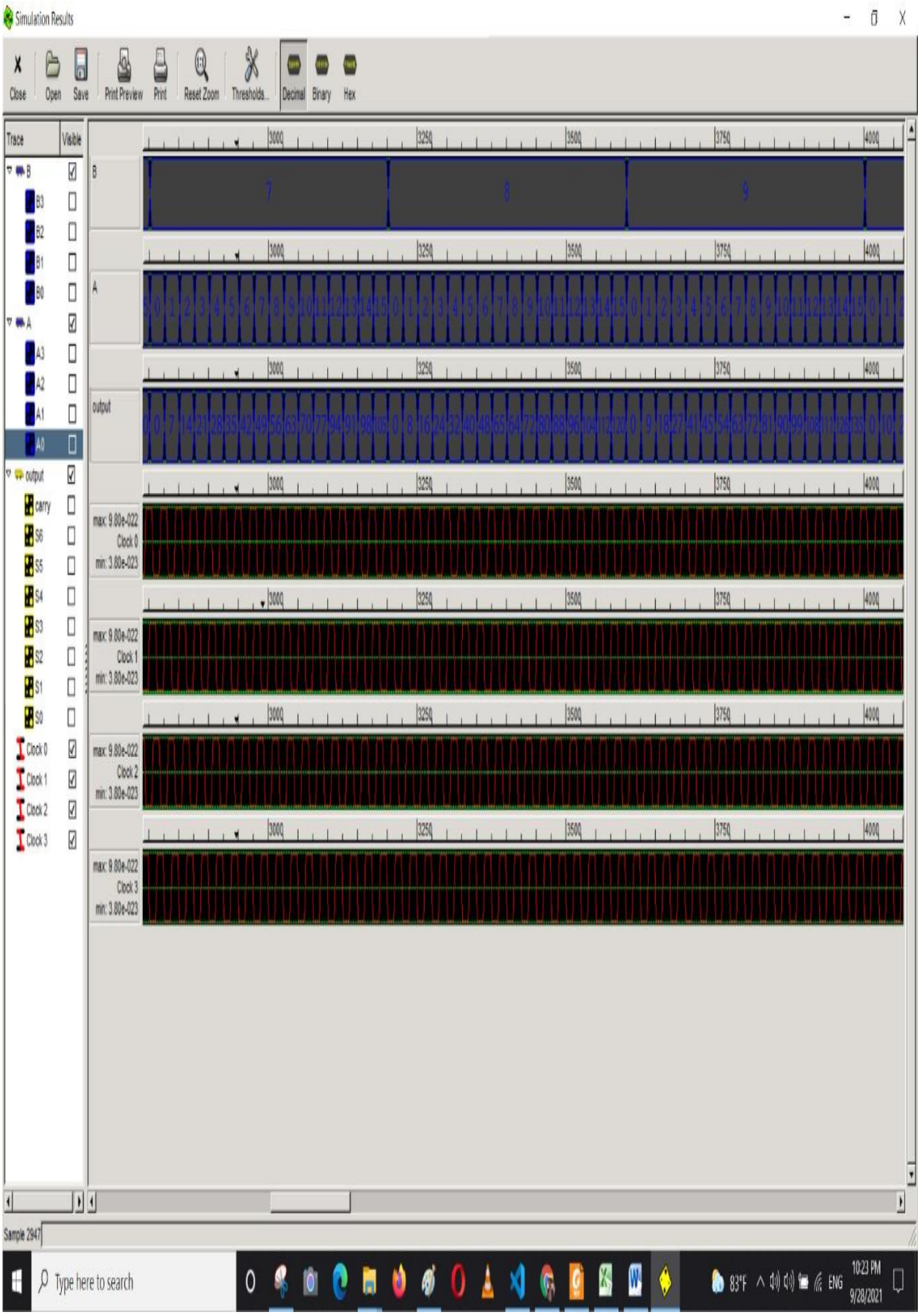

Figure 4.9(c): Simulation Result of 4*4 Multiplier (7-9).

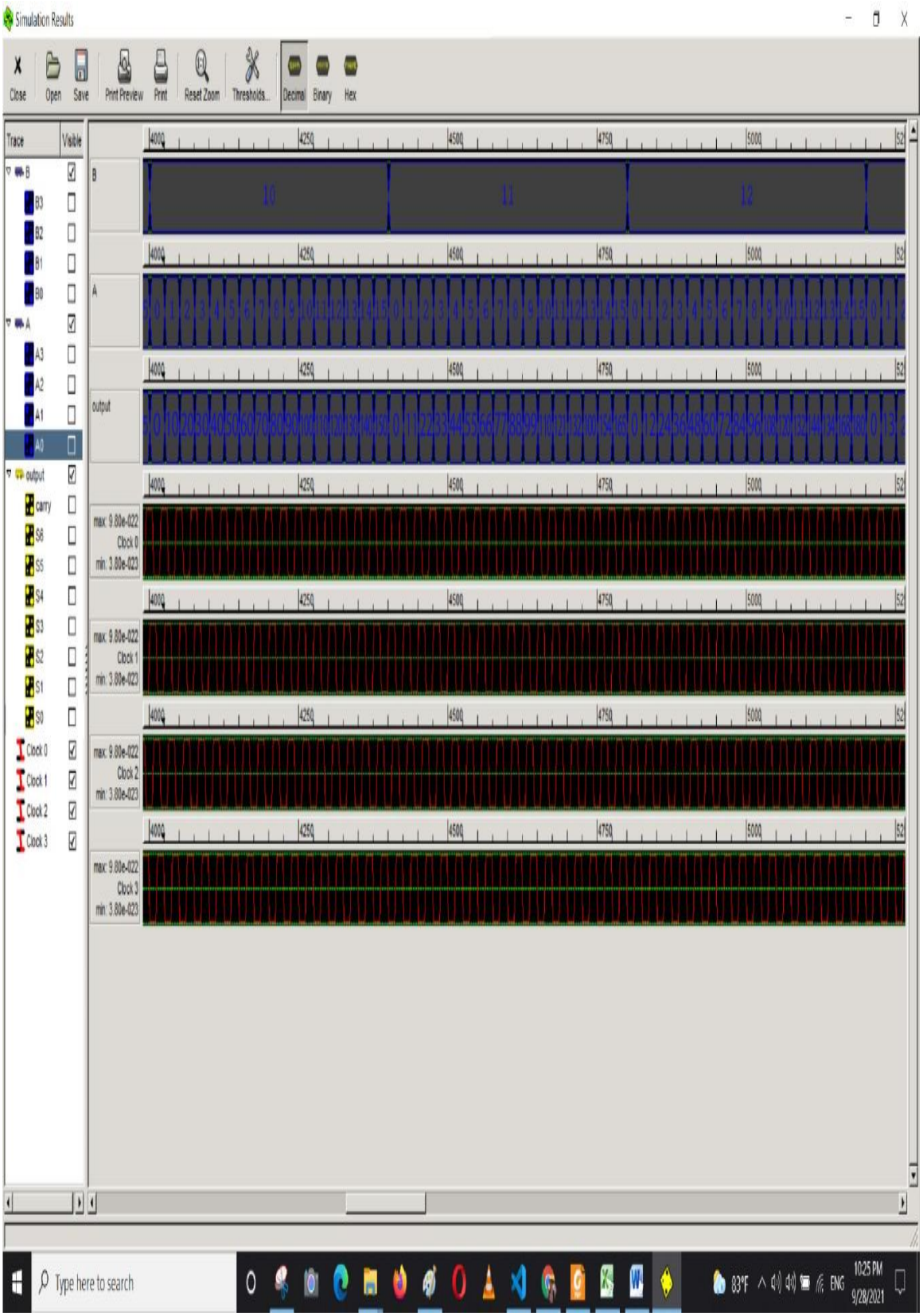

Figure 4.9(d): Simulation Result of 4*4 Multiplier (10-12).

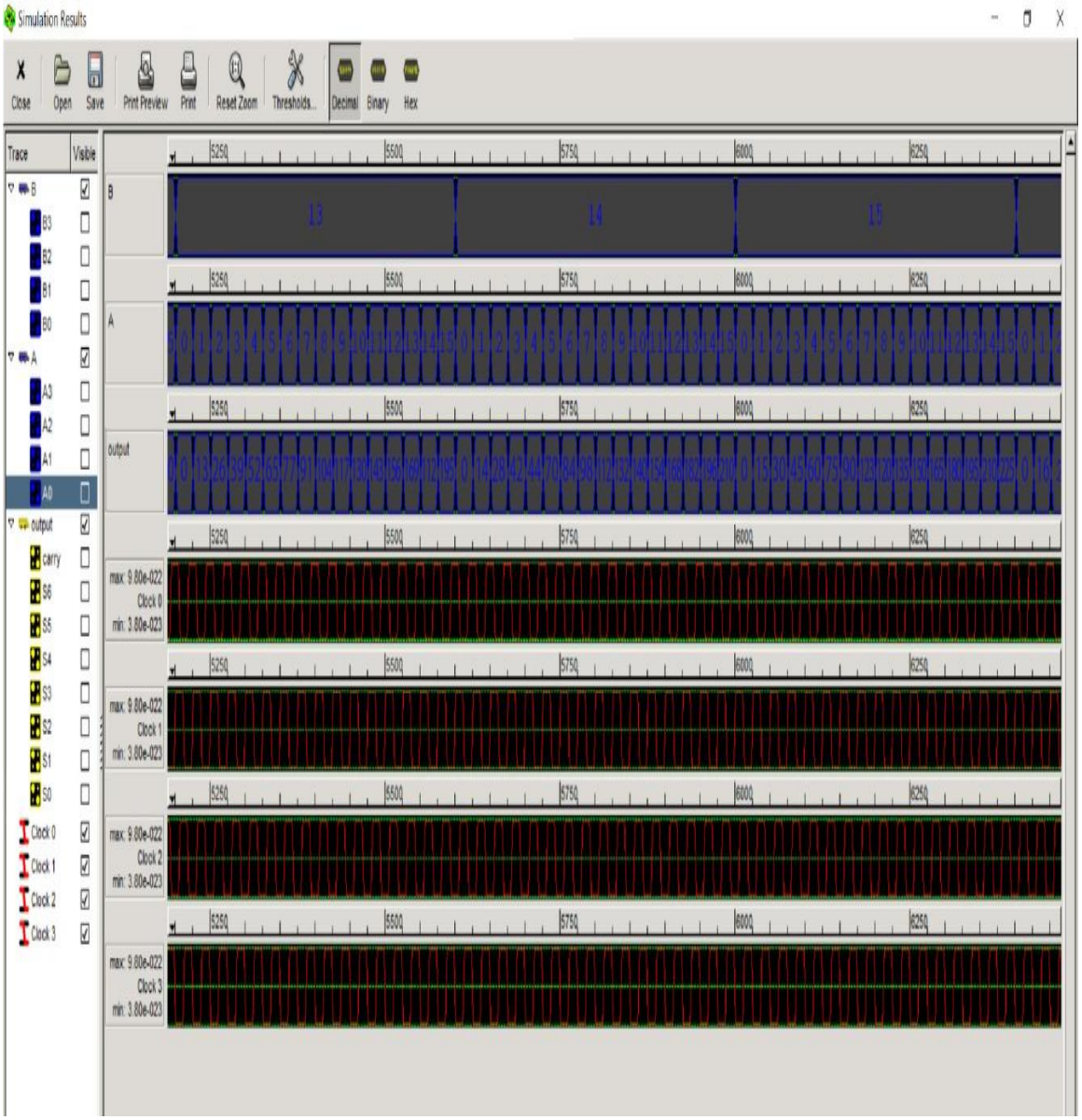

Figure 4.9(e): Simulation Result of 4*4 Multiplier (13-15).

4.8 Result Analysis

The 4*4 multiplier requires 128 inputs to design. Fortunately, we've discovered a complete adder design [7] that greatly aids us in reducing the number of cells and achieving our goal. Every parameter has its value set to the default in this program. QCA developer 2.0.3 uses cells with a diameter of 18 nm (nanometers). When the distance between cells is increased, the size rises to 20nm. Compared to earlier multiplier designs, which used cell counts of 2756 [3], 1955 [1], ours uses 1739 total cell counts.

As you can see in equation 4.1, the area-based formula comes into play. Maximum longitudinal and transverse cell numbers are multiplied here. m2 is the suggested multiplier's size in terms of surface area. The equation is the necessary equation to calculate the multiplier's surface area (4.1).

$$Area = Lm * Tm \quad (4.1)$$

Where,

Lm = Maximum longitudinal cell numbers

Tm = Maximum Transversal Cell Numbers.

Delay is evaluated by no. of clocking zones from input to output following a critical path. Delay is calculated in no. of cycles and no. of clock zones for CMOS and QCA. Each clocking zone gives ¼ unit cycle of delay where four clocking zone provides one cycle delay. The numbers of clocking zone haven't been assured yet. As a result, we aren't sure about the delay time. We are working on it & find the result soon.

4.9 Comparison of Different Multipliers

Comparison of or proposed multiplier against existing multiplier is given –

Table 4.1: Comparison of Referenced Multipliers against Proposed Multiplier.

Reference	Cell Count	Area	Delay Time	Cost Function	Comment
4*4Binary Multiplier[4]	2756	5.78	8.50	2709.38	Good
4*4 Vedic Multiplier[2]	1955	2.25	4.25	318.45	Best
Proposed Multiplier	1739	2.41	2.25	389.81	Better

Regarding the 4*4 Binary Multiplier and 4*4 Vedic Multiplier, our proposed multiplier has less cell count, less area, and the delay time has also been reduced. Still, the cost function has greater than others, So it is good.

4.9.1 Area (A)

In QCA, the number of cells is comparable to the number of transistors in CMOS. The area is proportional to the number of cells. The area is used to determine the circuit's complexity. The larger the area of the circuit, the more complicated it is. Cells make up the logic components, such as majority voter gates and inverter gates and binary wires. The area influences the radius effects of the circuit. [50]

4.9.2 Delay (D)

The number of clocking zones from input to output along the critical path is used to determine delay. It's a crucial metric for assessing circuit performance. In comparison, the performance of a circuit with fewer clocking zones is better. For CMOS and QCA, the delay is measured in cycles and clock zones, respectively. Figure 4.10 shows how each clocking zone provides a 14-unit-cycle delay, whereas four clocking zones create a one-cycle delay. [51]

4.9.3 Set/Reset Ability (SR)

The ability to set/reset is a crucial parameter in a Multiplier circuit. The necessity of a Multiplier circuit's Set/Reset capability is an essential consideration when choosing the optimal Multiplier circuit for QCA technology. Set indicates that the output is flipped to the logic one state, whereas Reset indicates that the output has flopped to the logic 0 states, independent of the input logic. [52]

4.9.4 Cost Function of CMOS

The CMOS cost function is dominated by area, latency, and power dissipation. Because of technological advancements, the focus on the area is waning. For CMOS technology, Thompson presented a cost function. The following is the cost function equation, which is followed by equation (4.2):

$$Cost\ Function\ Area{-}Delay = A \times Tp;\ 0 \leq p \leq 2 \quad (4.2)$$

A is for the area, T is for the delay in the cycle, p is for weightings. The minimum unit for the delay is ¼ cycle is equivalent to a clocking zone.

The cost function for power dissipation is calculated by equation (4.3) given in the following:

$$Cost\ Function\ Power{-}Delay = Pm \times Tn \quad (4.3)$$

Where,

P is the power dissipation, and

T is the delay in a cycle; m, n is the weightings. [42]

4.9.5 Cost Function of QCA

Some cost function equation parameters include the majority voter gate, inverter gate, crossover, and delay. In the equation, the irreversible power dissipation, manufacturing complexity, and response are measured using the majority voter gate, crossover, and delay

parameters, respectively. The inverter gate is used to evaluate the circuit's complexity. The number of logic gates and crossovers are better criteria for determining the complexity of a QCA circuit. The three primitives: majority gates, inverters, and crossovers, add up to the circuit complexity of QCA. The cost function of a QCA circuit is measured in this paper using the number of logic gates and crossings.

$$Cost\ Function,\ CA = (MV3k + I + Cl) \times Tp \text{ k, l, p} \geq 1 \quad (4.4)$$

MV3 is the number of three input majority voter gates, MV5 is the number of five input majority gates. F is the ratio of the number of cells under five input majority gates to three input majority gates. I am the number of inverter gates. C is the number of crossovers. Here k, l, p are the weightings that can be adjusted depending on optimization goals. The weightings of the inverter gate being '1' provide only complexity in the QCA circuit.

4.9.6 Calculation of Cost Function

To calculate the cost function of a QCA circuit as per the requirement, proposed design 4*4 multiplier have 34 MV3 gate, 0 inverter gate and 35 cross over. From the proposed equation (4.4),

Cost Function of QCA = (MV3k+ I + Cl) × Tp, k, l, p ≥ 1

= (441 + 0 + 33) × (2.25)2

= 389.8125

The value of weightings k & p is taken as 1 & 2, respectively. Weightings here are adjusted depending on the optimization goals. In the proposed 4*4 multiplier design, the number of inverter gates is 0 as there was not any requirement of it. The required MV3 gate and crossover numbers are 34 and 35. These are shown in Figures 4.10 (a) and 4.10 (b), respectively.

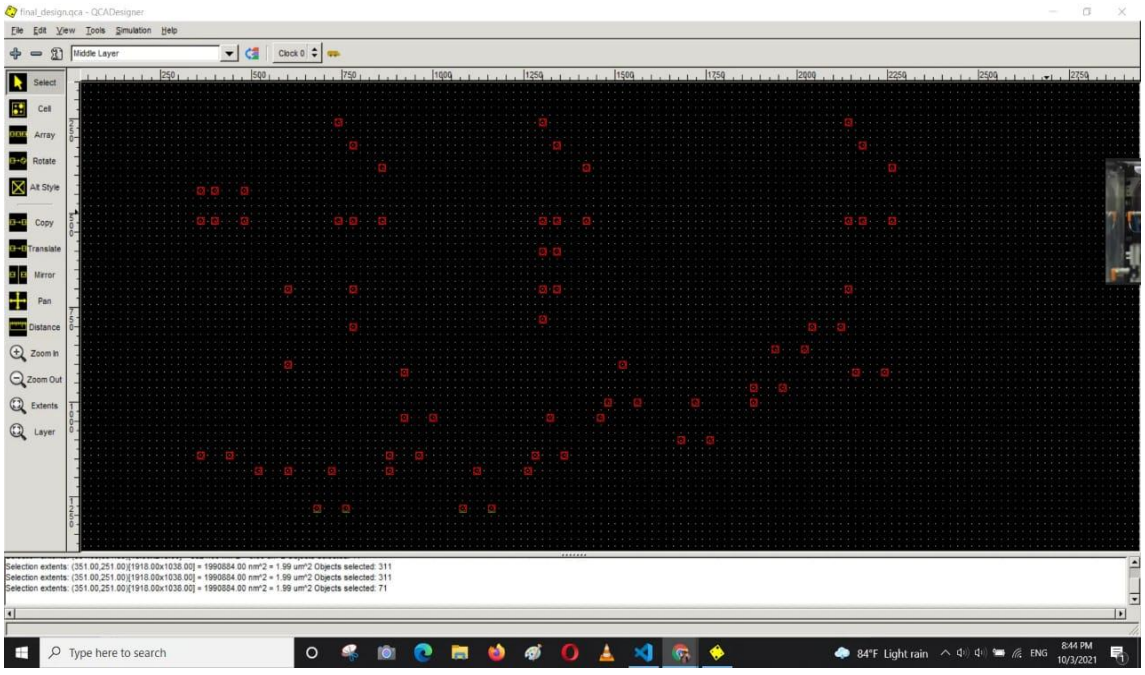

Figure 4.10 (a): Number of Logic Gates in Proposed 4*4 Multiplier.

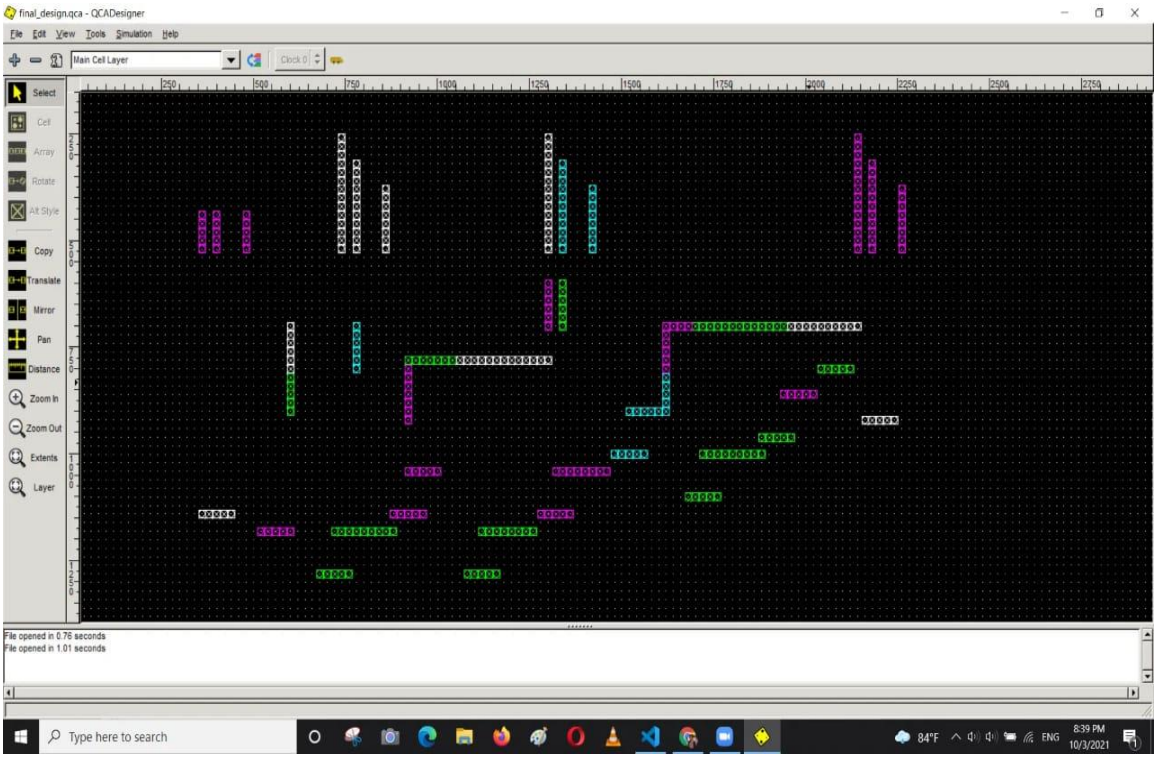

Figure 4.10 (b): Number of Crossover in Proposed 4*4 Multiplier.

4.10 Crossover for Cost Function

In the referenced paper of 4*4Binary Multiplier [4] and 4*4 Vedic Multiplier [2], the KPI parameters like area, cell count, delay time are determined for comparison with the proposed 4*4 multiplier. The table 4.1 displays the values of the referenced multiplier.

4.10.1 Performance Analysis of Full Adder

The circuit's performance is assessed by looking at Data Table-I. For each indicator, the best, better, and good designs are highlighted in red, green, and blue, respectively. In terms of KPI, the design given in [26] performs the best. One disadvantage of the design in [26] is the layered kind. When the designs in [25] and [27] are compared, most of the KPIs, such as delay, cell count, and several gates, are similar to those in [25], but the design in [27] lacks any crossover, including coplanar crossover. The design in [25], on the other hand, has a multilayer sort of crossover. Coplanar crossover is preferred by QCA technology over multilayer crossover because it is difficult to manufacture. As a result, the design in [27] is deemed superior to [25], and the performance of the design in [25] is deemed satisfactory.

4.10.2 Performance Analysis of Multiplier Circuit

In Data Table-II, it can be observed that the performance of design [32] is the best of all designs because all KPIs in this design have the lowest value. It also offers the ability to

Set/Reset. As a result, it has been designated as the most acceptable approach. The design in [33]b is hence deemed superior. The KPI is lower than it should be. In this design, a 2D clocking mechanism is used to alleviate the thermodynamics effect caused by the longest wire. The design delay in [32] is similar to [33]b for having the most minor other parameters such as cell count, number of gates, and number of clock zones, but the design delay in [33]b is similar to [32] since it uses a 2D clocking method. As a result, the design in [33]b is superior to [32]. The design [39] is also fantastic.

In conclusion, data analysis shows that many KPIs can influence a KPI. The same KPI may have the same value in two designs, but the reasons are different. The delay of a design can be impacted by cell count, gate count, crossover type, and other factors. The clocking technique can alter the delay in another design, but the latency in both designs is the same.

4.10.3 An Overall Picture of the Interrelationships between KPIs

Data analysis has resulted in the creation of a flow chart. This flow chart depicts the interrelationships between the KPIs depicted in the figure. The majority voter gate provides the intricacy in the circuit, AND, OR, NOT gate, and Crossover. The majority voter gate AND OR gate all disperse irrevocable power as a result. The difficulty of fabrication is a worry for Crossover. [42] Because cell counts are a measure of the circuit's area, they impact the circuit's delay. Furthermore, the number of clocking zones is determined by the design clocking method. As a result, the number of clocking zones measures a circuit's delay. Delay is an essential KPI, it might be argued. The flow chart will reveal the conclusion. The delay box is touched by two arrows from the area and several clocking zones boxes. Some clocking schemes include a feedback route to improve signal propagation and enable steady functioning in temperature fluctuations. [43] The cost function feels the combined effects of area and delay indicators.

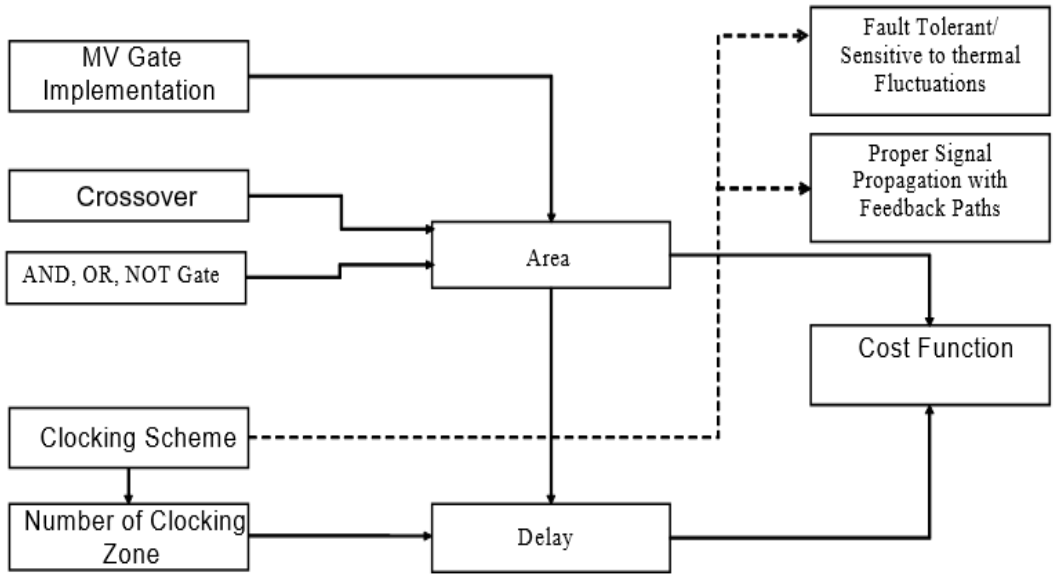

Figure 4.11 An overall picture of the interrelationships between KPIs [43]

Chapter 5
Conclusion

5.1 Summary of Research

Simulation results demonstrate that the multiplier is operating as intended. Total multiplier spread latency is decreased by 20% as expected. Using a binary parallel adder, we've devised a 4x4 multiplier architecture. It was created using QCA Designer to mimic the final product. We were here to design a multiplier circuit which is more efficient than any current multiplier design, which can fulfill requirement like, Reducing cell Numbers: Reduced cell numbers 63% compare with Binary Multiplier and 88% compare with Vedic Multiplier, Reducing Area: Reduced area 41% compare with Binary Multiplier and 56% compare with Vedic Multiplier, Reducing Delay Time: Reduced latency or delay time 26% compare with Binary Multiplier and 52% compare with Vedic Multiplier.

Compared to the 4x4 Vedic and Binary multiplier, the simulation indicates a 60 per cent decrease in cell count, a 30 per cent reduction in area, and a 20 per cent reduction in latency. Reduced cell numbers, therefore, contribute directly to low power usage. QCA Design Community discussion indicates that QCA Designer's multiplier simulation can lead to hard reproduced outcomes. Validating these findings might begin with an alternative modelling approach.

5.2 Future Work

In the future, those who want to do a more complicated multiplier project using QCA or who want to construct more input circuits might use this thesis as a reference. Larger circuits, such as 18 * 16, 32 * 32, 64 * 64, 128 * 128, and so on, maybe conceivable in the future with the information obtained from this thesis. Working with a 4 * 4 divider circuit or any other large divider circuit will be a lot easier now that you know this information. With a medium or more extensive size circuit, more work can be done to simplify nanotechnology while allowing for new creative possibilities.

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