Accurate Drain Current Modeling of Long Channel Junctionless Double-Gate Field Effect Transistor

by

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The thesis entitled **Accurate Drain Current Modeling of Long Channel Junctionless Double-Gate Field Effect Transistor** Submitted by Shuvro Chowdhury, Student No.: 0411062261, Session: April, 2011 has been accepted as satisfactory in partial fulfillment of the requirement for the degree of MASTER OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING on December 24, 2014.

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_____

Shuvro Chowdhury

"***Research is to see what everybody else has seen, and to think what nobody else has thought.***"

Albert Szent-Györgi (1893-1986), U. S. biochemist.

Dedicated to

My parents and my beloved wife-
who supported me each step of the way

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ABSTRACT

A new model based on linear depletion inside the channel region has been proposed for long channel Junctionless Double Gate (JL DG) MOSFETs. The proposed model shows improved performance over the previous models based on abrupt depletion. This new model provides a different way to determine surface potential of JL DG MOSFETs. The model based on gradual depletion provides different sets of equations for surface potential which are valid for different regions of operations. Thus there is a trade-off between accuracy and complexity in using the proposed model. Having the knowledge of surface potential, the proposed model obtains expressions for current and threshold voltage. The current expressions have been evaluated using numerical techniques. Surface potential characteristics and current voltage characteristics are found to have smooth transition between fully depleted region and partially depleted region. This smoothness may prove useful for SPICE like programs. Capacitance-voltage characteristics, output conductance and transconductance characteristics have also been observed, analyzed and compared against the results obtained from TCAD simulations. Upon comparison, it has been found that the results obtained from proposed model matches quite perfectly with the results provided by TCAD tool. Finally the effects of different device and process parameters on threshold voltage of the JL DG device and the sensitivities of threshold voltage on these parameters have been explored and analyzed. It has been observed that threshold voltage of JL DG MOSFET is very sensitive to parameter variations which would require proper control of geometry and impurity concentration.

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LIST OF ABBREVIATIONS

ASIC	**A**pplication **S**pecific **I**ntegrated **C**ircuit
BOX	**B**uried **O**xide
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
DG	**D**ouble **G**ate
GAA	**G**ate **A**ll **A**round
IC	**I**ntegrated **C**ircuit
ITRS	**I**nternational **T**echnological **R**oadmap for **S**emiconductors
JL	**J**unction **L**ess
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
MuGFET	**Mu**ltiple **G**ate **F**ield **E**ffect **T**ransistor
PD	**P**artially **D**epleted
FD	**F**ully **D**epleted
SOI	**S**ilicon **O**n **I**nsulator
TCAD	**T**echnology **C**omputer **A**ided **Design**

PHYSICAL CONSTANTS

Boltzmann's Constant	k_B	=	1.38×10^{-23} JK^{-1} (exact)
Permittivity of Free Space	ϵ_0	=	8.854×10^{-12} Fm^{-1} (exact)
Mass of a Free Electron	m_0	=	9.109×10^{-31} kg (exact)
Charge of an Electron	q	=	1.6×10^{-19} C (exact)
Planck's Constant	h	=	6.626×10^{-34} Js (exact)
Reduced Planck's Constant	$\hbar$	=	1.055×10^{-34} Js (exact)

LIST OF SYMBOLS

T	Absolute temperature	K
t_{ox}	Thickness of gate oxide	m
t_{Si}	Thickness of channel/film	m
V_G	Applied gate voltage	V
V_G^{eff}	Effective gate voltage	V
V_{FB}	Flatband voltage	V
v_T	Thermal voltage	V
L	Channel length	m
W	Device width	m
ρ	Charge density	Cm^{-3}
N_A	Acceptor doping concentration	m^{-3}
N_D	Donor doping concentration	m^{-3}
p	Hole concentration	m^{-3}
n	Electron concentration	m^{-3}
n_0	Electron concentration at flatband condition	m^{-3}
ϕ	Electrostatic potential	V
ϕ_{ox}	Voltage drop across gate oxide	V
ϕ_s	Surface potential	V
$\phi_{substrate}$	Workfunction of the substrate	V
ϕ_{gate}	Workfunction of the gate material	V
ϕ_{MS}	Workfunction difference between substrate and gate material	V
Q_{SC}	Surface charge per unit area	Cm^{-1}
Q_m	Mobile charge density per unit area	Cm^{-1}

Q_d	Fixed charge density per unit area	Cm^{-1}
ϵ_{ox}	Dielectric constant of gate oxide	null
ϵ_{Si}	Dielectric constant of channel/film	null
V	Quasi-Fermi potential	V
x	Position variable along x-direction	m
y	Position variable along y-direction	m
x_d	Depletion width	m
E	Magnitude of electric field intensity	Vm^{-1}
E_s	Surface electric field intensity	Vm^{-1}
C_{ox}	Gate oxide capacitance per unit area	Fm^{-2}
C_{Si}	Channel capacitance per unit area	Fm^{-2}
C_{eff}	Effective MOS capacitance per unit area	Fm^{-2}
V_{TH}	Threshold voltage	V
p	Normalized position variable along x-direction	null
u	Normalized electrostatic potential	null
u_s	Normalized surface potential	null
λ_D	Debye length	m
E_n	Normalized electric field intensity	null
E_{sn}	Normalized surface electric field intensity	null
v	Normalized quasi Fermi potential	null
ΔV_{TH}	Threshold voltage shift	V
V_S	Source voltage	V
V_D	Drain voltage	V
V_{GS}	Gate to source voltage	V
V_{DS}	Drain to source voltage	V
I_{DS}	Drain to source current	A
μ	Carrier mobility	$\mathrm{m}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$
P	Normalized half-channel thickness	null
u_c	Normalized potential of the axis of symmetry	null

g_m	Transconductance	S
g_d	Output conductance	S

1. INTRODUCTION

In the integrated circuit (IC) technology, the excessive down-scaling of transistor dimensions has been successfully carried on over the last 30 years. This continued scaling down has made dense packaging easier and improvement in performance of the integrated devices [3, 4]. For the last three decades, progress in device scaling has followed an exponential curve: device density on a microprocessor doubles every three years. This has come to be known as Moore's law [5]. The term device used here specifically refers to Metal Oxide Semiconductor Field Effect Transistor (MOSFET). According to the International Technological Roadmap for Semiconductors (ITRS) [1], the physical gate length (L_g) of the MOS transistor will shrink to 17 nm by the year 2015 as shown in Table 1.1.

Table 1.1: ITRS 2013 predicted feature size and physical gate length for long term period. [source: ITRS 2013 [1]].

Year of Production	2013	2015	2017	2019	2021	2023	2025	2028
DRAM half pitch[a](nm)	28	24	20	17	14	12	10	7.7
FLASH half pitch (nm)	18	15	13	11	9	8	8	8
MPU[b] physical gate length (nm)	20	17	14	12	10	8	7	5

[a]half the distance between cells in a dynamic RAM memory chip.

[b]Memory Protection Unit (MPU): the management unit in the processor responsible for shielding of system resources and tasks from unwanted access

There are a number of benefits of scaling MOSFETs down. First of all, the cost per device manufacturing is reduced as a each MOSFET occupies less area. Secondly, more transistors can be integrated on the chip, therefore, the integrated chip can perform more complex functions with less amount of time. The third advantage of scaling down is that capacitances of MOSFETs are reduced, which in turn reduces the time and power required to switch a transistor. Despite its potential advantages, scaling down is accompanied by a series of challenges to device design.

As the device is scaled down, a number of problems obstruct normal behavior of MOSFETs. Firstly, the MOSFET characteristics degrade with the reduction in size. Two key characteristics are threshold voltage (V_{th}) and subthreshold swing, known as short-channel effects (SCEs). Threshold voltage increases because of two-dimensional (2D) electrostatic charge confinement in the active region (channel) of the MOSFET [6]. Increase in threshold voltage increases the supply voltage requirement (V_{dd}). Hence power consumption increases by substantial amount.

Secondly, as the gate length (L_g) is reduced, power consumption of the device increases at high frequency operation. For the same applied bias (V_{dd}), the current is higher for short channel devices. Therefore, the heat generation by a high frequency silicon chip is tremendously high, and the cooling of the chip becomes difficult and, sometimes, practically impossible for some low-power applications without implementing expensive ionic cooling system [7]. Supply voltage (V_{dd}) reduction is an effective method to reduce the power consumption per device. However, lowering power supply voltage reduces the operational speed of MOSFETs. Hence, controlling power consumption has been a primary concern in MOSFET scaling.

Thirdly, decrease in gate length (L_g) introduces other short channel effects (SCEs) which significantly modify device operational behavior e.g. switching and amplifying characteristics. Some significant effects are (1) drain induced barrier lowering (DIBL), (2) reverse SCE, (3) field dependent mobility, (4) velocity saturation and

velocity overshoot, (5) gate induced drain leakage (GIDL), (6) channel length modulation (CLM), (7) Poly silicon gate depletion effect, (8) self-heating effect etc. [8] All these degrade the device performance.

Fourth major aspect of device scaling is excessive reduction in device layers' widths such as gate-oxide thickness (t_{ox}), diffusion width (t_{diff}), channel width (t_{ch}), gate material width (t_g) etc. Decreasing the oxide layer thickness (t_{ox}) causes high leakage through the gate oxide [9]. This also reduces the threshold voltage and hence increases subthreshold swing (S). This is detrimental to device performance since standby power consumption increases significantly.

Fifth vital challenge of scaling down is processing of devices. Decreasing channel demands highly sophisticated and controlled development of masks, features, projection equipment to fabrication laboratories (FLABs). Short channel requires ultra-shallow junction [10] formation which is a great challenge for fabrication labs. Development of extremely thin and uniform gate oxide (t_{ox}) without affecting oxide-channel boundary is also a matter of concern. Sometimes surface roughness becomes so dominant compared to oxide thickness that the device performance follows a declivity.

Finally, the secondary effects emerging out of scaling down of device dimensions require complex analysis and simulation techniques other than existing long channel compact models. The analysis of such nanoscale miniaturized devices require pure quantum mechanical treatment of electronic characteristics [11]. Incorporating the secondary effects demand involvement of complex physics in the simulation processes [12]. Device engineers are continuously exploring new phenomena through researches and new techniques are being discovered day by day.

In this work, the characteristics of modified MOS structures have been explored: long channel junctionless double-gate structure. The rationale behind choosing junctionless DG structure rather than conventional bulk MOSFET are explained in the subsequent sections.

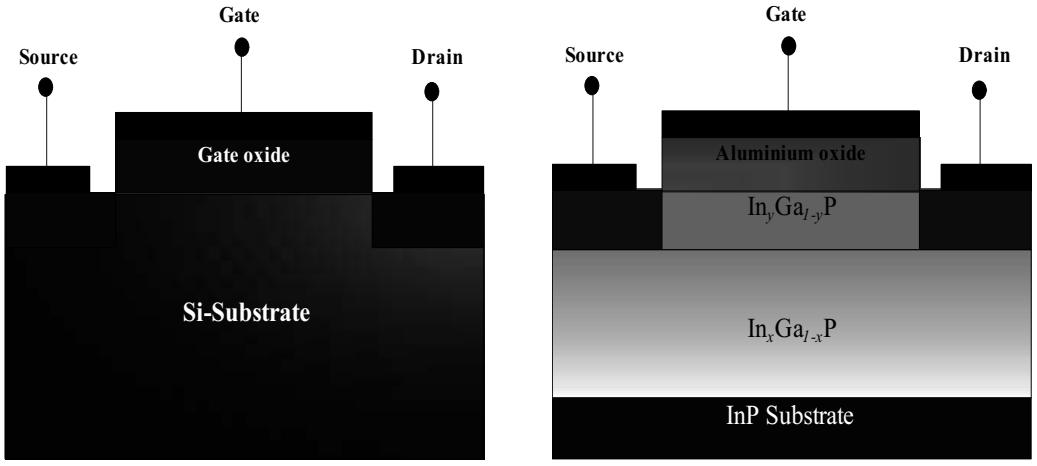
1.1 MOS Performance Improvement

As stated earlier, scaling down MOS transistors introduces many challenges in device design, manufacturing and analysis; alternate processes of devices' performance improvement are being indispensable day by day. Though there is no hard line boundary for device scaling limit, complexities associated with device scaling are increasing noticeably. This warns that the device design methodology is about to reach the scaling limit and about to cross the fundamental limits of semiconductor physics. Therefore exploring for new techniques without scaling down has become a top topic of research through the last few years.

Exploring for techniques of device performance improvement has divided the research mainstream into two major groups:

- Material Engineering
- Structural Modification

The first way to improve device performance without scaling is to change the materials of active region, gate dielectric, contact etc. of the device. Many research works are being continuously carried on to explore for new materials as a replacement of the conventional silicon and silicon-dioxide [13–16]. Changeable bandgap, higher mobility, direct semiconductor nature, wide range of variability in composition etc. make III-V compounds an excellent choice for next generation MOSFETs. By using compound semiconductors and carbon nanotubes, MOS operational characteristics can be improved considerably without crossing scaling limit. One of the popular MOS structures composed of III-V semiconductors as proposed in [16] is shown in Fig. 1.1. Recent MOS devices also come with gate oxide with high dielectric constant (κ) and oxide stacks. These also improve MOS performances significantly [17, 18]. The major problems associated with changing materials are manufacturing difficulties and cost. Fabrication industries still favor the conventional silicon and



(a) (b)

Figure 1.1: Schematic structure of (a)Bulk Silicon MOSFET and (b)III-V MOSFET

SiO_2 due to extremely matured growth technique and lost cost manufacturing. The second important way of refraining excessive scaling is to design alternate device structures other than bulk MOSFETs. Many research groups are working on design of efficient device structures. The structural change mainly includes incorporation of multiple gates and change in body structure. An attractive modification in body structure is *Silicon on Insulator* (SOI) structure [19]. This structure has brought about a revolutionary change in the MOS device arena. Continuous researches are proceeding on SOI devices due to its versatile applications. Another modification is migrating from single gate to multiple gate operation. Many multiple gate MOS (MuGFETs) structures have been proposed such as DG MOSFETs [20], Tri-gate SOI FETs like FinFETs [21], Gate all around (GAA) MOSFETs [22] etc. Sample multiple gate devices are illustrated in Fig. 1.2.

Although these above mentioned structures show performance improvement but existing fabrication technologies are not that much suitable for these novel structures. From this perspective a new modification in the simple bulk structure has gained much attraction - the junctionless structure. Junctionless structure uses same type and same amount of doping concentration at every point inside the channel and

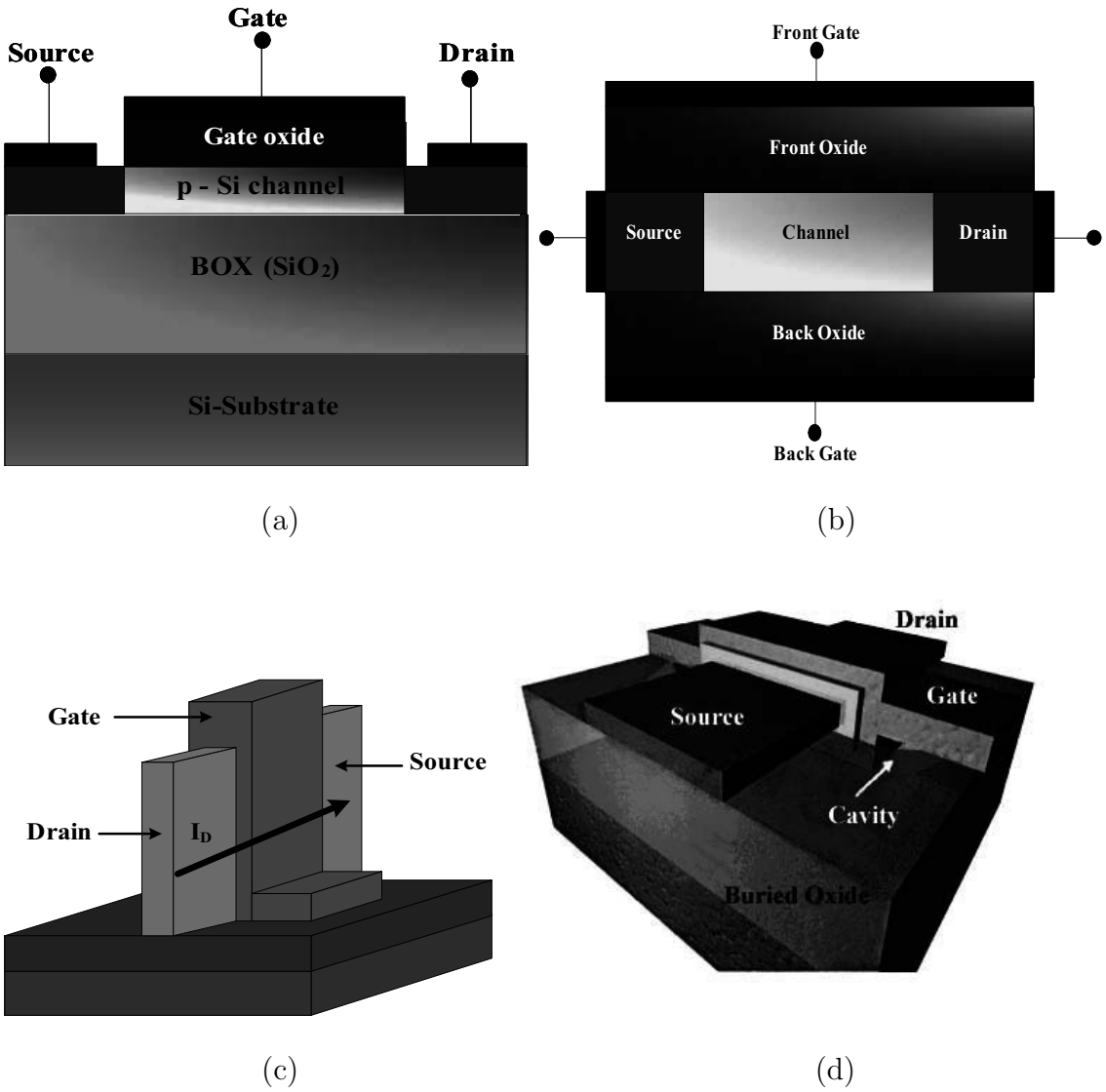


Figure 1.2: Schematic structure of Multiple Gate MOS Devices: (a)SOI Single Gate MOSFET, (b)DG MOSFET, (c) FinFET or Δ Structure and (d) GAA MOSFET

S/D regions and thus offers simple fabrication process for fabrication of these type of devices. Exploring the attractive performance characteristics of junctionless DG structure is one of the motives behind this thesis work.

1.2 Motivation and Work Highlights

Recently, a junctionless (JL) double-gate (DG) field effect transistor (DGFET) (JL DGFET) has been reported [23–25] as a promising candidate for future technology nodes. The fabricated device with a high content of impurity concentration within the channel and source/drain (S/D) regions requires no junctions and exhibits many advantages [26–29], such as the simplified flexible fabrication process, nearly ideal subthreshold slope (SS $\approx$ 60 mV/dec), high ON-OFF current ratio ($I_{\mathrm{ON}}/I_{\mathrm{OFF}} > 10^7$), low S/D series resistance, and small drain-induced barrier lowering. Moreover, the JL transistor shows many interesting characteristics, like conductance oscillations at low temperature [30] and high temperature behavior [31].

1.3 Literature Review

Due to the excellent electrostatic performance of the JL DG MOSFET, it is necessary to develop an accurate model to investigate its theoretical foundations, to better understand the behavior of this device, and to elucidate its strengths and weaknesses. Duarte et al. [32] first proposed a simple bulk current model relying on depletion approximation for the JL DGFET but neglected the accumulation condition. Then, Sallese et al. [33] carried out a space-charge-based model for the JL DG MOSFET to calculate the charge density and drain current, but it may cause convergence problems. Subsequently, Duarte et al. [34] proposed a non-piecewise model for the JL DG MOSFET based on parabolic potential approximation by a uniform charge–potential relationship. However, few studies have been carried out to develop a surface-potential-based compact model for the JL DG MOSFET valid in all regions, which includes a more physical and accurate description of the transistor behavior and is commonly accepted in compact modeling applications. Chen et al. [35] has proposed a surface potential based drain current model for JL DG MOSFET. This model is based on abrupt depletion between depleted and neutral regions and shows discontinuities in surface potential and drain current characteristics.

1.4 Outline of Dissertation

There are in total five chapters in this thesis. The first chapter is an introduction (Chapter 1) to the continuous need for scaling down of MOSFETs and recent advancements in the semiconductor industries. A short discussion about different types of MOSFETs is presented which depicts various ingenious attempts to improve MOSFET performances within the bounds imposed by technology. This introductory chapter also includes the motivation to this work and important highlights followed by a brief overview of current literature about the field of this work.

The second chapter (Chapter 2) considers the structure and discusses the operational principle of Junctionless (JL) Double Gate (DG) MOSFET devices. Then it provides a detailed basic mathematical theory of operation for long channel JL DG MOSFET available in literature. The theory focuses on the determination of surface potential and provides quantitative expressions for calculating other variables from this surface potential.

A new model has been proposed for long channel JL DG MOSFETs in the next chapter (Chapter 3). This new model is also based on finding the surface potential. While the basic theory is based on the assumption of abrupt depletion, the new model proposes gradual or linear depletion inside the channel. This new model provides significant improvement of accuracy in modeling JL DG MOSFET characteristics over the basic model based on abrupt depletion. This accuracy comes with some complexities in the formulation of modeling equations. With the help of this model, mathematical expressions for different JL DG MOSFET variables of interest have been determined.

The fourth chapter (Chapter 4) presents a list of equations obtained from the analytical models. It also discusses about the numerical simulation techniques used to justify the validity of the proposed model. Numerical simulation incorporates a two dimensional numerical simulation using SILVACO ATLAS - a widely used

Technology Computer-Aided Design (TCAD) tool along with a simple one dimensional Poisson-Boltzmann solver programmed in MATLAB. After that it presents the simulation results obtained from both the analytical and numerical methods. Surface potential profile, current-voltage (I-V) characteristic, charge-voltage (C-V) characteristics have been shown. It investigates the threshold voltage of JL DG MOSFET and its sensitivities on doping concentration and device parameters. It also compares the accuracy of the proposed model with the abrupt-depletion based model and numerical solutions.

With a summary of the work done, the last chapter (Chapter 5) marks the end of this dissertation. It also mentions the scopes for further improvement of the work and provides a suggestion of possible areas which can be explored in future.

2. Basic Operational Theory of JL DG MOSFET

This chapter is devoted to the development of the fundamental operational model for Junctionless Double Gate MOSFET. At first the device structure under consideration is presented which is followed by an explanation of the operational principle of the device. Then a systematic formulation of the working equation of the device will be discussed. A regional approach to the solution of the working equation is obtained next. Finally the ways to calculate the variables of interest e.g., surface potential, surface charge, threshold voltage and drain to source current from the solution of the working equation is discussed.

2.1 Device Description

A one dimensional analysis of an n-channel JL DG MOSFET structure is presented in this chapter. The device structure has been shown in Figure 2.1. The device is assumed to have a channel length L, device width W, channel thickness of t_{Si}, gate oxide thickness t_{ox} and a uniform donor doping concentration N_D within the channel, source and drain regions.

2.2 Junctionless Double Gate MOSFET - Device Operation Principle

An n-channel JL DG MOSFET operates quite differently from the conventional inversion-mode DG counterpart. In the subthreshold region of operation, the gate field pushes all the majority carriers (electrons for an n-channel device) away from

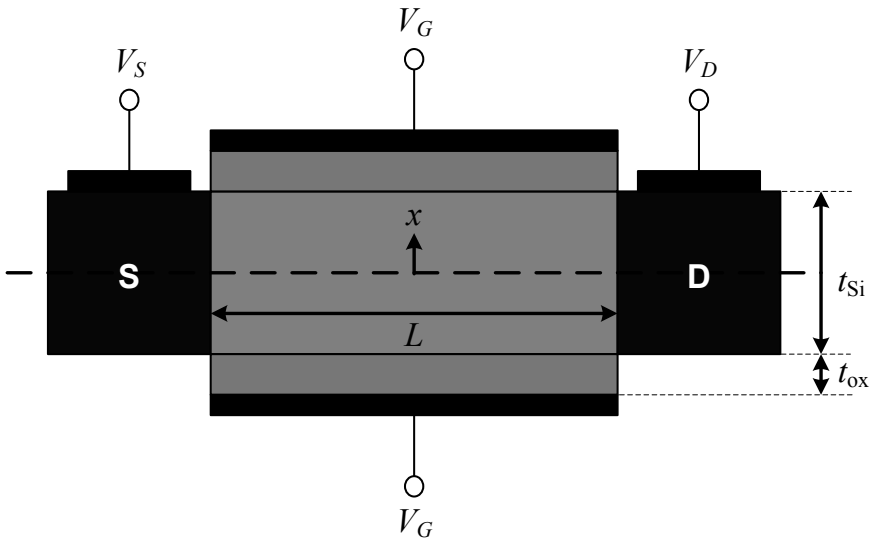


Figure 2.1: JL DG MOSFET structure.

the surfaces leaving the channel/silicon body fully depleted of free carriers, as is shown in figure 2.2. By increasing the gate voltage, the electric field in the channel reduces and the concentration of free carriers starts to rise. At some threshold voltage, the concentration of free carriers is just sufficient enough to form a conducting channel in the center from source to drain. This situation has been shown in figure 2.3 In the above-threshold region, the depletion width in the body decreases, and the conducting channel in the center squeezed by depleted regions near the silicon surface thickens, as is shown in figure 2.4. With continuing increase in gate voltage, a completely neutral channel is gradually created which has been shown in figure 2.5. The bulk current tends to reach its maximum value when the gate voltage increases to flatband voltage. By further increasing the gate voltage, the device eventually forms electron accumulation layers at the surfaces and produces large surface current, as is shown in figure 2.6.

2.3 Formulating the Working Equation

In this section a working equation for an n-channel JL DG MOSFET is developed from the basic MOS capacitor equation and the basic principles of electrostatics. To

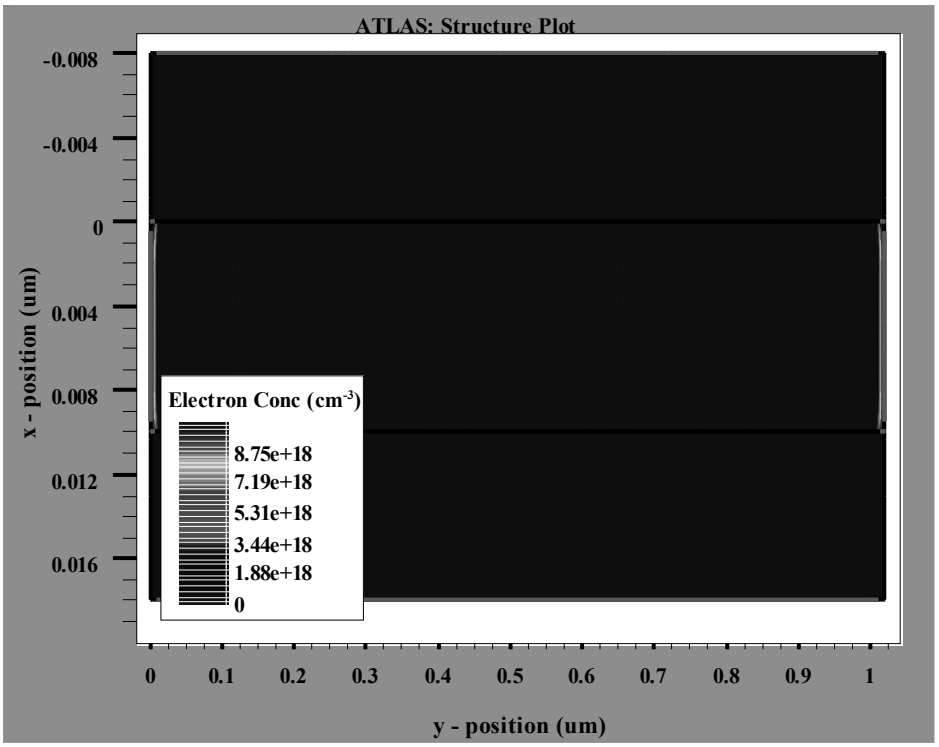


Figure 2.2: Electron density of JL DG MOSFET in the fully depleted mode (when gate voltage is much less than the threshold voltage of the device).

be specific, Boltzmann (or classical) carrier statistics and one dimensional Poisson's equation will play the key role in this formulation.

2.3.1 Basic charge - voltage equations

From the basic MOS capacitor equation it can be written that the applied voltage at gate terminal equals the sum of the voltage drops across the oxide and the semiconductor, i.e.,

$$V_G = V_{FB} + \phi_{ox} + \phi_s \tag{2.1}$$

Here,

V_G = Applied gate voltage

ϕ_s = Surface potential

V_{FB} = Flatband voltage

ϕ_{ox} = Voltage drop across oxide

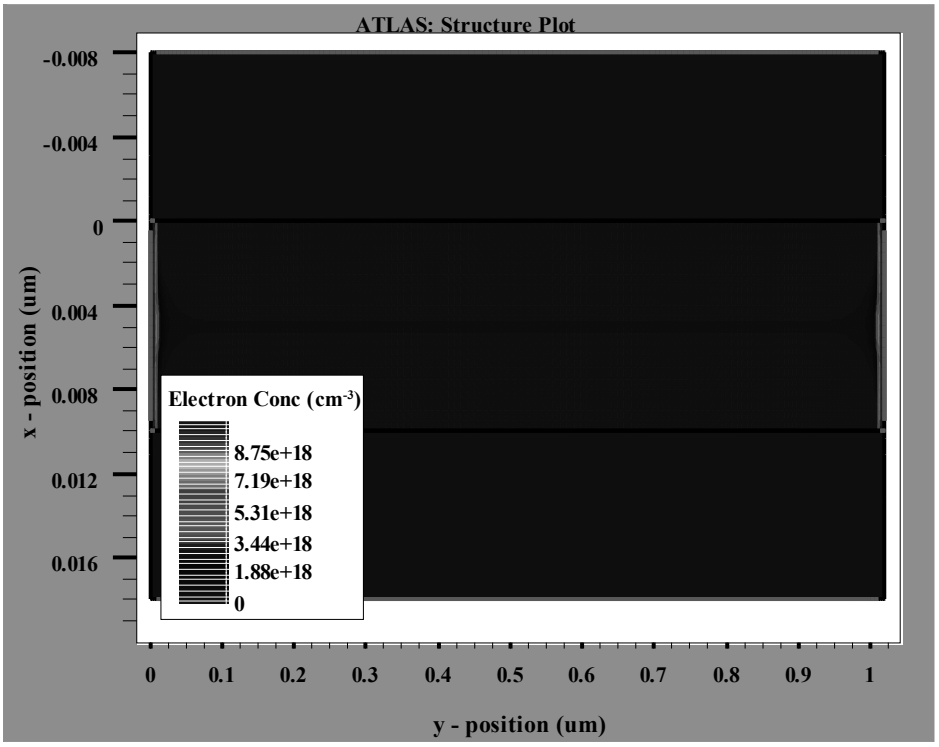


Figure 2.3: Electron density of JL DG MOSFET at threshold voltage (a conducting channel is just formed).

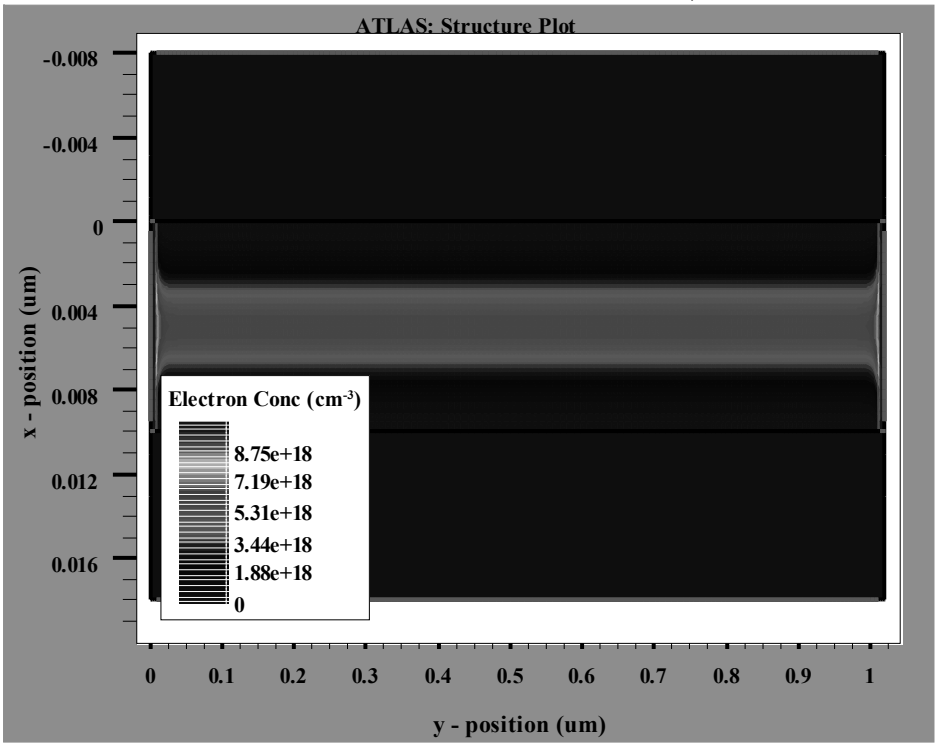


Figure 2.4: Electron density of JL DG MOSFET in the above-threshold region and thickening of the conducting channel.

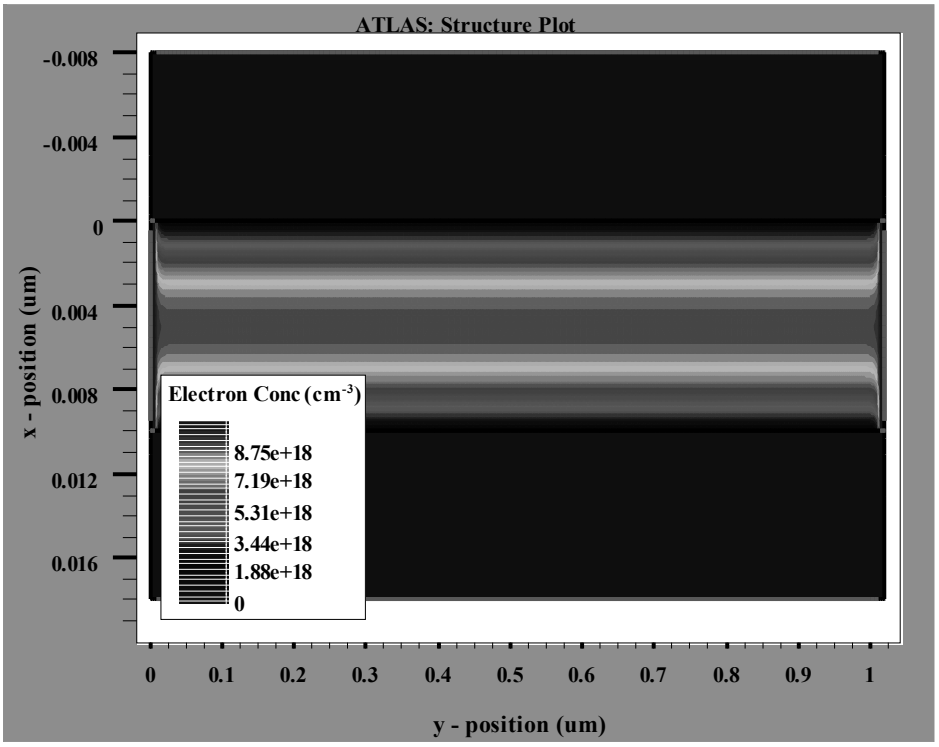


Figure 2.5: Electron density of JL DG MOSFET just below the flatband voltage of the device and the formation of a neutral channel.

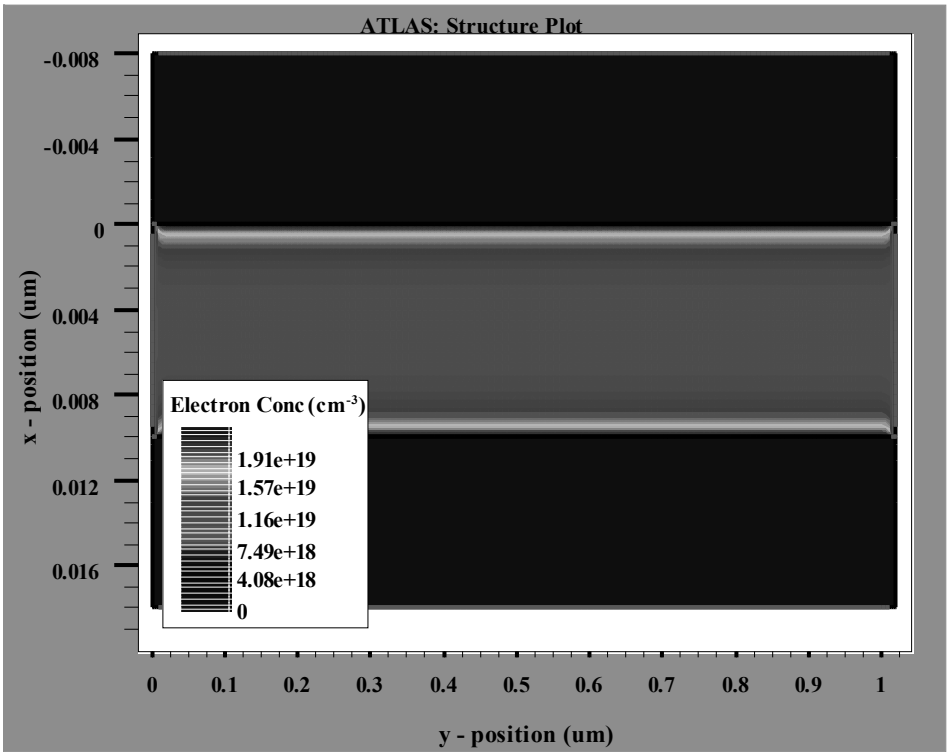


Figure 2.6: Electron density of JL DG MOSFET in the accumulation region and the formation of surface accumulation layers.

If no parasitic oxide charge is assumed and if interface trap charge density is considered to be negligible then flatband voltage, V_{FB} equals the workfunction difference, ϕ_{MS} of the gate material and substrate, i.e.,

$$V_{FB} = \phi_{substrate} - \phi_{gate} = \phi_{MS} \tag{2.2}$$

where, $\phi_{substrate}$ and ϕ_{gate} are workfunctions of the substrate and gate material.

With the same assumption, an expression for voltage drop across the oxide can be obtained as

$$\phi_{ox} = -\frac{Q_{SC}(\phi_s)}{2C_{ox}} \tag{2.3}$$

where,

$$\begin{aligned} Q_{SC} &= \text{Space charge density per unit area} \\ C_{ox} &= \text{Oxide capacitance per unit area} \end{aligned}$$

The reason for negative sign in the r.h.s. is that to get a positive voltage drop, a negative space charge density is required and vice versa.

For JL DG MOSFETs, C_{ox} is given by

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{2.4}$$

where, C_{ox} is the dielectric constant of the gate oxide of the JL DG MOSFET.

Therefore (2.1) can finally be rewritten as

$$V_G = V_{FB} - \frac{Q_{SC}(\phi_s)}{C_{ox}} + \phi_s \tag{2.5}$$

2.3.2 Poisson's equation and Boltzmann's carrier statistics

One dimensional (1D) Poisson's equation is given by

$$\frac{d}{dx}\left(\epsilon_{Si}\frac{d\phi}{dx}\right) = -\rho\left(x\right) \tag{2.6}$$

where x is the *one dimensional position variable*, ϕ is the *electrostatic potential*, ρ is *net charge density* and ϵ_{Si} is the *dielectric constant* of the medium (Silicon for the present analysis). If the medium is isotropic, dielectric constant is same everywhere so Poisson's equation can be rewritten as

$$\epsilon_{Si}\frac{d^2\phi}{dx^2} = -\rho \tag{2.7}$$

For an *extrinsic semiconductor* ρ is given by

$$\rho = q\left(p - n + N_D - N_A\right). \tag{2.8}$$

Here,

$$\begin{aligned} p &= \text{Hole concentration} \\ n &= \text{Electron concentration} \\ N_D &= \text{Donor atom concentration} \\ N_A &= \text{Acceptor atom concentration} \end{aligned}$$

In an n-type doped channel $N_A = 0$. For the sake of simplicity it is also assumed that the hole concentration is negligibly small (i.e., $p = 0$). Therefore, (2.8) is simplified to

$$\rho = q\left(N_D - n\right). \tag{2.9}$$

According to classical model and Boltzmann carrier statistics n is given by,

$$n = n_0 \exp\left[\frac{\phi - V}{V_T}\right] \tag{2.10}$$

where, n_0 is the electron concentration at flatband condition, V is known as *quasi Fermi potential* and V_T is the *thermal voltage* given by

$$v_T = \frac{k_B T}{q} \tag{2.11}$$

which has the value of 0.0259 V at room temperature ($T = 300K$).

For a heavily doped semiconductor $n_0 \simeq N_D$. Substituting all these (2.9) can be rewritten as

$$\rho = qN_D \left[1 - \exp\left(\frac{\phi - V}{V_T}\right)\right]. \tag{2.12}$$

Then using (2.12) in (2.7) and rearranging gives

$$\frac{d^2\phi}{dx^2} = \frac{qN_D}{\epsilon_{si}} \left[\exp\left(\frac{\phi - V}{v_T}\right) - 1\right] \tag{2.13}$$

This is a second order ordinary differential equation. No meaningful information can be obtained from a differential equation unless appropriate boundary conditions are specified. Appropriate boundary conditions required for this device has been discussed in the the next subsection.

2.3.3 Boundary conditions

For the present problem, the boundary conditions are given by

$$\left.\frac{d\phi}{dx}\right|_{x=0} = 0 \tag{2.14}$$

$$\phi\left(\pm\frac{t_{si}}{2}\right) = \phi_s \tag{2.15}$$

The first boundary condition (2.14) is due to the fact that the device under consideration is symmetric, so it is wise to use Neumann boundary condition at this symmetry point. This also reduces the complexity of computation.

The origin of the second boundary condition (2.15) is easy to understand. The value of potential at the surface is directly related to the potential applied at the gate.

2.3.4 Determination of surface charge

The surface charge can be found by applying Gauss's law, i.e.,

$$Q_{SC} = 2\epsilon_{Si} E\Big|_{x=t_{Si}/2} \tag{2.16}$$

The reason for the factor 2 is the DG structure of the MOSFET. Now for 1D case, the *magnitude* of electric field intensity E is related to potential as

$$E = -\frac{d\phi}{dx} \tag{2.17}$$

Finally Q_{SC} can be determined as

$$Q_{SC} = -2\epsilon_{Si} \left.\frac{d\phi}{dx}\right|_{x=\frac{t_{Si}}{2}} \tag{2.18}$$

2.4 Solution of the Working Equation via Approximation

Although simple, unfortunately (2.13) does not have any closed-form analytical solution. An approximate solution can be obtained using a regional approach and taking different simplifying assumptions under depletion and accumulation conditions.

2.4.1 Electric field equation from the working equation

An expression for *electric field*, $E(x)$ can be obtained by integrating (2.13) once. The integration is performed by multiplying both sides of (2.13) by $2\frac{d\phi}{dx}$, i.e.,

$$2\frac{d\phi}{dx}\frac{d^2\phi}{dx^2} = 2\frac{qN_D}{\epsilon_{si}}\left[\exp\left(\frac{\phi - V}{v_T}\right)\frac{d\phi}{dx} - \frac{d\phi}{dx}\right]$$

Now integrating both sides with respect to x as

$$\int_0^{E(x)} 2\frac{d\phi}{dx}\frac{d^2\phi}{dx^2}dx = 2\frac{qN_D}{\epsilon_{Si}}\int_0^{\phi(x)}\left[\exp\left(\frac{\phi - V}{v_T}\right)\frac{d\phi}{dx} - \frac{d\phi}{dx}\right]dx$$

an expression for $E(x)$ can be obtained i.e.,

$$E(x) = \frac{d\phi}{dx} = \sqrt{2\frac{qN_D v_T}{\epsilon_{Si}}\left\{\exp\left[\frac{\phi(x) - V}{v_T}\right] - \exp\left[\frac{\phi(0) - V}{v_T}\right] - \left[\frac{\phi(x) - \phi(0)}{v_T}\right]\right\}} \tag{2.19}$$

Surface electric field, E_s can be found by setting $x = \dfrac{t_{Si}}{2}$,

$$E_s = E\left(\frac{t_{Si}}{2}\right) = \sqrt{2\frac{qN_D v_T}{\epsilon_{Si}}\left\{\exp\left(\frac{\phi_s - V}{v_T}\right) - \exp\left[\frac{\phi(0) - V}{v_T}\right] - \left[\frac{\phi_s - \phi(0)}{v_T}\right]\right\}} \tag{2.20}$$

Unfortunately, further integration of (2.19) is not possible i.e., there is no closed-form expression. Therefore in the following, efforts will be put to obtain approximate analytical solutions.

2.4.2 Approximate solution under accumulation condition

In accumulation region i.e., when $\phi_s > V$ an approximate solution is obtained by expanding the $\exp\left[\dfrac{\phi(0) - V}{v_T}\right]$ term in (2.20) with Taylor's series expansion

$$E_s = \sqrt{2\frac{qN_DV_T}{\epsilon_{Si}}\left\{\exp\left[\frac{\phi_s - V}{v_T}\right] - 1 - \left[\frac{\phi(0) - V}{v_T}\right] - \text{higher order terms} - \phi_s + \phi(0)\right\}}$$

Then neglecting the higher order terms and manipulating a little the approximate expression can be found as

$$E_s \approx \sqrt{2\frac{qN_DV_T}{\epsilon_{Si}}\left[\exp\left(\frac{\phi_s - V}{v_T}\right) - \left(\frac{\phi_s - V}{v_T}\right) - 1\right]} \tag{2.21}$$

In the above approximation a common assumption has been used that in accumulation mode, the electric field drops very quickly and eventually becomes zero. Therefore the electric potential $\phi(x) \approx V$ over an extended region of the device if volume inversion is not considered [35, 36].

Now a further simplification can be achieved by carefully noting that the ratio between the terms $\left[\exp\left(\frac{\phi_s - V}{v_T}\right) - 1\right]$ and $\left(\frac{\phi_s - V}{v_T}\right)$ is greater than unity for aforementioned flatband conditions and becomes unity at flatband. So the term $\left(\frac{\phi_s - V}{v_T}\right)$ is generally neglected in literature and the final approximated electric field expression is obtained as

$$E_s \approx \sqrt{2\frac{qN_DV_T}{\epsilon_{Si}}\left[\exp\left(\frac{\phi_s - V}{v_T}\right) - 1\right]} \tag{2.22}$$

(2.1) can be modified to obtain

$$Q_{SC} = -2C_{ox}(V_G - V_{FB} - \phi_s) \tag{2.23}$$

Combining (2.18) and (2.23) implies

$$-2\epsilon_{Si}E_s = -2\,C_{ox}\,(V_G - V_{FB} - \phi_s) \tag{2.24}$$

Finally, substituting E_s from (2.22) to (2.24), then squaring both sides of the resulting equation and manipulating a little an expression for ϕ_s can be found as

$$\beta v_T \left[\exp\left(\frac{\phi_s - V}{v_T}\right) - 1\right] = (V_G - V_{FB} - \phi_s)^2 \tag{2.25}$$

where

$$\beta = \frac{2q\epsilon_{Si}N_D}{C_{ox}^2} \tag{2.26}$$

2.4.3 Approximate solution under partial depletion condition

In the partly depleted mode, a depletion approximation is taken to derive the $\phi_s - V_G$ relationship for simplicity. Under the coordinates shown in Fig. 2.1, Poisson's equation with depletion approximation translates into

$$\frac{d^2\phi\,(x)}{dx^2} = \begin{cases} 0, & \text{for } \left(-\dfrac{t_{Si}}{2} + x_d\right) < x < \left(\dfrac{t_{Si}}{2} - x_d\right) \\ -\dfrac{qN_D}{\epsilon_{Si}}, & \text{for } x < \left(-\dfrac{t_{Si}}{2} + x_d\right) \text{ or, } x > \left(\dfrac{t_{Si}}{2} - x_d\right) \end{cases}. \tag{2.27}$$

where the depletion width $|x_d| \leq \dfrac{t_{si}}{2}$ as shown in Fig. 2.7.

The upper half of (2.27) can be integrated once from $x = 0$ to $x = x$

$$\int_{\frac{d\phi}{dx}=0}^{\frac{d\phi}{dx}} \frac{d^2\phi\,(x)}{dx^2}\,dx = \int_{x=0}^{x} 0\,dx$$

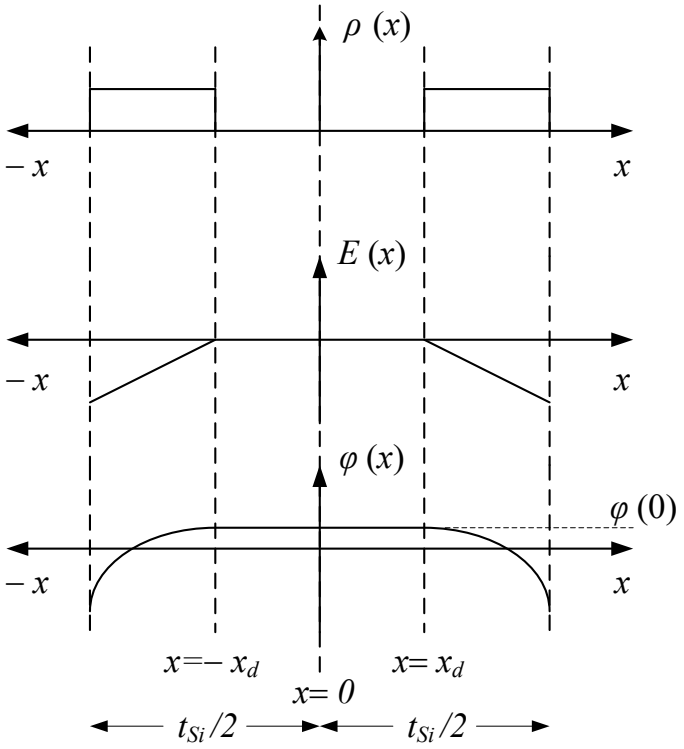


Figure 2.7: Nature of charge, electric field and potential profiles in JL DG MOSFET.

The result of integration is

$$\frac{d\phi\left(x\right)}{dx}=0,\ \text{for}\ \left(-\frac{t_{Si}}{2}+x_d\right)<x<\left(\frac{t_{Si}}{2}-x_d\right) \tag{2.28}$$

Similarly, integrating the lower part of (2.27) once from $x=\dfrac{t_{Si}}{2}-x_d$ to $x=x$ as

$$\int_{\frac{d\phi}{dx}=0}^{\frac{d\phi}{dx}}\frac{d^2\phi\left(x\right)}{dx^2}dx=\int_{x=t_{Si}/2-x_d}^{x}\left(-\frac{qN_D}{\epsilon_{Si}}\right)dx$$

results

$$\frac{d\phi\left(x\right)}{dx}=-\frac{qN_D}{\epsilon_{Si}}\left[x-\frac{t_{Si}}{2}+x_d\right],\ \text{for}\ \ |x|<\left(\frac{t_{Si}}{2}-x_d\right). \tag{2.29}$$

Then integrating (2.28) once from $x = 0$ to $x = x$ as

$$\int_{\phi(0)}^{\phi(x)} \frac{d\phi\,(x)}{dx} dx = \int_{x=0}^{x} 0\, dx$$

gives $\phi\,(x)$ in the neutral region, i.e.,

$$\phi\,(x) = \phi\,(0) \tag{2.30}$$

On the other hand, integrating (2.29) once from $x = \dfrac{t_{Si}}{2} - x_d$ to $x = x$

$$\int_{\phi(0)}^{\phi(x)} \frac{d\phi\,(x)}{dx} dx = -\frac{qN_D}{\epsilon_{Si}} \int_{x=t_{Si}/2-x_d}^{x} \left[x - \frac{t_{Si}}{2} + x_d \right] dx$$

provides the solution of Poisson's equation for $\phi\,(x)$ in the depleted region

$$\phi\,(x) = \phi\,(0) - \frac{qN_D}{2\epsilon_{Si}} \left[x - \left(\frac{t_{Si}}{2} - x_d \right) \right]^2 \tag{2.31}$$

valid in the region $|x| < \left(\dfrac{t_{Si}}{2} - x_d \right)$. In evaluating this integral the continuity of potential at $x = \dfrac{t_{Si}}{2} - x_d$ has been used.

The surface potential is then obtained from (2.31) by replacing $\phi\,(0)$ with V and setting $x = \dfrac{t_{Si}}{2}$,

$$\phi_s = V - \frac{qN_D}{2\epsilon_{Si}} x_d^2 \tag{2.32}$$

The space charge density in this condition can be determined as

$$Q_{SC} = 2qN_D x_d = -2C_{ox}\,(V_G - V_{FB} - \phi_s) \tag{2.33}$$

Substituting the value of x_d from (2.33) into (2.32) then leads to the following relationship between ϕ_s and V_G in the partly depleted mode i.e.,

$$\phi_s = V - \frac{1}{\beta}(V_G - V_{FB} - \phi_s)^2 \tag{2.34}$$

where β is the same as defined in (2.26).

2.4.4 Deep depletion approximation under subthreshold condition

Although (2.34) is based on the depletion approximation and represents surface potential in the partly depleted mode, it is not quite suitable for subthreshold conditions. The usual solution to derive the drain current is to carry out charge carrier statistics; however, here in this work a deep depletion approximation based on surface potential is used.

Squaring both sides of (2.24) and (2.20) and combining the resulting equations, it can be obtained that

$$(V_G - V_{FB} - \phi_s)^2 = \frac{2qN_D\epsilon_{Si}v_T}{C_{ox}}\left\{\exp\left(\frac{\phi_s - V}{v_T}\right) - \exp\left[\frac{\phi(0) - V}{v_T}\right] - \left[\frac{\phi_s - \phi(0)}{v_T}\right]\right\} \tag{2.35}$$

Let

$$\alpha = \frac{\phi(0) - \phi_s}{v_T} \tag{2.36}$$

be the normalized difference of potentials. Substituting (2.36) into (2.35), manipulating the resulting equation and finally taking the square root leads to

$$V_G - V_{FB} - \phi_s = -\sqrt{\frac{2qN_D\epsilon_{Si}v_T\alpha}{C_{ox}}}\sqrt{1 - \frac{1 - \exp(-\alpha)}{\alpha}\exp\left(\frac{\phi(0) - V}{v_T}\right)} \tag{2.37}$$

(2.37) is a transcendental equation. ϕ_s for deep depletion operation can be calculated by solving this equation. But for the below-threshold regime, an even simpler

expression can be obtained if the deep depletion nature of surface potential is exploited.

It can be noted that subthreshold operation leads to

$$\frac{1-\exp\left(-\alpha\right)}{\alpha} \ll 1$$

Therefore the term on the right hand side of (2.37) can be simplified through expanding the square root using binomial expansion theorem

$$\begin{aligned}\sqrt{1-\frac{1-\exp\left(-\alpha\right)}{\alpha}\exp\left(\frac{\phi\left(0\right)-V}{v_T}\right)} &\approx 1-\frac{1}{2}\left[\frac{1-\exp\left(-\alpha\right)}{\alpha}\exp\left(\frac{\phi\left(0\right)-V}{v_T}\right)\right] \\ &\approx 1-\frac{1}{2}\left[\frac{1-\left(1-\alpha\right)}{\alpha}\exp\left(\frac{\phi\left(0\right)-V}{v_T}\right)\right] \\ &= 1-\frac{1}{2}\left[\exp\left(\frac{\phi\left(0\right)-V}{v_T}\right)\right]\end{aligned} \tag{2.38}$$

In the deep depletion limit, the difference between the potential at the center of the silicon body and the surface potential can be computed by setting $x = x_d = \frac{t_{Si}}{2}$ in (2.31)

$$\phi\left(0\right) - \phi_s = \frac{qN_d t_{Si}^2}{8\epsilon_{Si}} \tag{2.39}$$

Using (2.39) and (2.36) with (2.37) and (2.38) and making some rearrangements it can be written as

$$V_G - V_{FB} - \phi_s = -\frac{qN_D t_{Si}}{2C_{ox}}\left[1-\frac{1}{2}\exp\left(\frac{\phi_s + \frac{qN_d t_{Si}^2}{8\epsilon_{Si}} - V}{v_T}\right)\right] \tag{2.40}$$

In quest for an explicit expression for surface potential (2.40) is further modified invoking (2.48) to (2.50)

$$V_G - V_{TH} - \frac{qN_D t_{Si}}{8C_{Si}} - \phi_s = \frac{qN_D t_{Si}}{4C_{ox}} \exp\left(\frac{\phi_s + \frac{qN_d t_{Si}^2}{8\epsilon_{Si}} - V}{v_T}\right)$$

Multiplying both sides by $-\frac{1}{v_T}$ and then rearranging the exponential term the above expression can be written as

$$\frac{\phi_s - V_G + V_{TH} + \frac{qN_D t_{Si}}{8C_{Si}}}{v_T}$$
$$= -\frac{qN_D t_{Si}}{4C_{ox}v_T} \exp\left(\frac{\phi_s - V_G + V_{TH} + \frac{qN_d t_{Si}^2}{8\epsilon_{Si}}}{v_T}\right) \exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)$$

Now dividing both sides by the exponential term and multiplying by -1 finally one can write

$$-\frac{\phi_s - V_G + V_{TH} + \frac{qN_D t_{Si}}{8C_{Si}}}{v_T} \exp\left(-\frac{\phi_s - V_G + V_{TH} + \frac{qN_d t_{Si}^2}{8\epsilon_{Si}}}{v_T}\right) = \frac{qN_D t_{Si}}{4C_{ox}v_T} \exp\left(\frac{V_G - V_{TH} - V}{v_T}\right) \tag{2.41}$$

(2.41) is of the form

$$Y = X \exp(X) \tag{2.42}$$

where

$$X = -\frac{\phi_s - V_G + V_{TH} + \dfrac{qN_D t_{Si}}{8C_{Si}}}{v_T} \tag{2.43}$$

Solution of (2.42) is found by using Lambert-W function [37], W which is the inverse of the function in (2.42). Using (2.43), the solution can be written as

$$X = -\frac{\phi_s - V_G + V_{TH} + \dfrac{qN_D t_{Si}}{8C_{Si}}}{v_T} = W\left[\frac{qN_D t_{Si}}{4C_{ox} v_T} \exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right] \tag{2.44}$$

The Lambert-W function has already proved its usefulness in numerous physics applications and has also been recently utilized for finding the solutions to bipolar transistor circuit analysis problems [38].

Finally rearranging (2.44) the explicit expression of surface potential can be written as

$$\phi_s = V_G - V_{TH} - \frac{qN_D t_{Si}}{8C_{Si}} - v_T\, W\left[\frac{qN_D t_{Si}}{4C_{ox} v_T} \exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right] \tag{2.45}$$

2.5 Expression for Threshold Voltage

Voltage drop across the oxide layer can be found from (2.3)

$$\phi_{ox} = -\frac{Q_{SC}}{2C_{ox}} = -\frac{qN_D}{\epsilon_{ox}} x_d t_{ox} \tag{2.46}$$

In (2.1) gate voltage is shown as the sum of the flatband voltage, the voltage drop across the semiconductor and the oxide layer. Therefore expressions for oxide drop and surface potential can be put into (2.1) from (2.46) and (2.34) respectively as

$$V_G = V_{FB} - \frac{qN_D}{2\epsilon_{ox}} x_d t_{ox} + V - \frac{qN_D}{2\epsilon_{Si}} x_d^2 \tag{2.47}$$

Maximum depletion charge is obtained when top gate depletion layer touches the bottom gate depletion layer i.e., the depletion width reaches its maximum value or, $x_d = \frac{t_{Si}}{2}$. In literature this condition is taken as the definition of *threshold voltage*, V_{TH}. Therefore the expression for threshold voltage can be found by setting this maximum value of x_d with $V = 0$ in (2.47); which yields the following:

$$V_{TH} = V_{FB} - \frac{qN_D t_{Si}}{2C_{eff}} \tag{2.48}$$

where

$$\frac{1}{C_{eff}} = \frac{1}{4C_{Si}} + \frac{1}{C_{ox}} \tag{2.49}$$

and

$$C_{Si} = \frac{\epsilon_{Si}}{t_{Si}} \tag{2.50}$$

2.6 Current - Voltage Relationship

In this section, current-voltage characteristics of JL DG MOSFET is discussed i.e., mathematical model for current along the channel is investigated. Based on the surface potential model developed in section 2.4 an analytical expression for drain current will be derived.

2.6.1 Expression for Drain Current

At first the *mobile charge density*, Q_m is expressed as

$$Q_m = Q_{SC} - Q_d \tag{2.51}$$

where

$$Q_d = qN_D t_{Si} \tag{2.52}$$

is the *fixed charge density*.

According to the current continuity condition, the *drain to source current*, I_{DS} is given by

$$I_{DS} = -\mu W Q_m \frac{dV}{dy} \tag{2.53}$$

where, μ is the carrier mobility (assumed to be a constant along the channel). Making use of gradual-channel approximation,

(2.53) can be rearranged in the form

$$I_{DS}\, dy = -\mu W Q_m\, dV$$

and then integrating both sides of this equation from $x = 0$ at the source to $x = L$ at the drain and, correspondingly from $V(0) = 0$ to $V(L) = V_{DS}$,

$$\int_0^L I_{DS}\, dy = -\mu W \int_0^{V_{DS}} Q_m\, dV$$

Pao-Sah integral can now be expressed as

$$I_{DS} = -\mu \frac{W}{L} \int_0^{V_{DS}} Q_m\, dV \tag{2.54}$$

With the help of (2.33), the above expression can be written as

$$I_{DS} = -\mu \frac{W}{L} \int_0^{V_{DS}} \left[2C_{ox}\left(V_G - V_{FB} - \phi_s\right) + Q_d\right] dV \tag{2.55}$$

with the assumption of $V_S = 0$ and $V_D = V_{DS}$. Substituting expressions for surface potential for different regions of operation, the drain current can be found valid in all these regions.

A slightly modified form of (2.55) will be helpful for the following derivations

$$I_{DS} = -\mu \frac{W}{L} \int_0^{V_{DS}} \left[2C_{ox} \left(V_G - V_{FB} - \phi_s \right) \frac{dV}{d\phi_s} d\phi_s + Q_d \, dV \right] \tag{2.56}$$

2.6.2 Current in accumulation region

When a large positive gate bias is applied i.e., if $V_G > V_{FB} + V_{DS}$, the whole channel of the JL DG MOSFET operates in accumulation mode. In this case differentiating both sides of (2.25) with respect to ϕ_s leads to

$$-2 \left(V_G - V_{FB} - \phi_s \right) = \beta v_T \exp \left(\frac{\phi_s - V}{v_T} \right) \left[\frac{1}{v_T} - \frac{1}{v_T} \frac{dV}{d\phi_s} \right]$$

which can be rearranged in the form

$$\frac{dV}{d\phi_s} = 1 + \frac{2 \left(V_G - V_{FB} - \phi_s \right)}{\beta \exp \left(\dfrac{\phi_s - V}{v_T} \right)} \tag{2.57}$$

From (2.25) one can write

$$\beta \exp \left(\frac{\phi_s - V}{v_T} \right) = \frac{\left(V_G - V_{FB} - \phi_s \right)^2}{v_T} + \beta$$

Using this expression into (2.57) one finally gets

$$\frac{dV}{d\phi_s} = 1 + 2 v_T \frac{V_G - V_{FB} - \phi_s}{\left(V_G - V_{FB} - \phi_s \right)^2 + \beta \, v_T} \tag{2.58}$$

Substituting (2.58) into (2.56) the expression for drain current becomes

$$I_{DS} = 2\mu C_{ox}\frac{W}{L}\int_0^{V_{DS}} (V_G - V_{FB} - \phi_s)\left[1 + 2v_T\frac{V_G - V_{FB} - \phi_s}{(V_G - V_{FB} - \phi_s)^2 + \beta\, v_T}\right] d\phi_s + \mu\frac{W}{L}\int_0^{V_{DS}} Q_d\, dV \tag{2.59}$$

and evaluating the resulting integral, the following expression for the drain current can be obtained

$$I_{DS} = \mu\frac{W}{L}\left[Q_d V - 4C_{ox}v_T\,(V_G - V_{FB} - \phi_s) - C_{ox}\,(V_G - V_{FB} - \phi_s)^2\right]_{\phi_s(0)}^{\phi_s(L)} + \left[4C_{ox}v_T\sqrt{\beta\, v_T}\tan^{-1}\left(\frac{V_G - V_{FB} - \phi_s}{\sqrt{\beta\, v_T}}\right)\right]_{\phi_s(0)}^{\phi_s(L)} \tag{2.60}$$

where $\phi_s\,(0)$ and $\phi_s\,(L)$ denote the surface potential values at source and drain ends respectively. Hence the current in accumulation can be calculated from the surface potential evaluated from (2.25) at the source and the drain.

2.6.3 Expression for current in partly depleted region

If $V_{TH} < V_G < V_{FB}$, i.e., when gate bias is small, the whole channel of the JL MOSFET is in the partly depleted mode. Differentiating both sides of (2.34) and rearranging, it can be obtained that

$$\frac{dV}{d\phi_s} = 1 - \frac{2}{\beta}(V_G - V_{FB} - \phi_s) \tag{2.61}$$

(2.61) is then substituted into (2.56) to obtain

$$I_{DS} = -\mu\frac{W}{L}\int_0^{V_{DS}} \left[2C_{ox}\,(V_G - V_{FB} - \phi_s)\left\{1 - \frac{2}{\beta}(V_G - V_{FB} - \phi_s)\right\} d\phi_s + Q_d\, dV\right]$$

Solving this integral one can obtain the drain current in partial depletion region of operation

$$I_{DS} = \mu \frac{W}{L} \left[Q_d V - C_{ox} \left(V_G - V_{FB} - \phi_s \right)^2 + \frac{4}{3\beta} C_{ox} \left(V_G - V_{FB} - \phi_s \right)^3 \right]_{\phi_s(0)}^{\phi_s(L)} \tag{2.62}$$

2.6.4 Current in hybrid channel

If applied gate bias is within the range $V_{FB} < V_G < V_{FB} + V_{DS}$ with $V_{DS} > 0$, then the channel is biased in the accumulation mode from the source to some flatband position and biased in partly depleted mode from the flatband coordinate to the drain. Under the circumstances, the integral in (2.56) must be divided into two parts, and the total current has to be written as the sum of two components, each being calculated by (2.25) and (2.34). Then the drain current for this hybrid channel can be obtained as

$$\begin{aligned} I_{DS} = \mu \frac{W}{L} \Bigg[& Q_d V_{DS} + 2C_{ox} \int_0^{V_G - V_{FB}} \left(V_G - V_{FB} - \phi_s \right) dV \Big|_{acc} \\ & + 2C_{ox} \int_{V_G - V_{FB}}^{V_{DS}} \left(V_G - V_{FB} - \phi_s \right) dV \Big|_{dep} \Bigg] \end{aligned} \tag{2.63}$$

2.6.5 Current expression in fully depleted region

If $V_G < V_{TH}$, the whole channel of the JL DG MOSFET is in the fully depletion mode, entering into the subthreshold region. Substituting ϕ_s from (2.38) the integral of (2.55) can be written as

$$\begin{aligned} & 2C_{ox} \left(V_G - V_{FB} - \phi_s \right) + Q_d \\ & = 2C_{ox} \left(V_{TH} - V_{FB} + \frac{qN_D t_{Si}}{8C_{Si}} + v_T W \left[\frac{qN_D t_{Si}}{4C_{ox} v_T} \exp \left(\frac{V_G - V_{TH} - V}{v_T} \right) \right] \right) + Q_d \end{aligned}$$

which can be simplified using (2.48)

$$\begin{aligned} &2C_{ox}\left(V_G - V_{FB} - \phi_s\right) + Q_d \\ &= 2C_{ox}\left(-\frac{qN_D t_{Si}}{2C_{eff}} + \frac{qN_D t_{Si}}{8C_{Si}} + v_T\, W\left[\frac{qN_D t_{Si}}{4C_{ox}v_T}\exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right]\right) + Q_d \end{aligned} \tag{2.64}$$

Substituting C_{eff} from (2.49) into (2.64) one obtains

$$\begin{aligned} &2C_{ox}\left(V_G - V_{FB} - \phi_s\right) + Q_d \\ &= 2C_{ox}\left(-\frac{qN_D t_{Si}}{2C_{ox}} + v_T\, W\left[\frac{qN_D t_{Si}}{4C_{ox}v_T}\exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right]\right) + Q_d \end{aligned} \tag{2.65}$$

Finally setting Q_d from (2.52) into (2.65) the integral simplifies to

$$2C_{ox}\left(V_G - V_{FB} - \phi_s\right) + Q_d = 2C_{ox}v_T\, W\left[\frac{Q_d}{4C_{ox}v_T}\exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right] \tag{2.66}$$

Therefore one can obtain the current in fully depleted region from (2.54) and (2.66) as follows:

$$I_{DS} = 2\mu\frac{W}{L}v_T\, C_{ox}\int_0^{V_{DS}} W\left[\frac{Q_d}{4C_{ox}v_T}\exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right] dV \tag{2.67}$$

Thus using abrupt depletion assumption, it is possible to have different explicit expressions of surface potential and drain current valid for all regions of device operation. MATLAB programs have been used to solve these equations. Graphical results obtained from those programs have been shown in chapter 4, .

3. First Order Depletion Model of JL DG MOSFET

In the previous chapter a simple analytical model has been developed for JL DG MOSFET. The model is based on the simple assumption of abrupt depletion inside the channel of the device. This chapter is devoted to the development of an improved analytical model. This new proposed model uses the concept of *gradual depletion* inside the channel. Abrupt depletion model assumes that an abrupt boundary exists between the depleted and neutral regions inside the channel. But this assumption cannot catch the the real scenario. In reality the boundary between depleted and neutral regions is not abrupt. Gradual depletion assumption is an attempt to incorporate this fact in device modeling. Abrupt depletion model helps to obtain simple modeling equations and quick understanding of the device behavior but accuracy of this model may not be satisfactory in real applications. In the next chapter, it has been shown that this new model provides a better approximation of Junctionless Double Gate MOSFET behavior.

3.1 Normalization

For the sake of clarity, all formula of the previous chapter have been presented without the use of simplifications or normalization. It is easier to deal with normalized equations rather than the actual ones because normalization helps to get rid of constant multiplying factors. Using normalized equations in modeling simulations is a common practice in literature. Performing the actual calculation using normalized units makes the algorithms more efficient, and in many cases helps to avoid numerical overflow and underflow. So, before proceeding further in developing the

new model, the working equation (2.13) developed in chapter 2 based on Poisson's equation will be normalized.

3.1.1 Normalization of Poisson's equation

The normalization procedure starts with the rearranging of (2.13) as

$$v_T \frac{d^2}{dx^2}\left(\frac{\phi}{v_T}\right) = \frac{qN_D}{\epsilon_{si}}\left[\exp\left(\frac{\phi}{v_T} - \frac{V}{v_T}\right) - 1\right]$$

and substituting $u = \phi/v_T$ and $v = V/v_T$ into the above expression which gives

$$\frac{d^2u}{dx^2} = \frac{qN_D}{\epsilon_{si}v_T}\left[\exp\left(u - v\right) - 1\right] \tag{3.1}$$

In effect in (3.1) electrostatic potential, ϕ and quasi Fermi potential, V have been *normalized* with respect to thermal voltage, v_T. So, u and v are referred to as *normalized electrostatic potential* and *normalized quasi Fermi potential* respectively.

Now, letting

$$\frac{1}{\lambda_D} = \sqrt{\frac{qN_D}{\epsilon_{si}v_T}} \tag{3.2}$$

and

$$p = \frac{x}{\lambda_D} \tag{3.3}$$

one can get

$$\frac{dp}{dx} = \frac{1}{\lambda_D}$$

and

$$\frac{d^2}{dx^2} \equiv \frac{dp}{dx}\frac{d}{dp}\left(\frac{dp}{dx}\frac{d}{dp}\right) \equiv \frac{1}{\lambda_D^2}\frac{d^2}{dp^2}$$

where λ_D is known as *Debye length*. Here x has been normalized with respect to λ_D. So p is referred to as *normalized position variable*.

Then (3.1) can be rewritten as

$$\frac{d^2u}{dp^2} = \exp(u - v) - 1 \tag{3.4}$$

It can be observed that there is no constant multiplying factor on any side of (3.4) and hence is the desired normalized working equation for the present analysis.

3.1.2 Normalized boundary conditions

In chapter 2 it has been shown that the boundary conditions can be expressed as

$$\left.\frac{d\phi}{dx}\right|_{x=0} = 0 \qquad \text{and} \qquad \phi\left(\pm\frac{t_{si}}{2}\right) = \phi_s$$

These above equations can easily be normalized to obtain *normalized boundary equations*

$$\left.\frac{du}{dp}\right|_{p=0} = 0 \tag{3.5}$$

$$u(\pm P) = u_s \tag{3.6}$$

where

$$P = \frac{t_{si}}{2\lambda_D}. \tag{3.7}$$

3.1.3 Electric field equation from the working equation

An expression for *normalized electric field*, $E_n(p)$ can be obtained by integrating (3.4) once. The integration is performed by multiplying both sides of (3.4) by $2\frac{du}{dp}$,

i.e.,

$$2\frac{du}{dp}\frac{d^2u}{dp^2} = 2\exp(u-v)\frac{du}{dp} - 2\frac{du}{dp}$$

Now integrating both sides with respect to p as

$$\int_0^{E_n(p)} 2\frac{du}{dp}\frac{d^2u}{dp^2}dp = 2\int_0^{u(p)}\left[\exp(u-v)\frac{du}{dp} - \frac{du}{dp}\right]dp$$

an expression for $E_n(p)$ can be obtained i.e.,

$$E_n(p) = \frac{du}{dp} = \sqrt{2\left\{\exp\left[u(p)-v\right] - \exp\left[u(0)-v\right] - u(p) + u(0)\right\}} \tag{3.8}$$

Normalized surface electric field, E_{ns} can be found by setting $p = P$ into (3.8),

$$\begin{aligned} E_{ns} = E_n(P) &= \left.\frac{du}{dp}\right|_{p=P} \\ &= \sqrt{2\left\{\exp\left[u_s - v\right] - \exp\left[u(0)-v\right] - u_s + u(0)\right\}} \end{aligned} \tag{3.9}$$

Once again, another integration of (3.8) does not yield any closed-form expression. Therefore in the following, efforts will be put to obtain approximate analytical solutions.

3.1.4 Determination of surface charge

Electric field expression in (2.17) can be modified to express in terms of normalized variables i.e., in terms of p and u as

$$E = -\frac{d\phi}{dp}\frac{dp}{dx} = -\frac{1}{\lambda_D}\frac{d}{dp}\left(v_T\frac{\phi}{v_T}\right) = -\frac{v_T}{\lambda_D}\frac{du}{dp} \tag{3.10}$$

and therefore surface charge Q_{SC} in (2.18) is transformed into

$$Q_{SC} = -2\left(\frac{\epsilon_{Si} v_T}{\lambda_D}\right) \left.\frac{du}{dp}\right|_{p=P} = -2\left(\frac{\epsilon_{Si} v_T}{\lambda_D}\right) E_{ns} \tag{3.11}$$

3.1.5 Approximate solution in accumulation region of operation

The first-order model deals only with the solution in depletion region of operation. Therefore it incorporates the solution obtained in chapter 2 for accumulation region of operation without further modification. Here the expressions for electric field and surface potential under accumulation is just restated in terms of normalized variables

$$E_s \approx \frac{V_T}{\lambda_D}\sqrt{2\left[\exp\left(u_s - v\right) - 1\right]} \tag{3.12}$$

and

$$\beta v_T \left[\exp\left(u_s - v\right) - 1\right] = \left(V_G - V_{FB} - u_s\, v_T\right)^2 \tag{3.13}$$

where β is the same as defined in (2.26)

3.1.6 Approximate solution under depletion condition

When $u_s < v$ i.e., the device is biased in depletion or subthreshold conditions, usually an *zero-order depletion approximation* is used in device modeling. In zero-order approximation it is assumed that an *abrupt transition* occurs between neutral and depleted regions as shown in Fig. 3.1. That is in zero-order depletion approximation

$$\rho\left(x\right) = \begin{cases} N_D, & x < x_d \\ 0, & x > x_d \end{cases} \tag{3.14}$$

where x_d is the length of the depletion region.

Here in this work a different modeling approach will be used under depletion condition. The exponential term present on the right hand side of (3.4) is *linearized* by

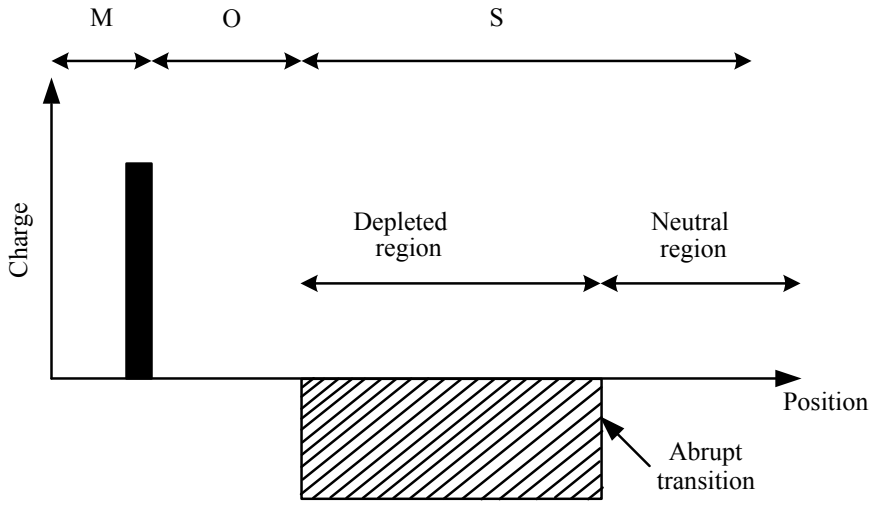


Figure 3.1: Illustration of zero-order depletion approximation.

setting

$$u = u_c + \delta u \tag{3.15}$$

where u_c is regarded as the electrostatic potential at the symmetry axis of the device. δu can be viewed as the deviation of electrostatic potential from that of the symmetry axis. Assumption of this type is regarded as a *first-order approximation* to the exact carrier concentration and has already been applied for JL nanowire FETs [39]. With this approximation (3.4) is modified as

$$\frac{d^2\delta u}{dp^2} - \exp\left(u_c - v\right)\delta u = \exp\left(u_c - v\right) - 1 \tag{3.16}$$

which is valid for $0 \leq p \leq p_0$. The point p_0 is defined as the point where

$$\delta u\left(p_0\right) = -1 \tag{3.17}$$

Let α be defined as

$$\alpha \triangleq \exp\left(u_c - v\right) \tag{3.18}$$

Then using the definition in (3.18), (3.16) can be modified as

$$\frac{d^2\delta u}{dp^2} - \alpha\delta u = \alpha - 1 \tag{3.19}$$

The first initial condition required to solve (3.19) can be obtained by noting that u must equal to u_c at the center of the channel i.e.,

$$u\,(0) = u_c \tag{3.20}$$

The second initial condition can be obtained by exploiting the symmetry of the DG device as stated in (3.5). These two conditions can be rewritten in terms of δu using (3.15) as

$$\delta u\,(0) \;\; = 0 \tag{3.21}$$

$$\frac{d\delta u}{dp}\,(0) \;\; = 0 \tag{3.22}$$

The trial solution for (3.19) is

$$\delta u\,(p) = C_1\, e^{\sqrt{\alpha}p} + C_2\, e^{-\sqrt{\alpha}p} + C_3 \tag{3.23}$$

where C_1, C_2 and C_3 are constants to be determined from the boundary conditions.

Applying the first boundary condition (3.21) into (3.23) leads to

$$C_1 + C_2 + C_3 = 0 \tag{3.24}$$

Similarly the use of the second boundary condition implies

$$C_1 = C_2 \tag{3.25}$$

Using (3.25) into (3.24) gives

$$2C_1 + C_3 = 0 \tag{3.26}$$

Use of (3.25) into (3.23) leads to

$$\delta u\,(p) = C_1\, \left(e^{\sqrt{\alpha}p} + \, e^{-\sqrt{\alpha}p}\right) + C_3 \tag{3.27}$$

The above two equations are not sufficient to determine all three constants. Three equations are required to solve for three unknown constants. The last equation required to completely determine the constants can be obtained by substituting $\delta u\,(p)$ from (3.27) back into (3.19) which leads to the following result

$$-\alpha C_3 = \alpha - 1 \tag{3.28}$$

Finally from (3.26), (3.27) and (3.28), the constants C_1, C_2 and C_3 can be obtained as

$$\begin{aligned} C_1 \quad &= C_2 = \frac{\alpha - 1}{2\alpha} \\ C_3 \quad &= -\frac{\alpha - 1}{\alpha} \end{aligned}$$

Substituting these values into (3.23), the final solution can be found as

$$\delta u = \frac{\alpha - 1}{2\alpha}\left[\, e^{\sqrt{\alpha}p} + \, e^{-\sqrt{\alpha}p}\right] - \frac{\alpha - 1}{\alpha} \tag{3.29}$$

or after some manipulation the above equation can be rewritten as

$$\delta u\,(p) = \frac{\alpha - 1}{\alpha}\left[\cosh\left(\sqrt{\alpha}\,p\right) - 1\right]; \qquad 0 \le p \le p_0 \tag{3.30}$$

From (3.17) and (3.30), the value of p_0 can be determined, i.e.,

$$p_0 = \frac{1}{\sqrt{\alpha}}\cosh^{-1}\left(\frac{1}{1-\alpha}\right) \tag{3.31}$$

For the region $p_0 < p < P$, the depletion approximation is used i.e., instead of (3.19), the following expression is used to determine the electrostatic potential

$$\frac{d^2\delta u}{dp^2} = -1 \tag{3.32}$$

The trial solution for (3.32) is

$$\delta u = C_4\, p^2 + C_5\,(p - p_0) + C_6 \tag{3.33}$$

where C_4, C_5 and C_6 are constants and subjected to two continuity conditions.

The first condition has already been stated in (3.17) which simply implies that the solution valid for region $0 < p < p_0$ and that valid for $p > p_0$ must provide the same value at p_0 i.e., the transition must be continuous.

The second continuity condition is given as follows

$$\left.\frac{d\delta u}{dp}(p_0)\right|_{0<p<p_0} = \left.\frac{d\delta u}{dp}(p_0)\right|_{p>p_0} \tag{3.34}$$

This condition implies that the derivatives of both solutions must also be continuous at p_0.

Using (3.17) with (3.33) leads to the following

$$C_4\, p_0^2 + C_6 = -1 \tag{3.35}$$

The second continuity equation (3.34) implies

$$\frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right) = 2C_4\, p_0 + C_5 \tag{3.36}$$

Putting $\delta u\,(p)$ from (3.33) into (3.32) gives

$$2C_4 = -1 \tag{3.37}$$

Solving the set of equations comprised of (3.35), (3.36) and (3.37) finally determines the constants

$$\begin{aligned} C_4 &= -\frac{1}{2} \\ C_5 &= p_0 + \frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha}\, p_0\right) \\ C_6 &= \frac{1}{2} p_0^2 - 1 \end{aligned}$$

Then the final solution of (3.32) can be obtained by substituting these values into (3.33) i.e.,

$$\delta u\left(p\right) = -\frac{p^2 - p_0^2}{2} - 1 + \left[p_0 + \frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha}\, p_0\right)\right]\left(p - p_0\right) \tag{3.38}$$

which is valid for the region $p_0 < p < P$.

3.1.7 Approximate analytical expression for surface potential

Since surface potential, $u_s = u\left(P\right)$, expressions for u_s under depletion mode of operation can be obtained by replacing p with P into (3.30) and (3.38).

$$u_s = u\left(P\right) = u_c + \delta u\left(P\right) \tag{3.39}$$

The surface potential is then given by,

$$u_s = u_c + \frac{\alpha - 1}{\alpha}\left[\cosh\left(\sqrt{\alpha} P\right) - 1\right] \tag{3.40}$$

for $p_0 > P$, and

$$u_s = u_c - \frac{P^2 - p_0^2}{2} - 1 + \left[p_0 + \frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right)\right]\left(P - p_0\right) \tag{3.41}$$

for $p_0 < P$.

3.2 Analytical Expression for Surface Charge Under Depletion Condition

Making use of (3.30) and (3.38) with (3.15), $\dfrac{du}{dp}$ can be found as

$$\frac{du}{dp} = \frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p\right); \qquad 0 < p < p_0 \tag{3.42}$$

or,

$$\frac{du}{dp} = -p + p_0 - \frac{1 - \alpha}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right); \qquad p_0 < p < P \tag{3.43}$$

Then Q_{SC} can be determined as

$$Q_{SC} = -\frac{\epsilon_{si} v_T}{\lambda_D} \left[\frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} P\right) \right] \tag{3.44}$$

for $p_0 > P$, or

$$Q_{SC} = \frac{\epsilon_{si} v_T}{\lambda_D} \left[P - p_0 + \frac{1 - \alpha}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right) \right] \tag{3.45}$$

for $p_0 < P$.

3.2.1 Determining surface potential and charge

In accumulation u_s is determined with (3.13). Then having the knowledge of u_s, Q_{SC} can be computed from (2.23).

In depletion the computation of u_s and u_c is carried out with (2.23) using, as an intermediate step, the computation of α with the help of (3.40) or (3.41). The knowledge of α provides $u_c - v$ and, thus, u_c for any given v, as well as u_s. Q_{SC} can be found with the help of (3.44) and (3.45) depending on the value of p_0.

It is to be remembered that u_s is not the true surface potential rather it is the normalized surface potential. The *true* surface potential can be obtained by multiplying

u_s by v_T that is,

$$\phi_s = u_s \, v_T \tag{3.46}$$

3.3 Threshold Voltage

Threshold voltage calculation in first-order model is quite straight forward. When complete depletion occurs the normalized Poisson's equation simply reads

$$\frac{d^2u}{dp^2} = -1 \tag{3.47}$$

Integrating both sides with respect to p under the boundary conditions of section 3.1.2 as

$$\int_{p=0}^{p} \frac{d^2u}{dp^2} dp = -\int_{p=0}^{p} dp$$

one gets

$$\frac{du}{dp} = -p \tag{3.48}$$

Then integrating the above expression again as

$$\int_{p=0}^{p} \frac{du}{dp} dp = -\int_{p=0}^{p} p \, dp$$

one gets

$$u\,(p) - u_c = -\frac{p^2}{2} \tag{3.49}$$

Setting $p = P$ in the expression just obtained, the following expression for u_s can be reached

$$u_s - u_c = -\frac{P^2}{2} = -\frac{t_{Si}^2}{8\lambda_D^2} = -\frac{qN_D t_{Si}^2}{8\epsilon_{Si} v_T} \tag{3.50}$$

Using the above expression with (2.1), (2.3) and (2.46), the following expression for threshold voltage, V_{TH} is obtained

$$V_{TH} = V_{FB} - \frac{qN_D t_{Si}}{2C_{eff}} \tag{3.51}$$

where C_{eff} is defined in (2.49).

It is to be noted that the threshold voltage expression obtained using the first-order model i.e., (3.51) and that obtained form abrupt depletion model namely (2.48) are identical. This is because under the assumption of complete depletion both models actually use the same picture of JL DG MOSFET. It is also important to remember that the limiting condition in (3.50) is in fact an asymptotic expression which occurs only for $V_{GS} \ll V_{TH}$.

3.4 Expression for current in First-order Model

In section 2.6.1, the concept of mobile charge density was introduced and (2.51) and (2.52) were used to calculate mobile charge density from the knowledge of space charge density. The same concept is also used with first-order model.

In accumulation region, the current expression is the same as used in chapter 2 namely (2.60) which has been restated here

$$\begin{aligned} I_{DS} = \mu \frac{W}{L} \left[Q_d V - 4C_{ox} v_T \left(V_G - V_{FB} - u_s v_T \right) - C_{ox} \left(V_G - V_{FB} - u_s v_T \right)^2 \right]_{u_s(0)}^{u_s(L)} \\ + \left[4C_{ox} v_T \sqrt{\beta\, v_T} \tan^{-1} \left(\frac{V_G - V_{FB} - u_s v_T}{\sqrt{\beta\, v_T}} \right) \right]_{u_s(0)}^{u_s(L)} \end{aligned} \tag{3.52}$$

where $u_s(0)$ and $u_s(L)$ denote the surface potential values at source and drain ends respectively.

In depletion mode of operation, mobile charge density is calculated by using (3.44) for Q_{SC} and then substituting it into (2.51) i.e.,

$$Q_m = -\frac{\epsilon_{si} v_T}{\lambda_D} \left[\frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} P\right) \right] - q N_D t_{Si} \tag{3.53}$$

for $p_0 > P$.

On the other hand when $p_0 < P$, (3.45) is used as an expression for Q_{SC}

$$Q_m = \frac{\epsilon_{si} v_T}{\lambda_D} \left[P - p_0 + \frac{1 - \alpha}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right) \right] - q N_D t_{Si}. \tag{3.54}$$

Using these above expressions with Pao-Sah integral in (2.54), the following expressions can be achieved

$$I_{DS} = -\mu \frac{W}{L} \int_{V_S}^{V_D} \left\{ -\frac{\epsilon_{si} v_T}{\lambda_D} \left[\frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} P\right) \right] - q N_D t_{Si} \right\} dV \tag{3.55}$$

if $p_0 > P$, or

$$I_{DS} = -\mu \frac{W}{L} \int_{V_S}^{V_D} \left\{ \frac{\epsilon_{si} v_T}{\lambda_D} \left[P - p_0 + \frac{1 - \alpha}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right) \right] - q N_D t_{Si} \right\} dV \tag{3.56}$$

for $p_0 > P$.

Unfortunately the integrals in (3.55) and (3.56) do not have closed form solutions, i.e., they have to be computed numerically. The current values are to be evaluated according to the bias condition as discussed in the following. Before that let a new parameter to be defined as

$$V_G^{eff} = V_G - V_{FB} \tag{3.57}$$

If $V_S < V_D < V_G^{eff}$, the surface is biased in accumulation from the source to the drain. In this case, the current expression is given by as per (3.52).

When $V_G^{eff} < V_S < V_D$, the surface is biased in depletion from the source to the drain. In this case the current, I_{DS} is calculated from (3.55) or (3.56) according to the value of p_0.

Finally, if $V_S < V_G^{eff} < V_D$, the surface is biased in accumulation at the source side and in depletion at the drain side of the channel. In this case the Pao-Sah integral in (2.54) is split into two, the first of which is extended from V_S to V_G^{eff} with the current expression is given by (3.52) where the upper limit of the integration is changed to V_G^{eff}. The second one is extended from V_G^{eff} to V_D with the integrand function given again by (3.55) or (3.56) depending on the value of p_0. The lower limit of the integral in both cases are to be replaced by V_G^{eff}.

Although using gradual/linear depletion assumption provides different closed-form equations of surface potential valid for different regions of operation but it fails to produce closed-form expressions for drain current. But drain current values can be obtained easily by writing some MATLAB codes applying numerical techniques and following the above discussion. Graphical results generated using the first-order depletion model has been presented in the next chapter.

4. Results and Discussions

In the previous two chapters, two different approaches to model Junctionless DG MOSFET have been discussed. Based on the modeling equations developed in chapter 2 and 3, simulation results obtained from these models are presented in this chapter. As mentioned earlier that this work limits itself only to n-channel Junctionless DG MOSFET. The electrostatic potential, space and inversion charge carrier density and drain current characteristics of JL DG MOSFET are presented. The impact of various factors on the threshold voltage have also been analyzed in detail. The simulations for modeling have been performed by writing programs in MATLAB software to evaluate the modeling equations. The validity of the results is confirmed by comparing the obtained results with numerical solution of Poisson's equation using MATLAB, SILVACO ATLAS TCAD tool and already published data in literature.

4.1 Device Parameters

In figure 2.1, a two dimensional cross-section of a junctionless DG MOSFET with appropriate labeling of the device parameters has been shown. Silicon (Si) has been used as the channel material along with silicon-di-oxide (SiO_2) as the material for both top and bottom gate oxides. Table 4.1 lists all the values used for different device parameters in this simulation work.

Table 4.1: Device and process parameter values used in the simulation.

Name	Symbol	Value	Unit
Gate length	L	1	μm
Device width	W	1	μm
Doping concentration	N_D	10^{19}	cm^{-3}
Oxide thickness	t_{ox}	8	nm
Channel thickness	t_{Si}	10	nm
Workfunction difference	ϕ_{MS}	1.12	eV

4.2 Modeling Setup and Numerical Simulation

To understand the nature of different variables and their impacts on the characteristics of JL DG MOSFET and to get a comparison between the two models discussed in previous chapters, different variables are simulated using the aforementioned models. In order to check for the validity of simulated results numerical simulations were performed to directly compare the results and to find out the differences. Finally the simulated results were verified against TCAD tools to further guarantee the efficacy of the analytical models.

4.2.1 Abrupt Modeling

Abrupt modeling of JL DG MOSFET consists of the equations obtained for surface potential, surface charge, threshold voltage and drain to source current in chapter 2. For convenience those equations are restated here.

Surface potential in accumulation ($V_G > V_{FB} + V_D$):

$$\beta v_T \left[\exp\left(\frac{\phi_s - V}{v_T} \right) - 1 \right] = (V_G - V_{FB} - \phi_s)^2 \tag{4.1}$$

Surface potential under partial depletion ($V_{TH} < V_G < V_{FB} + V_D$):

$$\phi_s = V - \frac{1}{\beta}(V_G - V_{FB} - \phi_s)^2 \tag{4.2}$$

Surface potential under full depletion ($V_G < V_{TH}$):

$$\phi_s = V_G - V_{TH} - \frac{qN_D t_{Si}}{8C_{Si}} - v_T W \left[\frac{qN_D t_{Si}}{4C_{ox} v_T} \exp\left(\frac{V_G - V_{TH} - V}{v_T}\right)\right] \tag{4.3}$$

Threshold voltage:

$$V_{TH} = V_{FB} - \frac{qN_D t_{Si}}{2C_{eff}} \tag{4.4}$$

Current in accumulation ($V_G > V_{FB} + V_D$):

$$\begin{aligned} I_{DS} = \mu \frac{W}{L} &\left[Q_d V - 4C_{ox} v_T (V_G - V_{FB} - \phi_s) - C_{ox} (V_G - V_{FB} - \phi_s)^2\right]_{\phi_s(0)}^{\phi_s(L)} \\ &+ \left[4C_{ox} v_T \sqrt{\beta\, v_T} \tan^{-1}\left(\frac{V_G - V_{FB} - \phi_s}{\sqrt{\beta\, v_T}}\right)\right]_{\phi_s(0)}^{\phi_s(L)} \end{aligned} \tag{4.5}$$

Current in partial depletion ($V_{TH} < V_G < V_{FB}$):

$$I_{DS} = \mu \frac{W}{L} \left[Q_d V - C_{ox} (V_G - V_{FB} - \phi_s)^2 + \frac{4}{3\beta} C_{ox} (V_G - V_{FB} - \phi_s)^3\right]_{\phi_s(0)}^{\phi_s(L)} \tag{4.6}$$

Current in the hybrid channel ($V_{TH} < V_G < V_{FB} + V_D$):

$$\begin{aligned} I_{DS} = \mu \frac{W}{L} &\left[Q_d V_{DS} + 2C_{ox} \int_0^{V_G - V_{FB}} (V_G - V_{FB} - \phi_s)\, dV \Big|_{acc}\right. \\ &\left. + \; 2C_{ox} \int_{V_G - V_{FB}}^{V_{DS}} (V_G - V_{FB} - \phi_s)\, dV \Big|_{dep}\right] \end{aligned} \tag{4.7}$$

Current under full depletion ($V_G < V_{TH}$):

$$I_{DS} = 2\mu \frac{W}{L} v_T \, C_{ox} \int_0^{V_{DS}} W \left[\frac{Q_d}{4 C_{ox} v_T} \exp\left(\frac{V_G - V_{TH} - V}{v_T} \right) \right] dV \tag{4.8}$$

Several MATLAB scripts were written to simulate the above equations and plot the results. The prime advantage of abrupt model is that there are explicit expressions for currents so that results are obtained faster than any other models.

4.2.2 First-order Modeling

In the first order modeling, expressions for surface potential, surface charge, threshold voltage and drain current as derived in chapter 3 provide all information regarding the state of the device in all operating region. Those expressions are restated here for convenience.

Surface potential in accumulation ($V_G > V_{FB} + V_D$):

$$\beta v_T \left[\exp\left(u_s - v \right) - 1 \right] = \left(V_G - V_{FB} - u_s \, v_T \right)^2 \tag{4.9}$$

Surface potential under depletion ($V_G < V_{FB} + V_D$):

$$u_s = u_c + \frac{\alpha - 1}{\alpha} \left[\cosh\left(\sqrt{\alpha} P \right) - 1 \right] \tag{4.10}$$

for $p_0 > P$, and

$$u_s = u_c - \frac{P^2 - p_0^2}{2} - 1 + \left[p_0 + \frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0 \right) \right] \left(P - p_0 \right) \tag{4.11}$$

for $p_0 < P$.

$$p_0 = \frac{1}{\sqrt{\alpha}} \cosh^{-1}\left(\frac{1}{1 - \alpha} \right) \tag{4.12}$$

Surface charge under depletion ($V_G < V_{FB} + V_D$):

$$Q_{SC} = -\frac{\epsilon_{si} v_T}{\lambda_D} \left[\frac{\alpha - 1}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} P\right) \right] \tag{4.13}$$

for $p_0 > P$, or

$$Q_{SC} = \frac{\epsilon_{si} v_T}{\lambda_D} \left[P - p_0 + \frac{1 - \alpha}{\sqrt{\alpha}} \sinh\left(\sqrt{\alpha} p_0\right) \right] \tag{4.14}$$

for $p_0 < P$.

Normalized surface potential:

$$\phi_s = u_s \, v_T \tag{4.15}$$

Threshold voltage:

$$V_{TH} = V_{FB} - \frac{q N_D t_{Si}}{2 C_{eff}} \tag{4.16}$$

4.2.3 One-dimensional numerical simulation

In order to verify the accuracy of the analytical models and to prove the validity of abrupt and gradual depletion approximations, a one-dimensional numerical simulation of JL DG MOSFET has also been performed. The simulation zone is taken in the middle of the channel along the gate-to-gate line which is marked as the x-axis in figure 2.1. Equation (2.13) has been solved numerically along this line.

The differential equation was solved using *finite difference* technique. In this method the whole simulation zone is *discretized* into a finite number of grid points. The difference between the grid points and the total number of grid points is chosen in such a way to obtain sufficiently accurate results. At any grid point (except for the grids at the boundary), i the second order derivative is discretized according to the following equation

$$\frac{d^2\psi}{dx^2} = 2\,\frac{\left(\dfrac{\psi_{i+1}-\psi_i}{\Delta x_{i+1,i}} - \dfrac{\psi_i-\psi_{i-1}}{\Delta x_{i,i-1}}\right)}{\Delta x_{i+1,i}+\Delta x_{i,i-1}} \tag{4.17}$$

where $\Delta x_{i+1,i}$ is the spacing between node i and j. If a homogeneous grid spacing i.e., $\Delta x_{1,2} = \Delta x_{2,3} = \cdots = \Delta$ is used then the above equation reduces to

$$\frac{d^2\psi}{dx^2} = 2\,\frac{\psi_{i+1} - 2\,\psi_i + \psi_{i-1}}{(\Delta x)^2} \tag{4.18}$$

For this work a grid spacing of 0.01 nm has been used. At the first grid point Dirichlet boundary (fixed voltage) condition has been applied. On the other hand at the last grid point Neumann boundary condition has been applied. These boundary conditions are in conformity with the boundary conditions stated in (2.14) and (2.15) of chapter 2 or with those stated in (3.5) and (3.6) of chapter 3.

The matrix equation obtained after discretization has been solved using Newton-Raphson method. Newton-Raphson method is a very powerful method for solving matrix equations. Faster convergence can be achieved with this method if a reasonable initial guess is used.

4.2.4 TCAD simulation

Technology Computer-Aided Design (TCAD) tools are used to automate electronic device design and allows modeling of semiconductor fabrication and semiconductor device operation. They are widely used in semiconductor device simulation for prediction, analysis and test purpose. Modeling device fabrication includes modeling different process steps such as ion implantation and diffusion. TCADs are also very useful to simulate the behavior of electronic devices and to model them based on their underlying fundamental physics. TCADs also allows to create compact models such as for transistors. Many TCAD tools are available nowadays. They provide

facilities to simulate a wide number of semiconductor devices. Here in this simulation ATLAS device simulation software [2] from SILVACO, Inc. has been used to prove validity of the analytical models described in this work.

In this work, a two dimensional device has been simulated in ATLAS which conforms with the device shown in figure 2.1. ATLAS uses *finite element* method to solve differential equations. The spacing between grids has been chosen to vary so that *fine* spacing can be used in critical regions such as at junctions and interfaces. On the other hand *coarse* spacing has been used where variations are expected to be smooth and slow in nature such as inside the oxide layers.

Figure 4.1 shows the structure used for JL DG MOSFET in ATLAS. As can be verified that the channel length is 1 μm. Such a long channel has been used to neglect the effects of *short-channel* effects. On the other hand, 1 μm device width has been used so that *narrow-channel* effects can be avoided . To avoid *parasitic resistance* effect, source and drain lengths are set to be 10 nm [35]. Although poly-silicon gates are usually used but in order to be in conformity with the theoretical analysis metal gates has been used. The workfunction of for this gate metal has been set to 5.33 eV to match with the workfunction difference enlisted in table 4.1.

The doping profile used in ATLAS has been shown in Figure 4.2 which is in conformity with the abrupt nature of analytical models, except for the fact that a default doping concentration of 10^{12} cm^{-3} has been used in oxide layers. The effect of using such low concentration is very negligible as can be seen later.

Since the objective of TCAD simulation is just to validate the analytical models, no rigorous models available in ATLAS has been used. This is why only Boltzmann carrier model has been used. Mobility is a very important parameter necessary to calculate currents. Since mobility depends on doping concentration, concentration dependent mobility model available in ATLAS has been included in the simulation. The mobility values used in the simulation of analytical models are the same as used

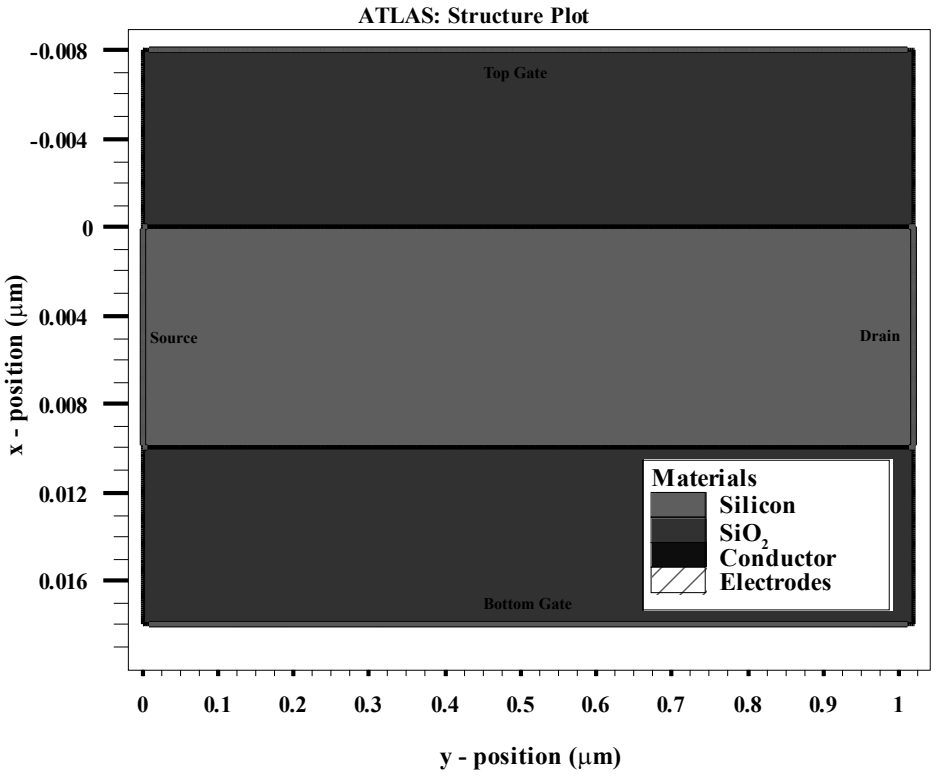


Figure 4.1: Two dimensional structure used for simulation of JL DG MOSFET in SILVACO ATLAS.

in ATLAS and has been enlisted in table 4.2. The full list of mobility values versus doping concentration can be found in ATLAS software manual.

Table 4.2: Mobility of Electrons and Holes in Silicon at $T = 300$ K [2]

Concentration ($\mathbf{cm^{-3}}$)	**Electron mobility** $\mathbf{cm^2\,V^{-1}\,s^{-1}}$	**Hole mobility** $\mathbf{cm^2\,V^{-1}\,s^{-1}}$
6.0×10^{18}	113.6	74.5
8.0×10^{18}	99.5	66.6
1.0×10^{19}	90.5	61.0
2.0×10^{19}	86.9	55.0

4.3 JL DG MOSFET Characteristics

In the previous sections, structure of the simulated device along with different methods of simulation have been discussed. This section and the following sections focus

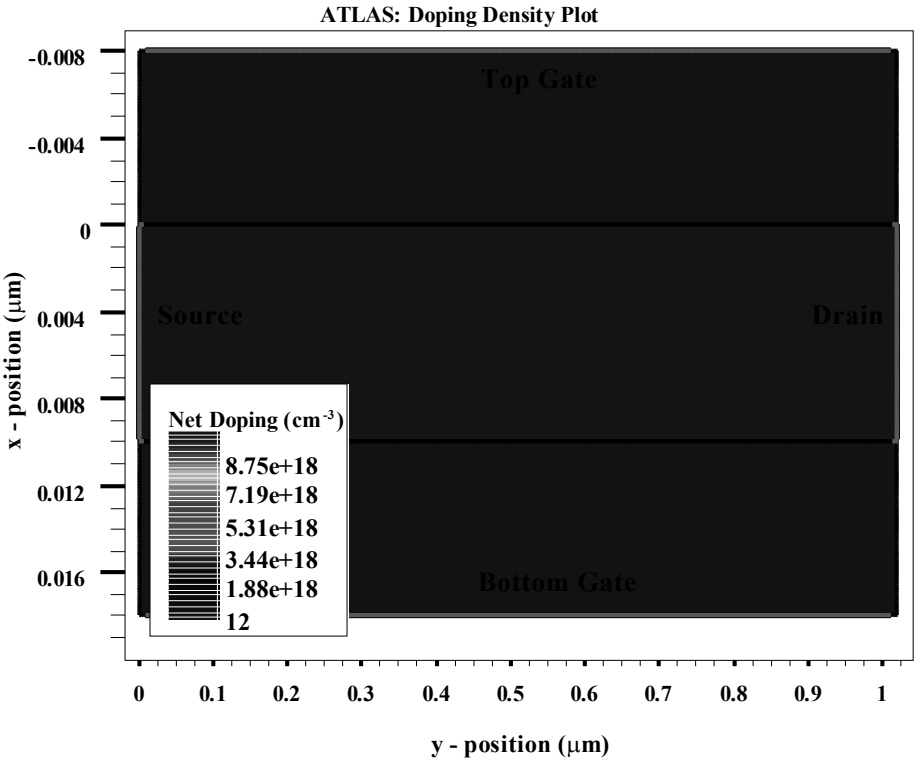


Figure 4.2: Doping profile used for simulation of JL DG MOSFET in SILVACO ATLAS.

on the characteristics of JL DG MOSFET. Surface potential, surface charge and drain current characteristics of this device are analyzed and discussed in detail in this section.

4.3.1 Potential vs. position characteristics

Figure 4.3 depicts the nature of electrostatic potential inside the channel of JL DG MOSFET under deep depletion. The plots cover only the lower half of the channel since a mirror reflection along y axis will produce the results for the upper half of the channel. This nature of is attributed to the symmetric structure used for JL DG MOSFET. It can be checked form the figure that the first-order depletion model matches very well with the exact numerical solution of the Poisson's equation in (2.13).

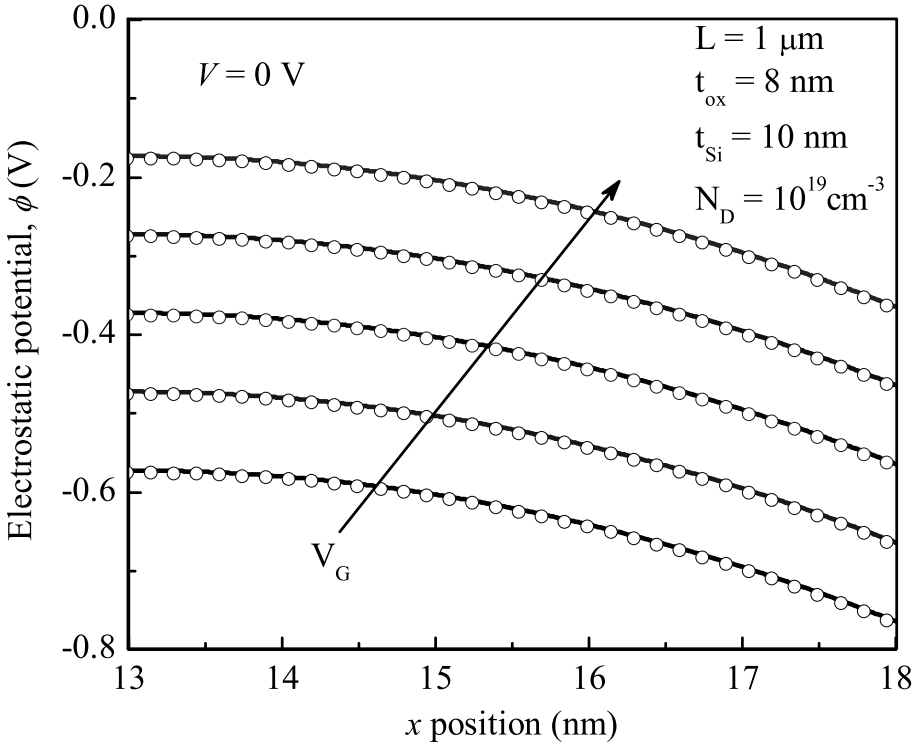


Figure 4.3: Electrostatic potential in depletion versus x coordinate of position variable for gate voltage values below threshold ranging from −1.5 V to −1.1 V in steps of 0.1 V. Numerical solutions using MATLAB (Symbols). First-order model results (Solid lines).

The potential under deep depletion for a particular gate voltage attains its maximum value at the center of the channel and falls non-linearly towards the oxide-semiconductor interfaces. The value of center potential and surface potential increases with gate voltage. The spacing between the curves decreases slowly as the gate voltage rises.

4.3.2 Surface Potential vs. Gate Voltage characteristics

The key parameter underlying the development of two models discussed here is the surface potential. For this reason it is very important to observe and analyze the surface potential versus gate voltage characteristics from deep depletion to strong

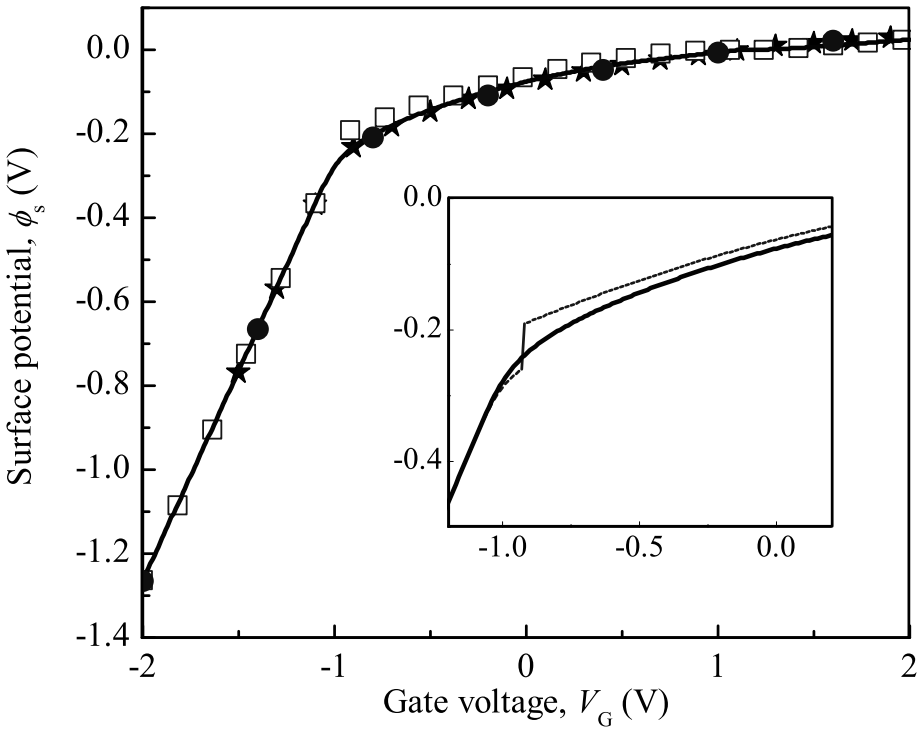


Figure 4.4: Surface potential of the JL DG MOSFET plotted against the gate voltage. (Stars) SILVACO ATLAS simulation. (Squares) Abrupt model. (Circles) MATLAB simulation. (Line) First-order model. (Inset) Expanded view of transition from full depletion to partial depletion - solid line corresponds to first-order model and dashed line represents abrupt depletion model.

accumulation. Figure 4.4 shows surface potential characteristics for a JL DG MOSFET and compares the result obtained from the first order model with those obtained from the abrupt depletion model and numerical simulations. It is very clear from the figure that surface potential obtained from the first-order depletion model matches very well with both numerical and TCAD solutions from the whole range of gate voltage from deep depletion to strong accumulation. On the other hand, the surface potential obtained from the abrupt model fails to match with numerical solutions in partial depletion region where it simply overestimates surface potential than its true value. Another weak point of the abrupt depletion based surface potential model is that there is a *discontinuity in transition* from deep depletion to partial depletion

around the threshold voltage. In reality surface potential always varies continuously with gate voltage. Therefore abrupt depletion based model fails to provide the correct picture and may cause convergence problems in SPICE like programs.

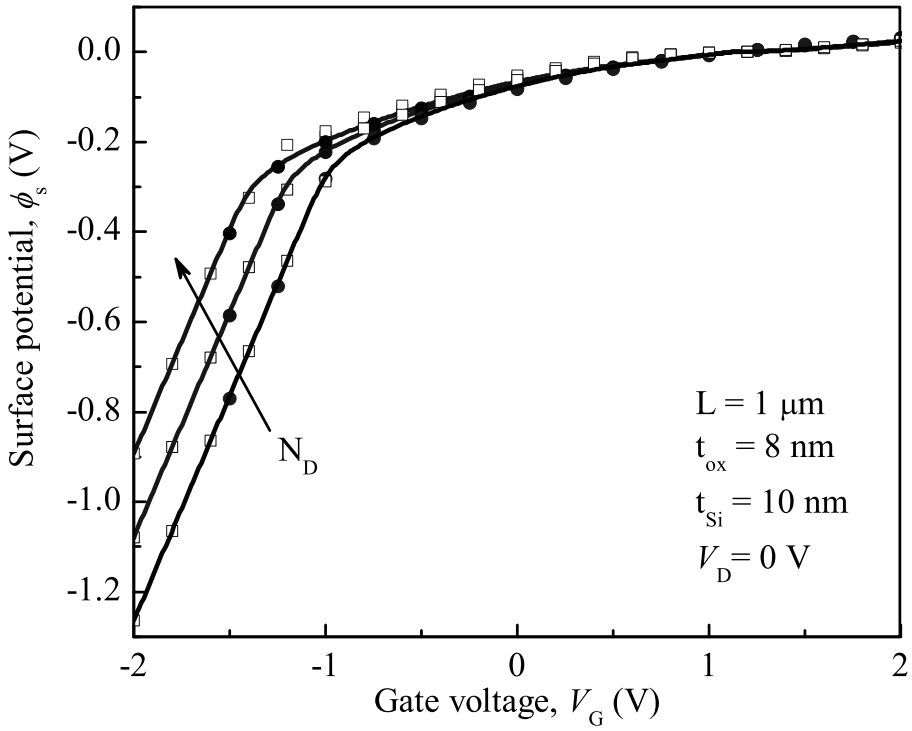


Figure 4.5: Surface potential of the JL DG MOSFET plotted against the gate voltage for N_D ranging from 10^{19} cm^{-3} to 1.2×10^{19} cm^{-3} in steps of 1×10^{18} cm^{-3}. (Solid symbols) MATLAB simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

Figure 4.5 to 4.8 demonstrates the dependencies of the surface potential versus gate voltage characteristics with respect to various parameters. These parameters include doping concentration, oxide thickness, channel thickness and quasi-Fermi potential. Change in each of these parameters affects surface potential characteristics differently.

The effect of increasing doping concentration is that it shifts the characteristics towards left that is as the doping concentration increases threshold voltage becomes more negative. There is no visible change in the accumulation region.

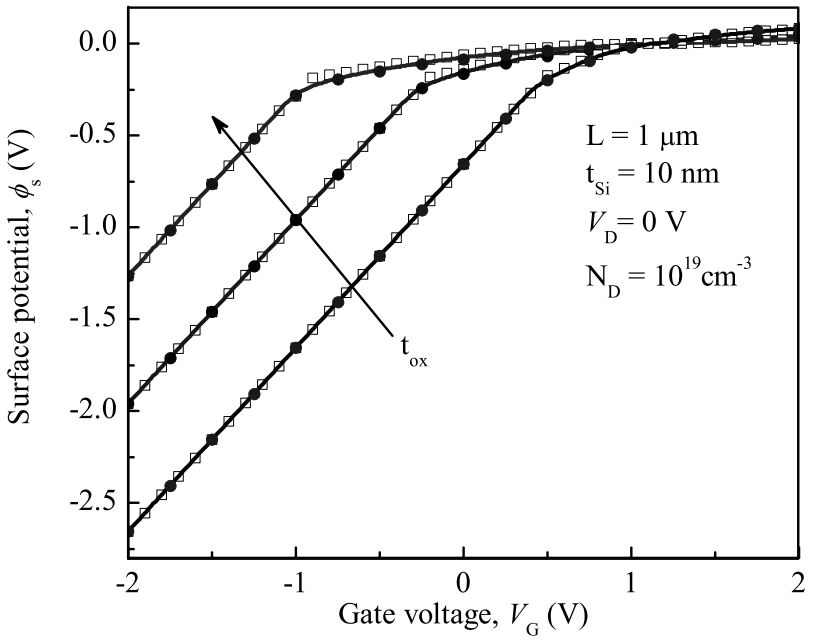


Figure 4.6: Surface potential of the JL DG MOSFET plotted against the gate voltage for t_{ox} ranging from 2 nm to 8 nm in steps of 3 nm. (Solid symbols) MATLAB simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

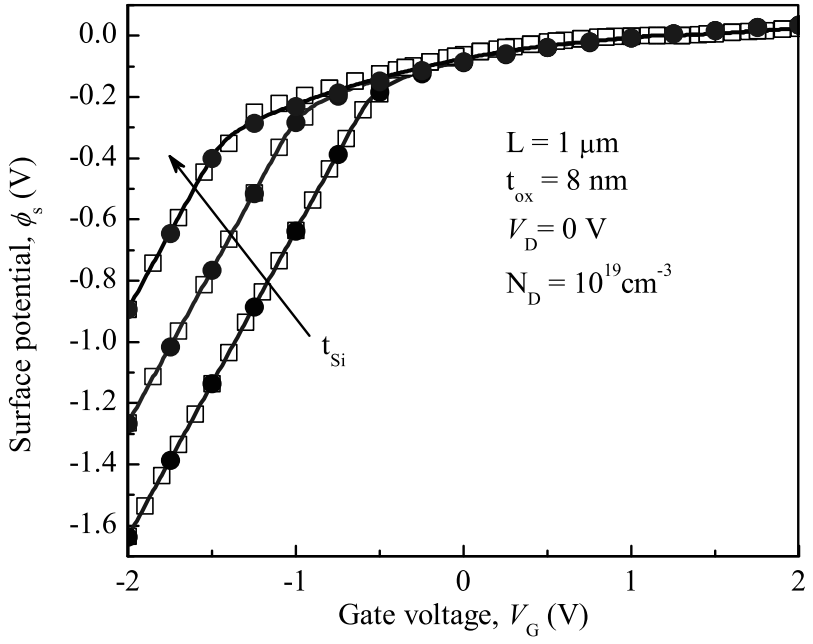


Figure 4.7: Surface potential of the JL DG MOSFET plotted against the gate voltage for t_{Si} ranging from 8 nm to 12 nm in steps of 2 nm. (Solid symbols) MATLAB simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

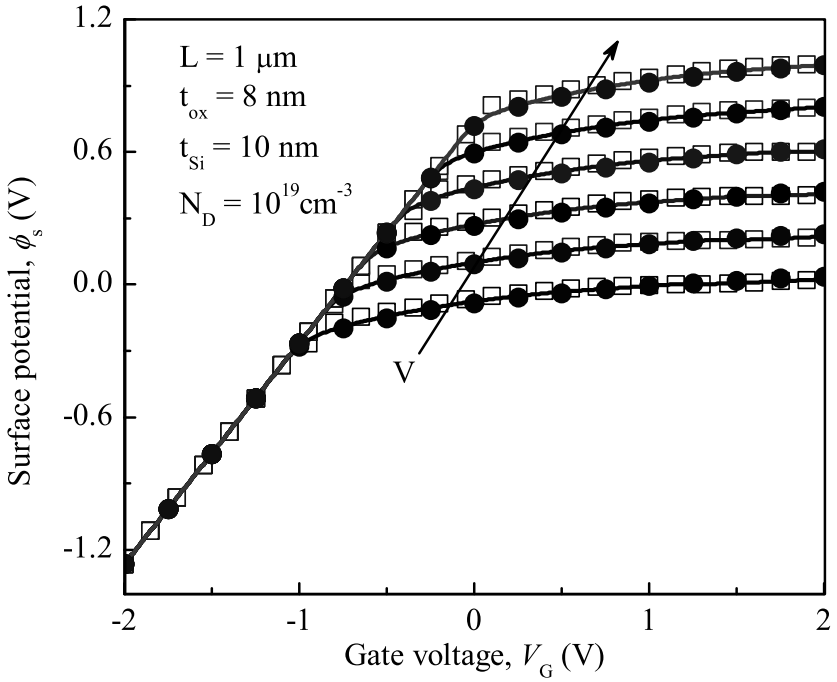


Figure 4.8: Surface potential of the JL DG MOSFET plotted against the gate voltage for V ranging from 0 V to 1 V in steps of 0.2 V. (Solid symbols) MATLAB simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

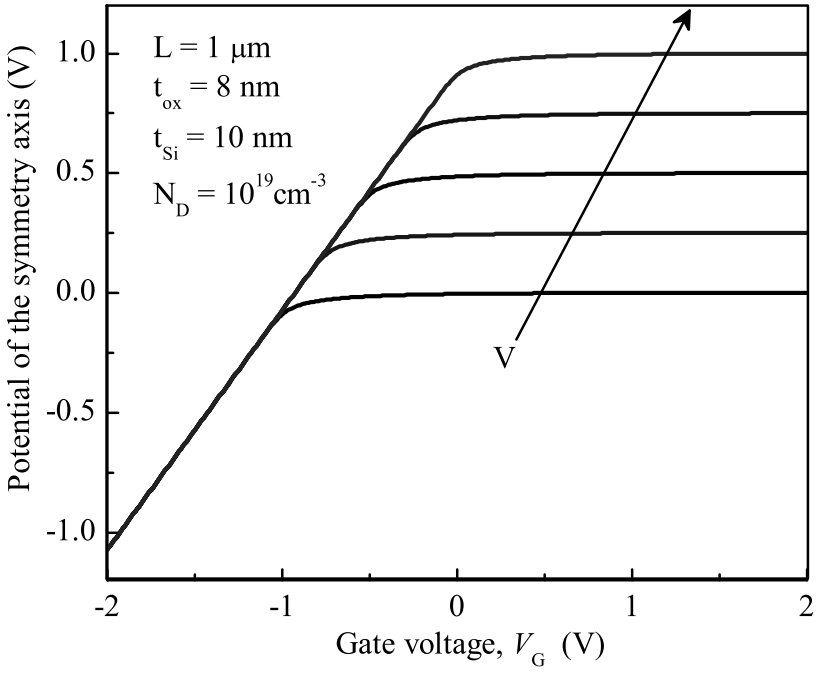


Figure 4.9: Potential of the symmetry axis of the JL DG MOSFET plotted against the gate voltage for V ranging from 0 V to 1 V in steps of 0.25 V.

On the other hand, increasing gate oxide thickness shifts the subthreshold region of the characteristics towards left which also means a decrease in threshold voltage. There is another effect of increasing oxide thickness - the surface potential in accumulation slowly reduces. As gate oxide thickness increases more gate voltage drops across the gate oxide and less potential drops inside the channel.

Increasing channel thickness also shifts threshold voltage towards negative. This time it is not an exact left shift because the surface potential value also shifts down in the subthreshold region. Increasing quasi-Fermi level does not affect the subthreshold region but increases the surface potential value in accumulation region. In all the figures, the discrepancies between the abrupt-depletion based surface potential model and first-order depletion model can easily be identified.

Finally in figure 4.9, the potential of the symmetry axis has been plotted against the gate voltage for various values of quasi-Fermi potential. From the figure it can be observed that potential of the symmetry axis remains constant to quasi-Fermi potential up to the transition from partial depletion to full depletion. It then falls linearly with the decrease in gate voltage in strong depletion.

4.3.3 Charge vs. Gate Voltage characteristics

In figure 4.10 and 4.11, space charge density and mobile charge density characteristics from subthreshold to strong accumulation have been shown. Space charge density is *negative* for gate voltage greater than flatband voltage whereas *mobile charge density is always negative*. Therefore in these figures *absolute* values of space charge and mobile charge densities per unit area within the channel region have been plotted against gate voltage. To have better understanding about the number of carriers involved, these plots have been *normalized* with respect to free electron charge.

Results from the first order model has been compared against abrupt model and numerical solution obtained from MATLAB. It is clear from the figure that both

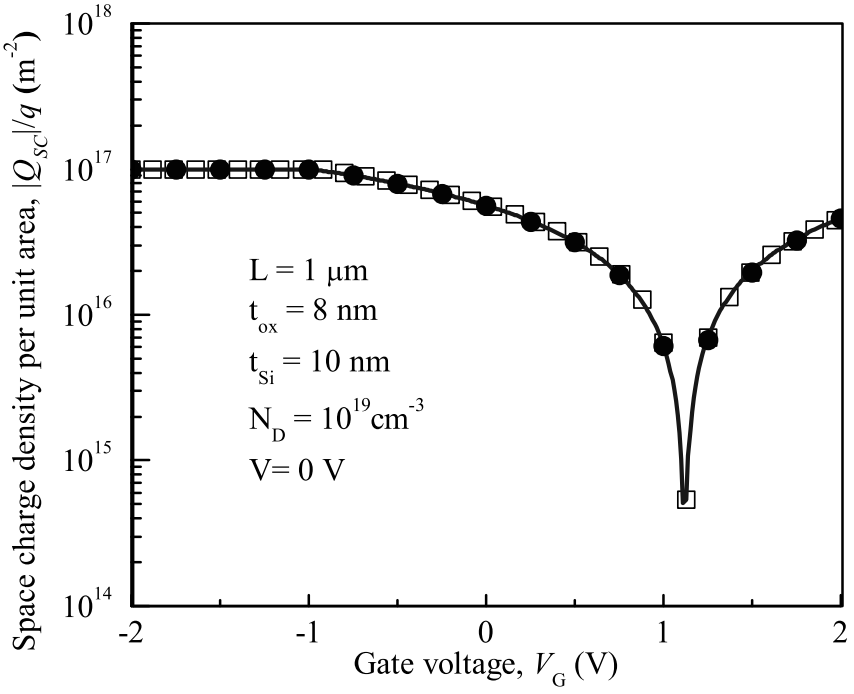


Figure 4.10: Space charge density of JL DG MOSFET plotted against the gate voltage for $V = 0$. (Solid symbols) MATLAB simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

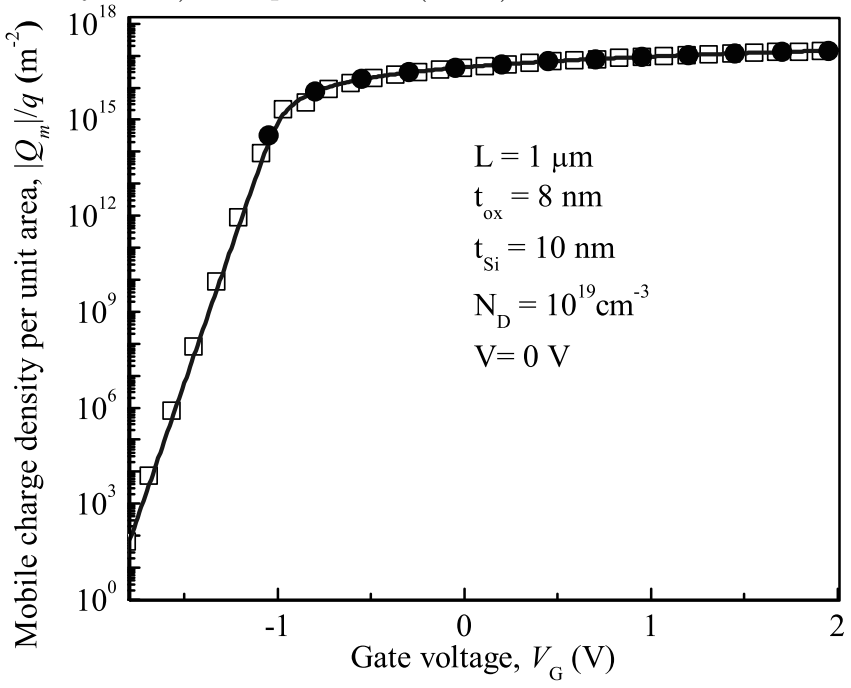


Figure 4.11: Mobile charge density of JL DG MOSFET plotted against the gate voltage for $V = 0$. (Solid symbols) MATLAB simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

models are in excellent agreement with numerical simulation. In deep depletion charge density is almost constant which is quite reasonable because the channel region has already been fully depleted. The increased voltage drop in this region of operation leads to drastic change in mobile charge density but is still quite small compared to fixed charge density. The linear change in log scale translates into an exponential increase in mobile charge density under deep deletion.

As the region of operation shifts from deep depletion to partial depletion, the channel starts to be depleted partially. Therefore space charge value starts to decrease in magnitude. Also the exponential increase in mobile charge density ceases and starts to saturate as it enters into accumulation. The sharp notch in the plot implies zero space charge density which occurs in flatband condition. This notch appears because of logarithmic nature of plot. In reality there is no sharp change in magnitude of space charge density.

In strong accumulation, a large increase in gate voltage causes a small increase in mobile charge density and hence in accumulation both space charge and mobile charge densities have slow increment and almost tend to saturate.

4.4 Current-Voltage Characteristics

This section reveals the most desirable characteristics of the JL DG MOSFET - its current-voltage characteristics. These characteristics are important because the properties of these characteristics can be used to judge the efficacy and suitability of using JL DG MOSFET in real applications. Two types of current-voltage characteristics will be considered here. The first one is the transfer characteristic which is also known as turn-on characteristics in the literature. The second important current-voltage characteristic is the output characteristic of the JL DG MOSFET. Emphasis will be given on the superiority of first order depletion model over the traditional abrupt depletion model in modeling these characteristics. There will be

a discussion on output conductance and transconductance of the device at the end of the section.

4.4.1 Transfer characteristics

Transfer characteristics help to determine many important MOSFET properties like turn-on current, turn-off current, subthreshold swing/slope and so on. From these properties one can choose the desired MOSFET from various types of MOSFETs for integrated circuit designs. In figures 4.12 to 4.15, transfer characteristics for JL DG MOSFET have been demonstrated. These figures also illustrates the dependencies of transfer characteristics on various MOSFET parameters such as doping concentration, gate oxide thickness, channel thickness and quasi-Fermi potential. These dependencies have shown both in normal and logarithmic scale to make it easy for the readers to get a comprehensive idea about these characteristics. The results obtained from the first-order model have been compared against the abrupt depletion model and ATLAS TCAD simulation to prove the validity and superiority of first order modeling. It can be seen from the figures that first order model better approximates the transfer characteristics than the abrupt model does.

The abrupt model fail to match with TCAD results in partial depletion region and shows discontinuity at the transition from deep depletion to partial depletion. Also in the partial depletion region abrupt model overestimates the current than TCAD results. These discontinuities appear in the transfer characteristics due to the presence of discontinuities in the surface potential characteristics. Both abrupt depletion and first order model deviates slightly from TCAD results in accumulation region. This may be due to the oversimplification of surface potential in this region.

4.4.2 Output characteristics

The output characteristics of JL DG MOSFET have been shown in figure 4.16. To prove the validity of the results obtained from the first order model, comparison

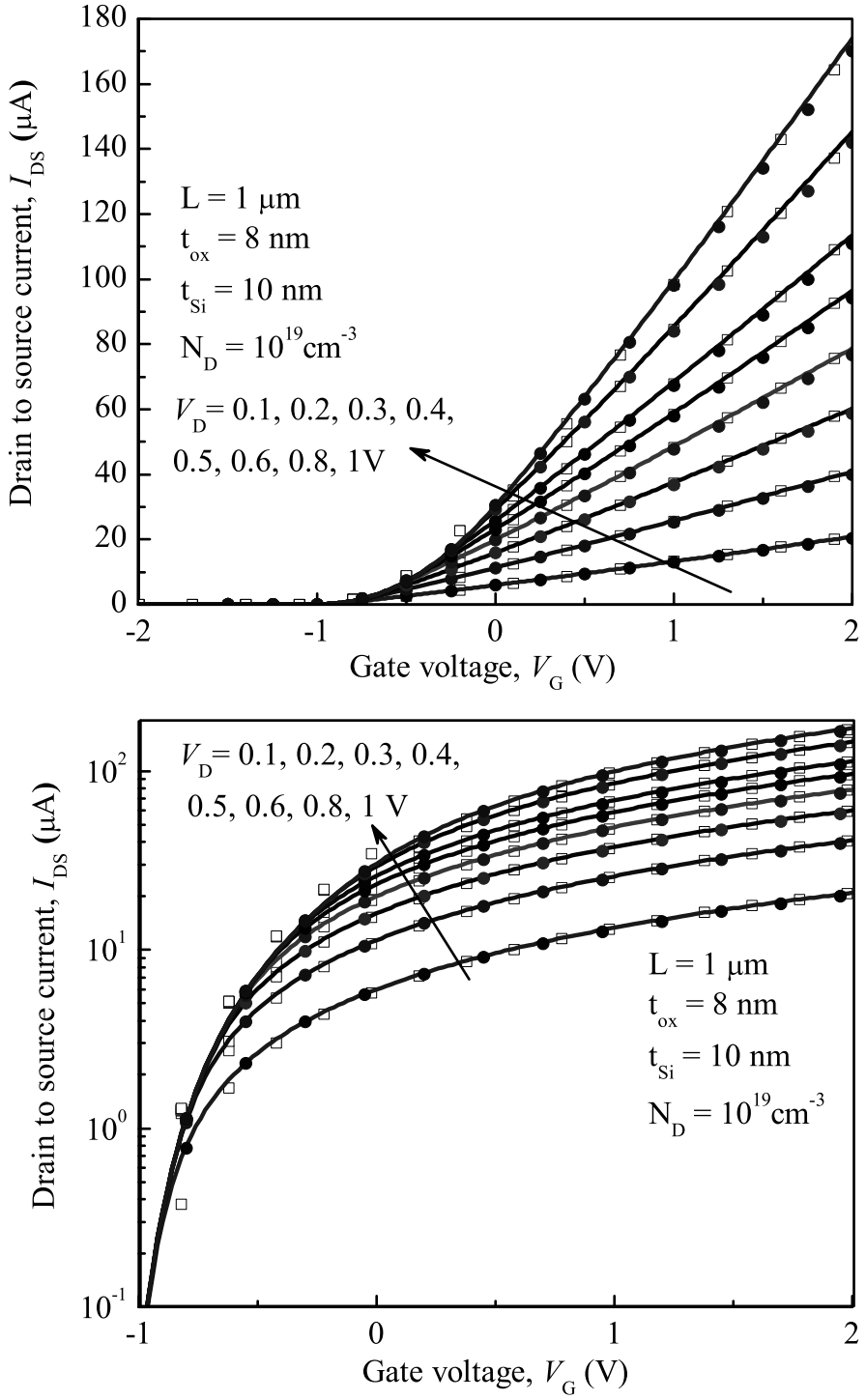


Figure 4.12: Transfer characteristic obtained from the proposed model of the JL DG MOSFET for different values of V_{DS} ranging from 0.1 V to 0.8 V. (Top) Normal scale, (Bottom) y-axis in logarithmic scale. (Solid symbols) ATLAS simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

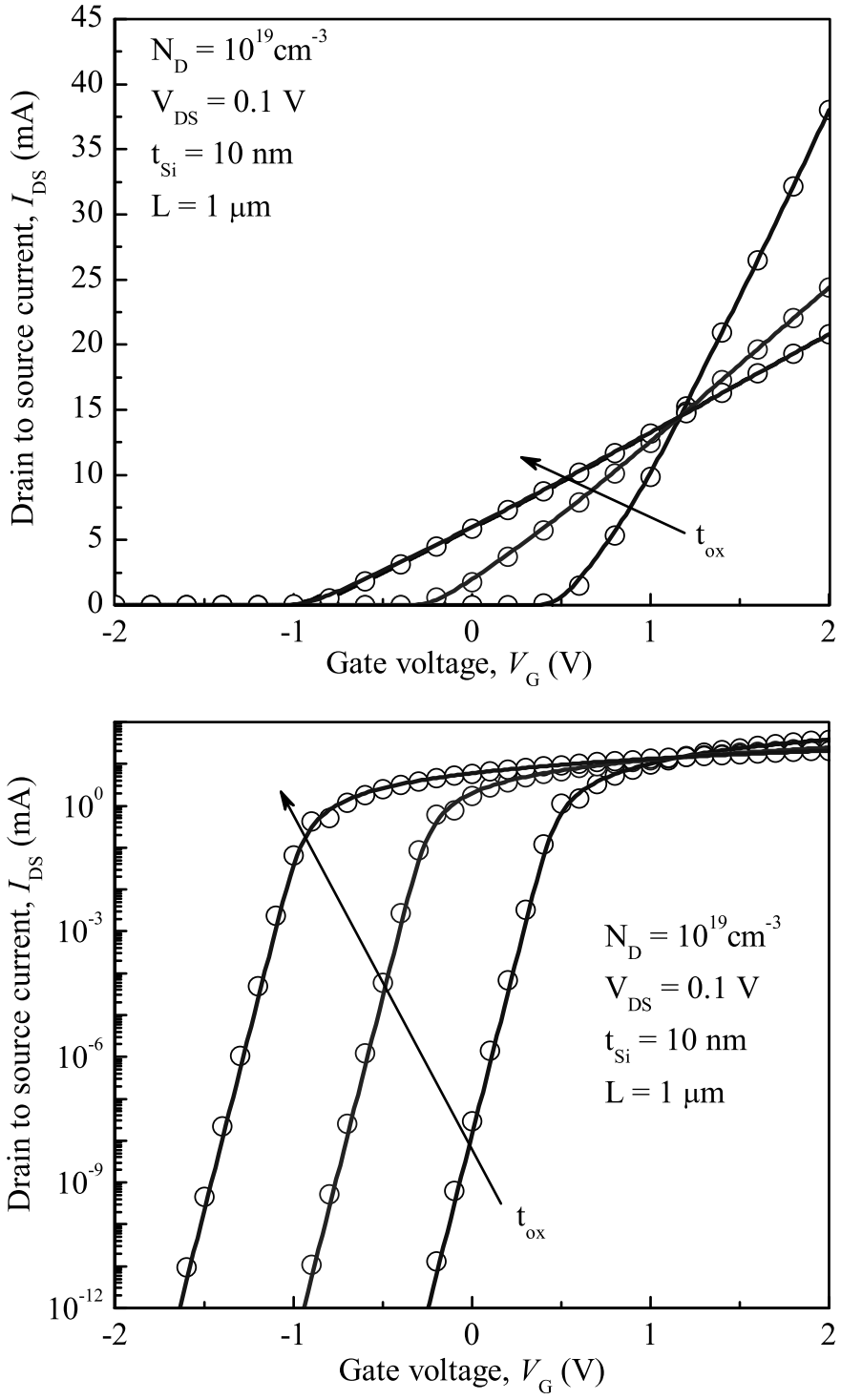


Figure 4.13: Transfer characteristic obtained from the proposed model of the JL DG MOSFET for t_{ox} ranging from 2 to 8 nm in steps of 3 nm. (Top) Normal scale, (Bottom) y-axis in logarithmic scale. (Symbols) Abrupt model. (Lines) First-order model.

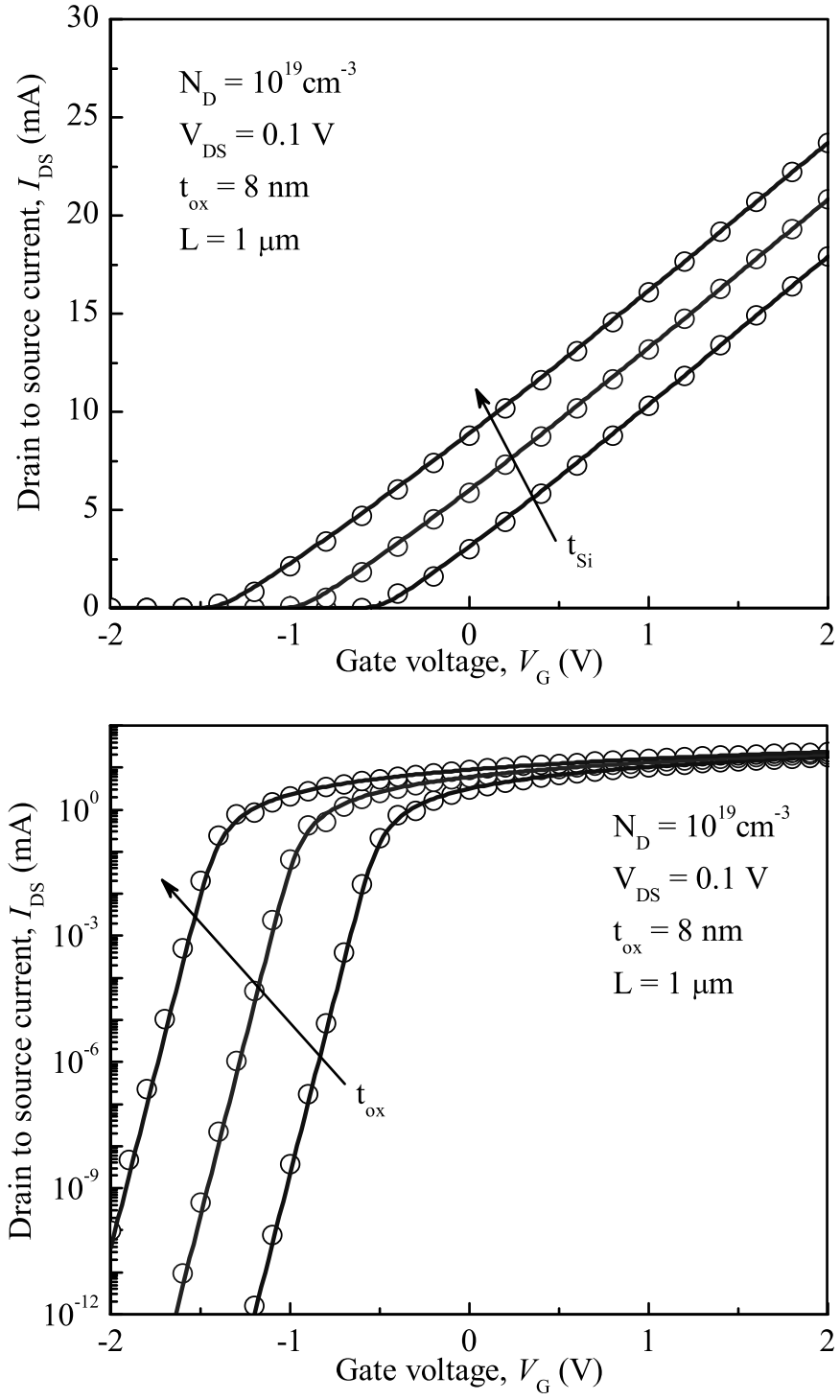


Figure 4.14: Transfer characteristic obtained from the proposed model of the JL DG MOSFET for t_{Si} ranging from 8 nm to 12 nm in steps of 2 nm. (Top) Normal scale, (Bottom) y-axis in logarithmic scale. (Symbols) Abrupt model. (Lines) First-order model.

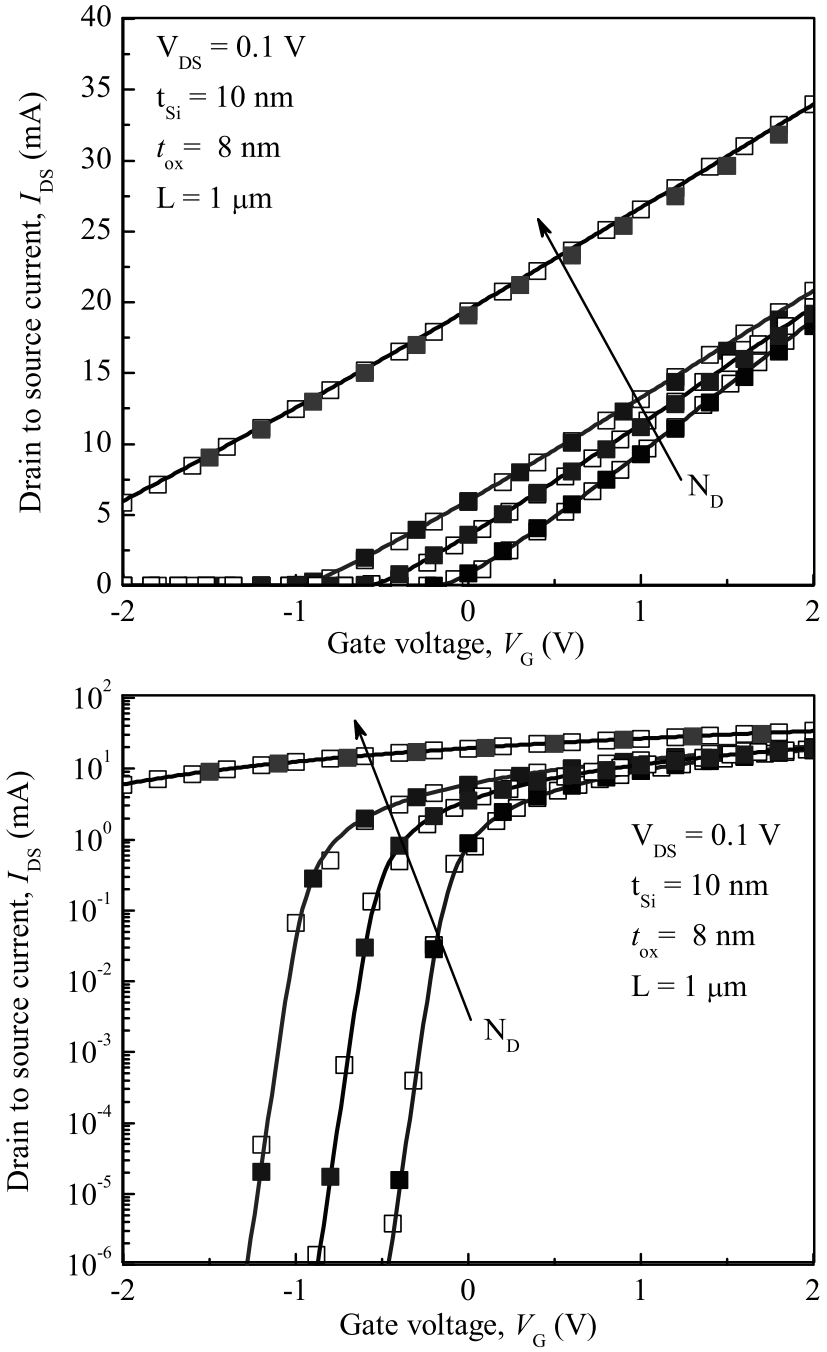


Figure 4.15: Transfer characteristic obtained from the proposed model of the JL DG MOSFET for $N_D = 6 \times 10^{18}$, 8×10^{18}, 10^{19} and 2×10^{19} cm^{-3} , corresponding to μ varying among 113.6, 99.5, 90.5 and 86.9 cm^2/V $\cdot$ s. (Top) Normal scale, (Bottom) y-axis in logarithmic scale. (Solid symbols) ATLAS simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

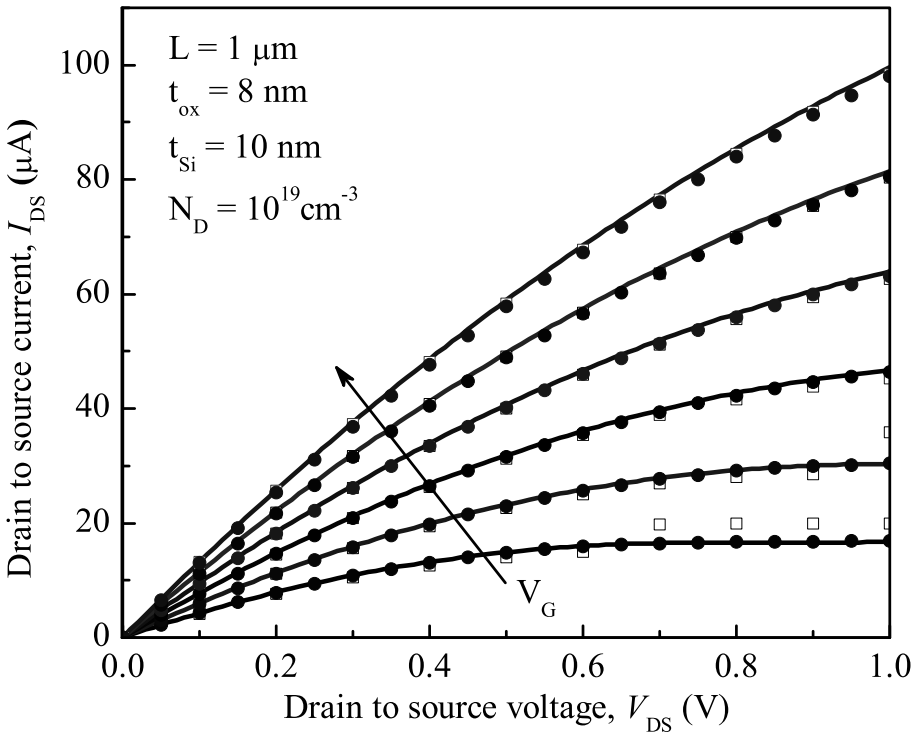


Figure 4.16: Output characteristic calculated from the proposed model of the JL DG MOSFET for V_G ranging from -0.25 V to 1 V in steps of 0.25 V. (Solid symbols) SILVACO ATLAS simulation. (Hollow symbols) Abrupt model. (Lines) First-order model.

have been made with abrupt model and TCAD simulations. A very good agreement with TCAD simulations have been obtained. Abrupt model slightly deviates from the TCAD solutions. The reason for this may be the poor accuracy of this model in modeling of surface potential since drain current calculation is dependent on the values of surface potential.

In the output characteristics, drain to source current, I_{DS} have been plotted against drain to source voltage, V_{DS} ranging from 0 V to 1 V. within this range saturation in I_{DS} is observed only for very low gate voltages. For higher gate voltages, the channel remains in partial depletion region and saturation is not achieved.

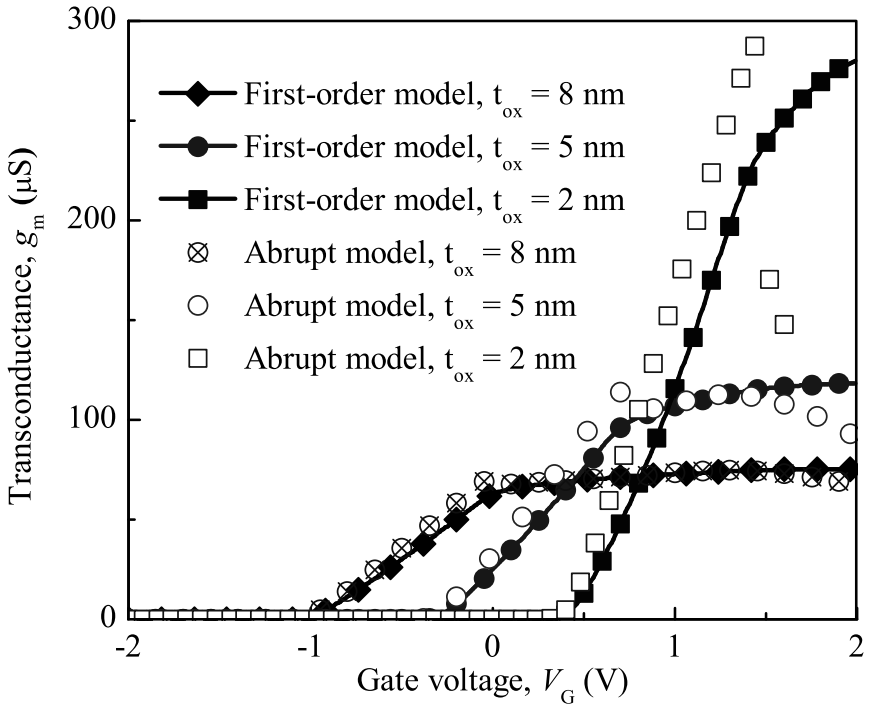


Figure 4.17: Transconductance obtained from the proposed model of the JL DG MOSFET for t_{ox} ranging from 2 nm to 8 nm in steps of 3 nm.

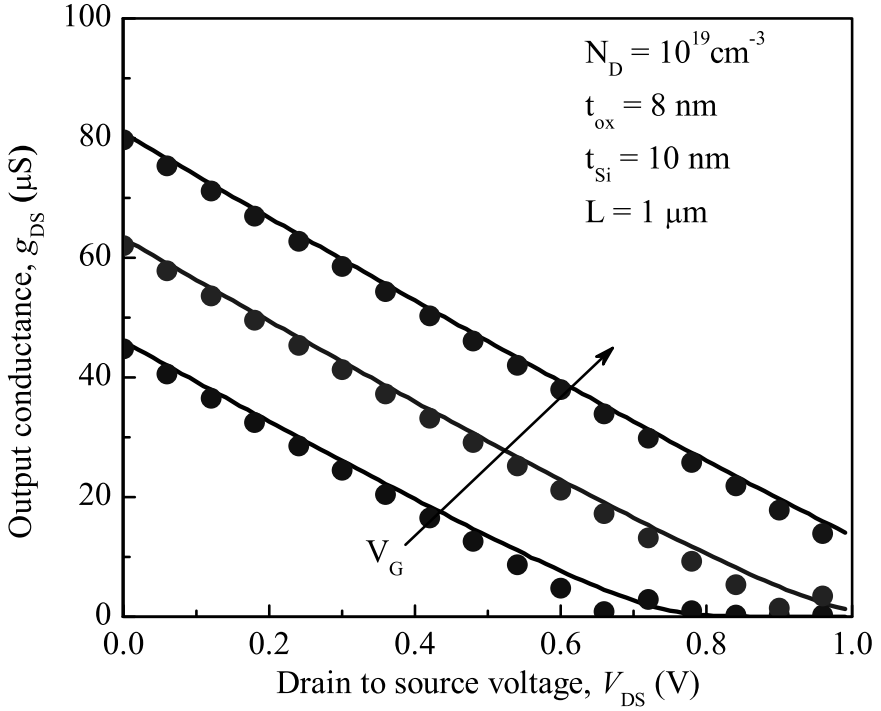


Figure 4.18: Output conductance obtained from the proposed model of the JL DG MOSFET for V_G ranging from −0.25 V to 0.25 V in steps of 0.25 V. (Symbols) Abrupt model. (Lines) First-order model.

4.4.3 Transconductance and Output conductance

Figure 4.17 and 4.18 demonstrate the transconductance and output conductance characteristics of JL DG MOSFET respectively. Transconductance and output conductance characteristics as obtained from the analytical equations predicted by abrupt depletion model has also been plotted alongside with those predicted by first order depletion model. The transconductance of a JL DG MOSFET is defined as

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{4.19}$$

On the other hand the output conductance of a JL DG MOSFET is given by

$$g_d = \frac{dI_{DS}}{dV_{DS}} \tag{4.20}$$

Tranconductance value of JL MOSFET increases rapidly with the decrease in gate oxide thickness which is expected because it is easier for the gate terminal to control charges inside the channel with thin gate oxide. The thinner the gate oxide the lower the voltage drop across the gate oxide. Saturated tranconductance value is also higher for thinner gate oxide JL DG MOSFETs. Another important point to note about the transconsuctance is that the thinner the gate oxide the higher the gate voltage required to achieve sufficient transconductance value.

Output conductance for a JL DG MOSFET decreases almost linearly with the increase in drain to source voltage, V_{DS} for a particular gate voltage. With the increase in gate voltage this characteristic shifts up.

First order depletion model predicts the characteristics better than the abrupt depletion model as evident from the figures. Abrupt model in particular shows very poor result in transconductance characteristics modeling. This deviation is prominent for thinner gate oxide thickness.

4.5 Capacitance-Voltage (CV) Characteristics

The nature of the capacitance-voltage (C-V) characteristics of JL DG MOSFET is quite different compared to the conventional bulk MOSFETs because of the junctionless nature of the MOSFET and the presence of two oxide-semiconductor interfaces. Capacitance in JL DG MOSFETs originates from the capacitance of two gate oxides and the capacitance of the channel. The dependence of total capacitance of a JL DG MOSFET with gate oxide capacitance and channel capacitance can be established from the definition of capacitance

$$C = \frac{dQ_G}{dV_G} = -\frac{dQ_{SC}}{dV_G} \tag{4.21}$$

where C is the total capacitance of a JL DG MOSFET and Q_G is the gate charge per unit area. The rightmost term is originated from the fact that charge balance relation still applies i.e.,

$$Q_G + Q_{SC} = 0$$

With the help of (2.5), it is possible to modify (4.21) as

$$C = -\frac{dQ_{SC}}{d\left(V_{FB} - \dfrac{Q_{SC}}{2C_{ox}} + \phi_s\right)} = \frac{-\dfrac{dQ_{SC}}{d\phi_s}}{\dfrac{d\left(V_{FB} - \dfrac{Q_{SC}}{2C_{ox}} + \phi_s\right)}{d\phi_s}} = \frac{-\dfrac{dQ_{SC}}{d\phi_s}}{1 + \dfrac{1}{2C_{ox}}\left(-\dfrac{dQ_{SC}}{d\phi_s}\right)} \tag{4.22}$$

If channel capacitance, C_{ch} is defined as

$$C_{ch} = -\frac{dQ_{SC}}{d\phi_s} \tag{4.23}$$

then (4.22) can be modified to

$$C = \frac{C_{ch}}{1 + \dfrac{C_{ch}}{2C_{ox}}} = \frac{1}{\dfrac{1}{C_{ch}} + \dfrac{1}{2C_{ox}}} \tag{4.24}$$

Now, (2.33) defines the surface charge in depletion which in turn helps to estimate C_{ch} as

$$C_{ch} = -\frac{dQ_{SC}}{d\phi_s} = -2qN_D\frac{dx_d}{d\phi_s} \tag{4.25}$$

To calculate $\dfrac{dx_d}{d\phi_s}$, first (2.32) is set with $V = 0$

$$\phi_s = -\frac{qN_D}{2\epsilon_{Si}}x_d^2 \Rightarrow \frac{dx_d}{d\phi_s} = -\frac{\epsilon_{Si}}{qN_D x_d} \tag{4.26}$$

The final expression for C_{ch} can be found as

$$C_{ch} = \frac{2\epsilon_{Si}}{x_d} \tag{4.27}$$

In accumulation, there is no depletion layer i.e., $x_d = 0$, therefore C_{ch} approaches to infinity. Actually in accumulation, there is an accumulation layer of electrons whose width is negligible and can be considered as surface charge. Hence in strong accumulation

$$C = 2C_{ox}$$

As the JL DG MOSFET enters into depletion and the region of operation shifts to deep depletion, x_d increases from zero which in turn lowers channel capacitance and hence the total capacitance. As there is no inversion in JL DG MOSFET hence total capacitance continues to decrease with decreasing gate voltage. Reflection of these words is found in figure 4.19 where normalized total capacitance C/C_{ox} has been plotted. Results from analytical models and TCAD solutions have also been

plotted in the same figure. It is readily observable that first-order model has better agreement with TCAD results.

In figures 4.20 to 4.22, dependencies of C-V characteristics on different parameters such as gate oxide, channel thickness and doping concentration have been depicted.

4.6 Threshold Voltage Characteristics

Threshold voltage is a significantly important parameter of a JL DG MOSFET. This section concentrates on the parameters those affect the threshold voltage of a JL DG MOSFET. The factors whose effects will be discussed in this context are channel thickness, gate oxide thickness and doping concentration.

Figure 4.23 demonstrates the effect of increasing gate oxide thickness on threshold voltage of a JL DG MOSFET. The figure shows that with the increase in gate oxide thickness, V_{TH} continues to decrease. From classical viewpoint, the explanation is simple. As the oxide thickness increases, so does the voltage drop across the oxide. Therefore more negative voltage on gate terminal is required to deplete the channel as the gate oxide increases.

The effect of increasing channel thickness on threshold voltage of a JL DG MOSFET has been shown in figure 4.24. As can be seen from the figure that V_{TH} decreases as the channel thickness increases. The reason behind this is that as the channel thickness increases, more free carriers become available inside the channel region. Putting differently, increasing channel thickness requires more negative gate voltage to deplete the free electrons inside the channel.

Both figure 4.23 and 4.24 also show the effect of doping concentration on threshold voltage. V_{TH} decreases with increasing doping concentration. Again the explanation is the same. Increased doping concentration increases the number of carriers inside

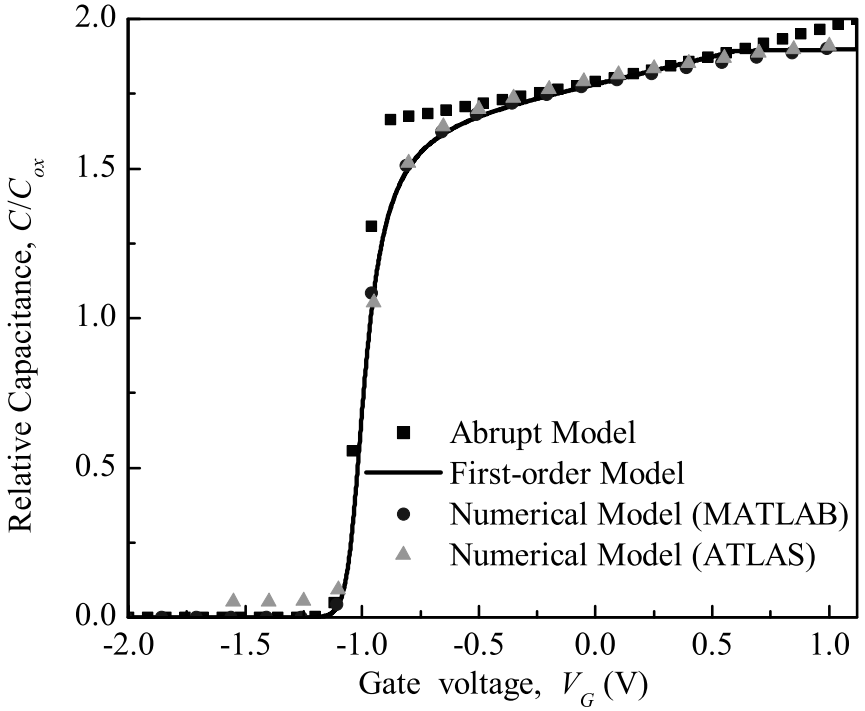


Figure 4.19: Capacitance vs. voltage curve obtained from the proposed model of the JL DG MOSFET.

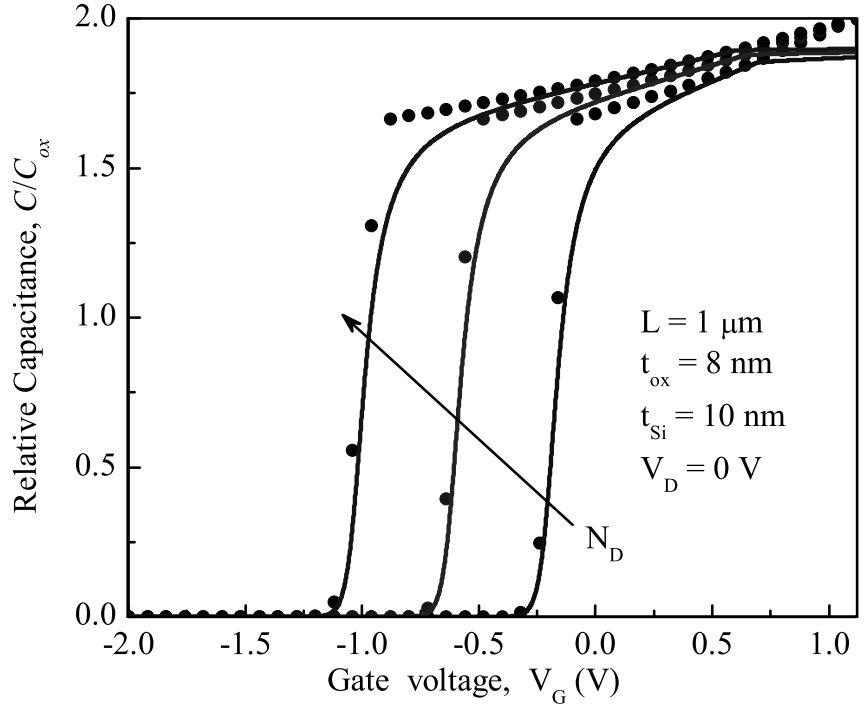


Figure 4.20: Capacitance vs. voltage curve obtained from the proposed model of the JL DG MOSFET for N_D ranging from 6×10^{18} to 10^{19} cm^{-3} in steps of 2×10^{18} cm^{-3}. (Symbols) Abrupt model. (Lines) First-order model.

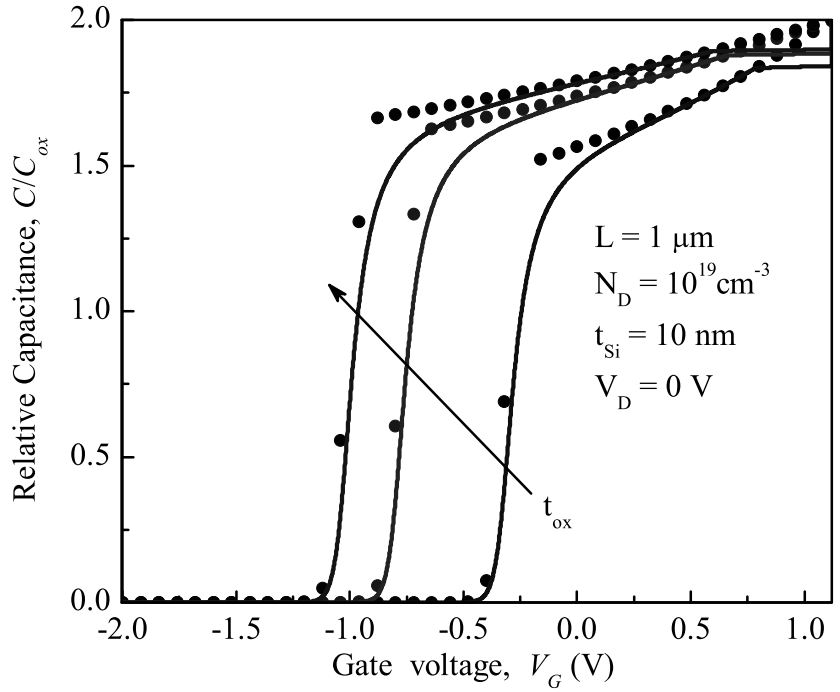


Figure 4.21: Capacitance vs. voltage curve obtained from the proposed model of the JL DG MOSFET for t_{ox} ranging from 2 nm to 8 nm in steps of 3 nm. (Symbols) Abrupt model. (Lines) First-order model.

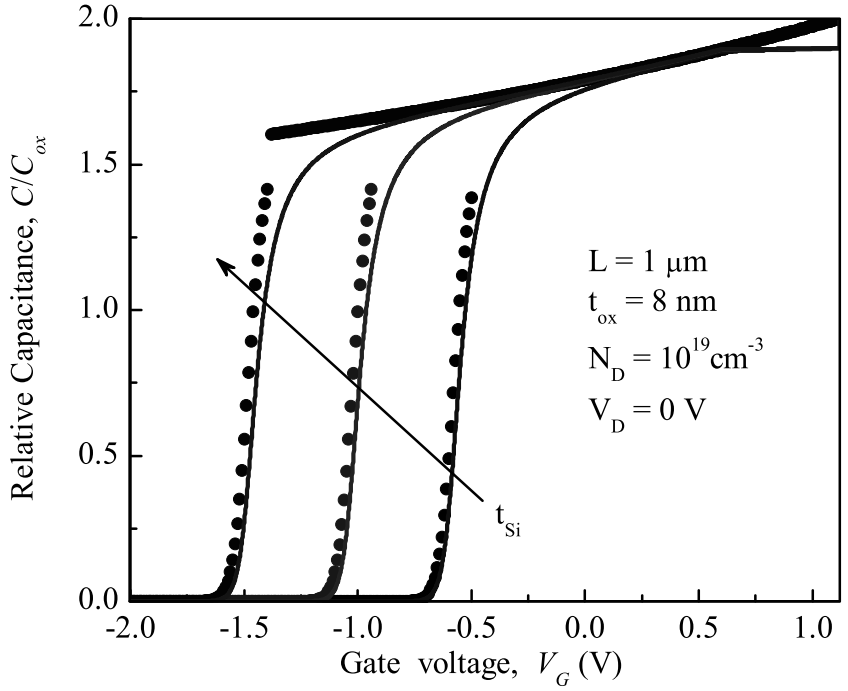


Figure 4.22: Capacitance vs. voltage curve obtained from the proposed model of the JL DG MOSFET for t_{Si} ranging from 8 nm to 12 nm in steps of 2 nm. (Symbols) Abrupt model. (Lines) First-order model.

the channel which requires more negative gate voltage (decreased threshold voltage) to deplete the channel.

For JL DG MOSFETs it is also important to discuss about their threshold voltage shifts. This threshold voltage shift is significantly larger than that of the undoped channel transistor, as mentioned in [40] and [35]. In order to have quantitative knowledge about the threshold voltage shift (ΔV_{TH}) of JL DG MOSFETs, threshold voltage sensitivity of V_{TH} with respect to channel thickness, gate oxide thickness, and doping concentration has been determined here.

These expressions can very easily be obtained by taking variations of (4.16) with respect to t_{si}, t_{ox} and N_D. Then the following expressions can be obtained

$$\Delta V_{TH,N_D} = -\frac{qN_D t_{Si}}{2C_{eff}}\left(\frac{\Delta N_D}{N_D}\right) \tag{4.28}$$

$$\Delta V_{TH,t_{Si}} = -\frac{qN_D t_{Si}}{2}\left[\frac{1}{4C_{Si}}\left(\frac{\Delta t_{Si}}{t_{Si}}\right)^2 + \frac{1}{C_{ox}}\frac{\Delta t_{Si}}{t_{Si}}\right] \tag{4.29}$$

$$\Delta V_{TH,t_{ox}} = -\frac{qN_D t_{Si}}{2C_{ox}}\left(\frac{\Delta t_{ox}}{t_{ox}}\right) \tag{4.30}$$

where $\Delta V_{TH,N_D}$, $\Delta V_{TH,t_{Si}}$, and $\Delta V_{TH,t_{ox}}$ are threshold voltage shifts caused by relative changes of doping concentration, channel thickness and gate oxide thickness respectively. These sensitivities as determined in (4.28) to (4.30) have been plotted in figures 4.25 to 4.27. From these figures it is very much evident that the threshold voltage of JL DG MOSFET is much sensitive to parameter variations. For example, from figure (4.28) it can be found that a 10% variation of N_D would lead a 200 mV shift in threshold voltage. The same behavior can be observed for channel thickness and gate oxide thickness variations.

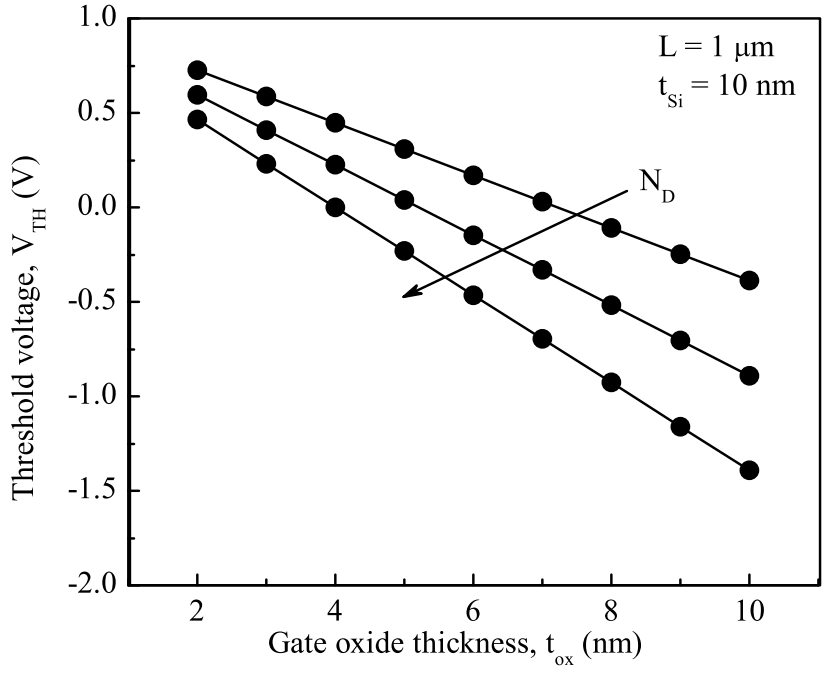


Figure 4.23: Threshold voltage of the JL DG MOSFET for various oxide thicknesses plotted as a parameter of N_D ranging from 6×10^{18} to 10^{19} cm^{-3} in steps of 2×10^{18} cm^{-3}. (Symbols) Abrupt model. (Lines) First-order model.

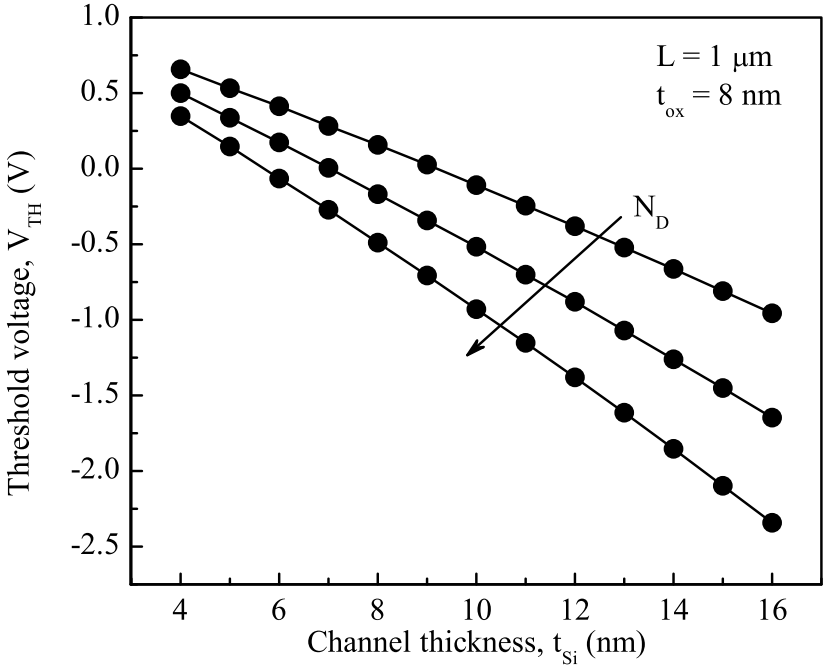


Figure 4.24: Threshold voltage obtained of the JL DG MOSFET for various channel thicknesses plotted as a parameter of N_D ranging from 6×10^{18} to 10^{19} cm^{-3} in steps of 2×10^{18} cm^{-3}. (Symbols) Abrupt model. (Lines) First-order model.

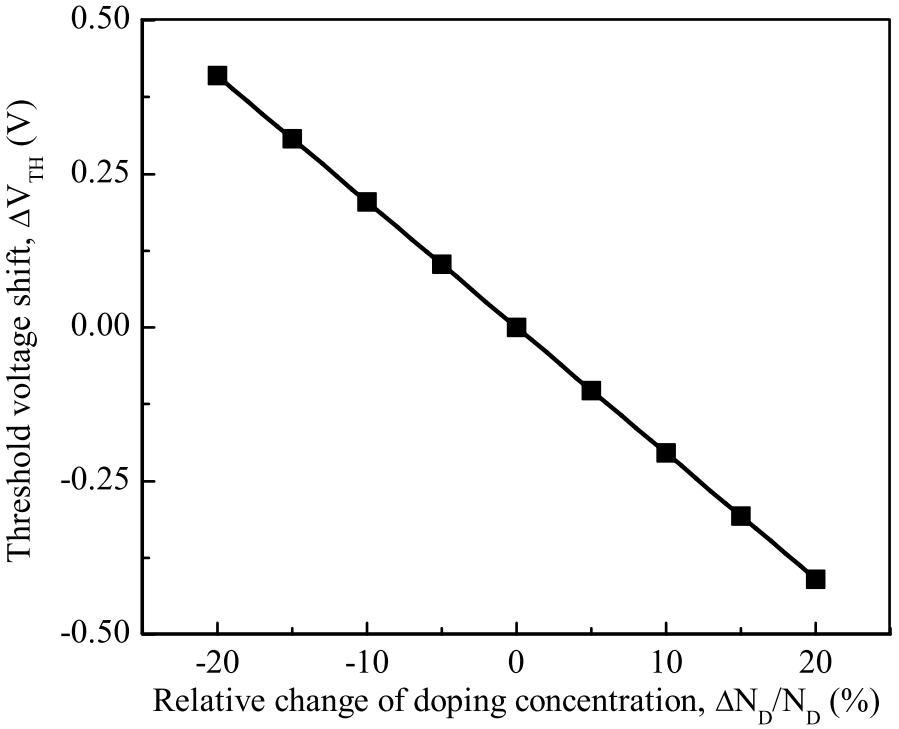


Figure 4.25: Threshold voltage shift obtained from the proposed model of the JL DG MOSFET as a function of the relative change of impurity concentration.

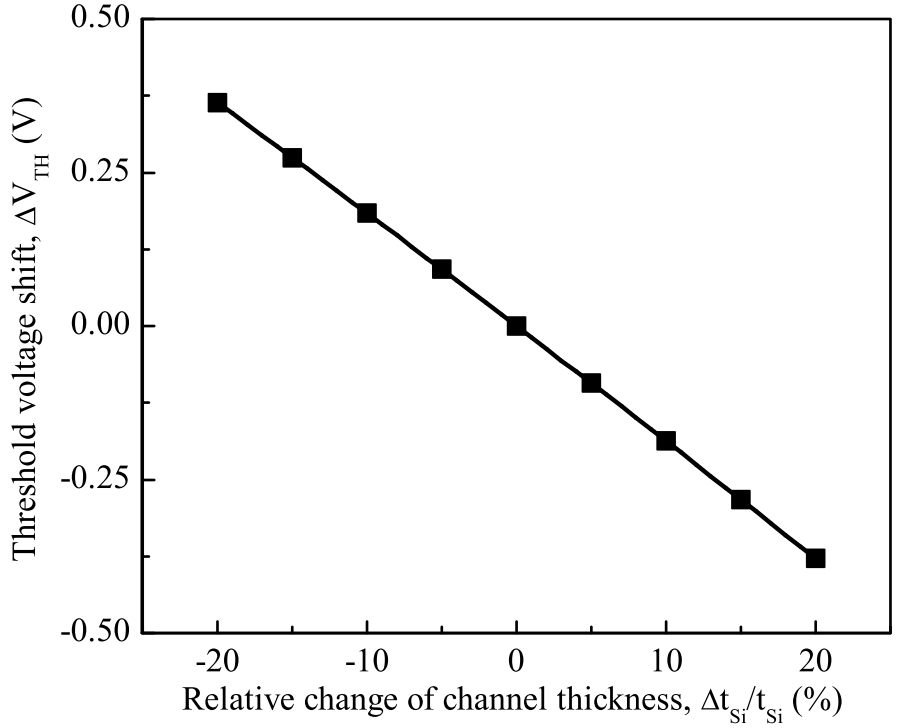


Figure 4.26: Threshold voltage shift of the JL DG MOSFET plotted as a function of the relative change of channel thickness.

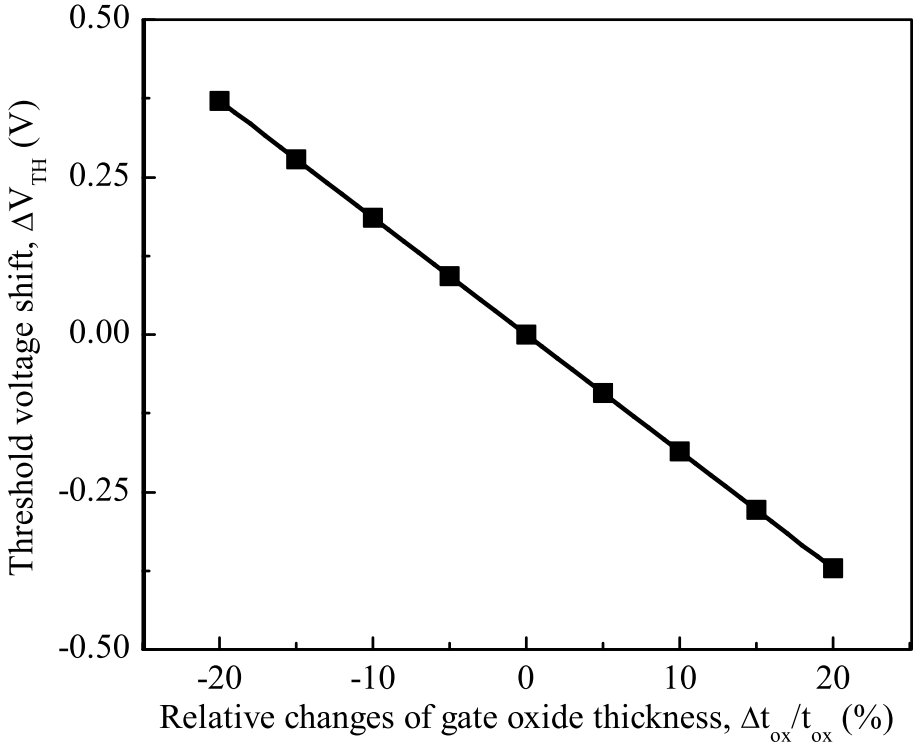


Figure 4.27: Threshold voltage shift of the JL DG MOSFET plotted as a function of the relative change of gate oxide thickness.

5. CONCLUSION

5.1 Summary

In this thesis work, a new analytical model based on gradual depletion has been proposed to calculate the surface potential and the drain current for a symmetric long-channel JL DG MOSFET. Since the proper operation of JL DG MOSFETs require the channel region to be heavily doped, no closed-form solution of Poisson's equation can be found for these device structure. That is why appropriate simplifying assumptions have been made under deep depletion, partial depletion, and accumulation conditions. The proposed model is valid in all regions of operation, i.e., the subthreshold, linear, and saturation regimes and provides improved accuracy in modeling device characteristics which has been verified with the help of numerical simulations from TCAD tools.

With this new model, surface potential and drain current characteristics have been analyzed and effects of different device parameters like channel thickness, gate oxide thickness have been observed and explained. These characteristics are also affected by impurity concentration which has also been studied here. Some other important characteristics of the device such as transconductance and output conductance have been analyzed and interesting results have been obtained. It has been found that transconductance of the device varies significantly with gate oxide thickness.

Capacitance-voltage characteristic of the JL DG device has been examined for varying channel thickness and gate oxide thickness and doping concentration inside the channel of the device. High doping concentration and thick channel can supply

more carriers and thus help the device reach accumulation condition quickly. On the other hand, thick gate oxide reduces the effect of gate voltage by consuming a greater portion of the applied voltage and thus helps to acquire early accumulation.

This works has also portrayed consistent results with the previously examined threshold condition. This has indicated higher sensitivity of threshold voltage on process and device parameters which is supported by earlier results.

The proposed model has been found to provide improved accuracy over the model based on abrupt depletion in analyzing the characteristics of JL DG devices. The proposed model not only provides improved estimations of current and potential values but also provides continuous surface potential and drain current expressions which are extremely important for SPICE modeling. On the contrary the earlier model based on abrupt depletion provides discontinuous results which makes the proposed model a suitable candidate for further investigation of JL DG device characteristics.

5.2 Scope of Future Works

Since this model has been developed considering long channel devices, this model may not be accurate for short channel devices whose normal operation is affected by different short-channel effects (SCE) and narrow channel effects (NCE). The proposed model does not consider these effects. For the sake of simplicity, constant carrier mobility has been employed in derivation of current expressions for JL DG MOSFET.

In 1D analysis, the following works can be included as immediate extensions of the work presented in the thesis.

Field dependent mobility may be calculated for the devices' transport characteristics.

Modeling of asymmetric device can be done. This will provide more parameters to allow more sophisticated control of device characteristics.

Performance of modified JL DG devices can be evaluated. These modifications may include the use of stack gate and high-κ gate oxide.

Quantum effects are not included in the proposed model. In order to include these effects a self consistent analysis can be performed by developing a Schrödinger-Poisson solver.

Gate tunneling current and leakage performance analysis can be included in the simulation, which may carry very interesting information that cannot be obtained from the conventional gate tunneling compact models for JL DG MOSFETs. Tunneling current and leakage performance analysis by pure quantum mechanical treatment is essential for devices' evaluation as an efficient nanoscale transistor.

Interface trap states can be calculated using 1D self consistent analysis. The significance of interface traps calculation lies in its modification of the device's threshold voltage.

Besides these, thorough investigation of the device can be made by developing 2D and 3D device solver which will easily capture short-channel and narrow channel effects. Effect of strain of mobility can also be explored.

Finally, it is required to optimize the structural issues in order to lessen the threshold voltage shift of the JL DGFET due to shift in process and device parameters. It is expected that the model may provide some insight into the design and application of the JL DG MOSFET, a promising candidate for future technology nodes.

Bibliography

[1] S. I. Association, "International Technology Roadmap for Semiconductors," 2013. [Online]. Available: http://www.itrs.net/Links/2013ITRS/Summary2013.htm xvi, 1

[2] *Atlas Device Simulator User's Manual*, SILVACO Int., Santa Clara, CA (USA), 2005. xvi, 55, 56

[3] G. Moore, "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82 –85, jan 1998. 1

[4] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259 –288, mar 2001. 1

[5] G. Moore, "Progress in digital integrated electronics," *IEDM Tech. Digest*, pp. 11 –13, 1975. 1

[6] S. S. Ahmed and D. Vasileska, "Threshold voltage shifts in narrow-width SOI devices due to quantum mechanical size-quantization effects," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 19, no. 1-2, pp. 48 – 52, 2003, fourth International Symposium on Nanostructures and Mesoscopic Systems. [Online]. Available: http://www.sciencedirect.com/science/article/B6VMT-48YW33R-2/2/3f2b203e239943f95216b0494a75d693 2

[7] M. technologyreview, "Tiny Pump Cools Chips," 2006. [Online]. Available: http://www.technologyreview.com/article/17381/ 2

[8] Y. Cheng and C. Hu, *MOSFET MODELING & BSIM3 USERS GUIDE.* USA: KLUWER ACADEMIC PUBLISHERS, 2002, ch. 2. 3

[9] M. L. Green, T. W. Sorsch, G. L. Timp, D. A. Muller, B. E. Weir, P. J. Silverman, S. V. Moccio, and Y. O. Kim, "Understanding the limits of ultrathin SiO_2 and Si—O—N gate dielectrics for sub-50 nm CMOS," *Microelectronic Engineering*, vol. 48, no. 1-4, pp. 25 – 30, 1999, insulating Films on Semiconductors. [Online]. Available: http://www.sciencedirect.com/science/article/B6V0W-4002B25-5/2/b29a6bf6b6dc7ac4c18f812cd7e18b38 3

[10] S. A. Campbell, *The Science and Engineering of Microelectronic Fabrication*, 2nd ed. New Delhi: Oxford University Press, 2007, ch. 5,7. 3

[11] A. Pirovano, A. Lacaita, and A. Spinelli, "Two-dimensional quantum effects in nanoscale MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 49, no. 1, pp. 25 –31, jan 2002. 3

[12] Y. Omura and K. Izumi, "Quantum mechanical influences on short-channel effects in ultra-thin MOSFET/SIMOX devices," *Electron Device Letters, IEEE*, vol. 17, no. 6, pp. 300 –302, jun 1996. 3

[13] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, "Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric," *Applied Physics Letters*, vol. 88, no. 26, p. 263518, 2006. [Online]. Available: http://link.aip.org/link/?APL/88/263518/1 4

[14] Y. Xuan, Y. Wu, and P. Ye, "High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET With Maximum Drain Current Exceeding 1 A/mm," *Electron Device Letters, IEEE*, vol. 29, no. 4, pp. 294 –296, april 2008.

[15] H. Zhao, Y.-T. Chen, J. H. Yum, Y. Wang, N. Goel, and J. C. Lee, "High performance $In_{0.7}Ga_{0.3}As$ metal-oxide-semiconductor transistors with mobility $> 4400\,cm^2/Vs$ using InP barrier layer," *Applied Physics*

Letters, vol. 94, no. 19, p. 193502, 2009. [Online]. Available: http://link.aip.org/link/?APL/94/193502/1

[16] Y. Wu, W. Wang, O. Koybasi, D. Zakharov, E. Stach, S. Nakahara, J. Hwang, and P. Ye, "0.8-V Supply Voltage Deep-Submicrometer Inversion-Mode $In_{0.75}Ga_{0.25}As$ MOSFET," *Electron Device Letters, IEEE*, vol. 30, no. 7, pp. 700 –702, july 2009. 4

[17] B. Cheng, M. Cao, R. Rao, A. Inani, P. Vande Voorde, W. Greene, J. Stork, Z. Yu, P. Zeitzoff, and J. Woo, "The impact of high-κ gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 46, no. 7, pp. 1537 –1544, july 1999. 4

[18] J. Zhang, J. S. Yuan, and Y. Ma, "Modeling short channel effect on high-k and stacked-gate MOSFETs," *Solid-State Electronics*, vol. 44, no. 11, pp. 2089 – 2091, 2000. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY5-41P16V5-11/2/8ae45681073f94b58f40243edefaf090 4

[19] D. Hisamoto, "FD/DG-SOI MOSFET-a viable approach to overcoming the device scaling limit," in *Electron Devices Meeting, 2001. IEDM Technical Digest. International*, 2001, pp. 19.3.1 –19.3.4. 5

[20] Y. Li and H.-M. Chou, "A Comparative Study of Electrical Characteristic on Sub-10-nm Double-Gate MOSFETs," *Nanotechnology, IEEE Transactions on*, vol. 4, no. 5, pp. 645 – 647, sept 2005. 5

[21] X. Shao and Z. Yu, "Nanoscale FinFET simulation: A quasi-3D quantum mechanical model using NEGF," *Solid-State Electronics*, vol. 49, no. 8, pp. 1435 – 1445, 2005. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY5-4GHBPJ6-1/2/d0e5bbadcc8f4ab73a96a0ee04f0b948 5

[22] J. Wang, E. Polizzi, and M. Lundstrom, "A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation,"

Journal of Applied Physics, vol. 96, no. 4, pp. 2192–2203, 2004. [Online]. Available: http://link.aip.org/link/?JAP/96/2192/1 5

[23] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," *Applied Physics Letters*, vol. 94, no. 5, pp. –, 2009. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/94/5/10.1063/1.3079411 7

[24] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat Nano*, vol. 5, no. 3, pp. 225–229, March 2010. [Online]. Available: http://dx.doi.org/10.1038/nnano.2010.15

[25] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, no. 7373, pp. 310–316, 11 2011. [Online]. Available: http://dx.doi.org/10.1038/nature10676 7

[26] H.-C. Lin, C.-I. Lin, and T.-Y. Huang, "Characteristics of n-Type Junctionless Poly-Si Thin-Film Transistors With an Ultrathin Channel," *Electron Device Letters, IEEE*, vol. 33, no. 1, pp. 53–55, Jan 2012. 7

[27] C.-W. Lee, A. N. Nazarov, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J.-P. Colinge, "Low subthreshold slope in junctionless multigate transistors," *Applied Physics Letters*, vol. 96, no. 10, pp. –, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/96/10/10.1063/1.3358131

[28] C.-J. Su, T.-I. Tsai, Y.-L. Liou, Z.-M. Lin, H.-C. Lin, and T.-S. Chao, "Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels," *Electron Device Letters, IEEE*, vol. 32, no. 4, pp. 521–523, April 2011.

[29] J. Colinge, A. Kranti, R. Yan, C. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, "Junctionless nanowire transistor (jnt): Properties and design guidelines," *Solid-State Electronics*, vol. 6566, no. 0, pp. 33 – 37, 2011, selected Papers from the {ESSDERC} 2010 Conference. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038110111002139 7

[30] J.-T. Park, J. Y. Kim, C.-W. Lee, and J.-P. Colinge, "Low-temperature conductance oscillations in junctionless nanowire transistors," *Applied Physics Letters*, vol. 97, no. 17, pp. –, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/97/17/10.1063/1.3506899 7

[31] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Akhavan, P. Razavi, and J. Colinge, "High-temperature performance of silicon junctionless mosfets," *Electron Devices, IEEE Transactions on*, vol. 57, no. 3, pp. 620–625, March 2010. 7

[32] J. Duarte, S.-J. Choi, D.-I. Moon, and Y.-K. Choi, "Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors," *Electron Device Letters, IEEE*, vol. 32, no. 6, pp. 704–706, June 2011. 7

[33] J. M. Sallese, N. Chevillon, C. Lallement, B. Iniguez, and F. Pregaldiny, "Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors," *Electron Devices, IEEE Transactions on*, vol. 58, no. 8, pp. 2628–2637, Aug 2011. 7

[34] J. Duarte, S.-J. Choi, and Y.-K. Choi, "A Full-Range Drain Current Model for Double-Gate Junctionless Transistors," *Electron Devices, IEEE Transactions on*, vol. 58, no. 12, pp. 4219–4225, Dec 2011. 7

[35] Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu, and Y. Zhou, "Surface-Potential-Based Drain Current Model for Long-Channel Junctionless Double-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 59, no. 12, pp. 3292–3298, December 2012. 7, 20, 55, 79

[36] J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," *Applied Physics Letters*, vol. 96, no. 7, pp. –, 2010. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/96/7/10.1063/1.3299014 20

[37] R. Corless, G. Gonnet, D. Hare, D. Jeffrey, and D. Knuth, "On the LambertW function," *Advances in Computational Mathematics*, vol. 5, no. 1, pp. 329–359, 1996. [Online]. Available: http://dx.doi.org/10.1007/BF02124750 27

[38] T. Banwell, "Bipolar transistor circuit analysis using the Lambert W-function," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 47, no. 11, pp. 1621–1633, Nov 2000. 27

[39] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the Junctionless Nanowire FET," *Electron Devices, IEEE Transactions on*, vol. 58, no. 9, pp. 2903–2910, 2011. 39

[40] S.-J. Choi, D.-I. Moon, S. Kim, J. Duarte, and Y.-K. Choi, "Sensitivity of Threshold Voltage to Nanowire Width Variation in Junctionless Transistors," *Electron Device Letters, IEEE*, vol. 32, no. 2, pp. 125–127, 2011. 79