ANALYTICAL 2-D MODELING OF SOI TUNNELING FIELD EFFECT TRANSISTORS

THESIS

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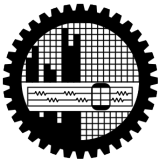

To my beloved mother Shamsun Nahar
and father Salim Chowdhury

Declaration

I hereby declare that the work presented here is my own work and this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

Signature of the Candidate

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(Nadim Chowdhury)

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Abstract

Tunneling Field Effect Transistor (TFET) with its remarkable attributes as a steep subthreshold slope device presents itself as a potential candidate to replace MOSFET beyond 14 nm node. Though a number of experimental and simulation studies on this device have been carried out over the past few years but rigorous and accurate two dimensional analytical study on this device is yet to be reported. Extensive analytical modeling is necessary to understand the physics and capture the inherent working mechanism of any device. In this work, a 2-D analytical model for Single gate Silicon On Insulator (SOI) Tunnel FET have been developed. The development of this model is based on accurate solution of 2-D Poisson's equation in the rectangular boundary conditions. The electrostatic potential and the electric field in the Oxide, Channel, and Buried Oxide region has been obtained from Poisson's equation. While solving Poisson's equation the effect of substrate and drain bias have also been taken into account. To justify the accuracy of the model, Poisson's equation with the same boundary conditions is solved in the COMSOL using Finite Element Method (FEM) and the obtained results are matched with those of modeled ones. Modeled results show excellent agreement with the FEM results, thus corroborate the accuracy of the modeled electrostatic potential and electric field. The electric field is then employed to obtain 3-D band to band generation rate in the channel region then the volume integration of this generation rate in the channel region yields the total tunnel current. The obtained tunnel current is then matched with technology computer aided (TCAD) simulation results to underpin the validity of this model. Based on the analytical model, the variation of Drain Induced Barrier Thinning (DIBT) with several device parameters viz. Channel Length, Channel Thickness, Oxide Thickness have also been studied.

Contents

List of Abbreviations

2-D	Two Dimensional
C-TFET	Carbon nanotube Tunnel Field Effect Transistor
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
DIBT	Drain Induced Barrier Thinning
DMG	Dual Material Gate
FeFET	Ferroelectric Field Effect Transistor
I-MOS	Impact Ionization Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NCTFET	Negative Capacitance Tunnel Field Effect Transistor
NEMFET	Nano-Electro-Mechanical Field Effect Transistor
S	Subthreshold Swing
SCE	Short Channel Effect
SG	Single Gate
SOI	Silicon On Insulator
TCAD	Technology Computer Aided Design
TFET	Tunneling Field Effect Transistor

List of Symbols

$\Phi(x, y)$	Electrostatic Potential
$u(x, y)$	Contribution of gate and substrate voltage in electrostatic potential
$v(x, y)$	Contribution of source and drain voltage in electrostatic potential
$E(x, y)$	Electric field intensity
$E_x(x, y)$	Horizontal component of electric field intensity
$E_y(x, y)$	Vertical component of electric field intensity
E_g	Semiconductor Band Gap
ϕ_m	Metal work function
ϕ_s	Semiconductor work function
χ_{si}	Electron affinity of silicon
L_c	Channel length
W_{ch}	Channel width.
V_G	Applied effective gate voltage
V_{DS}	Applied drain bias.
V_{SUB}	Substrate bias.
ϕ_f	Fermi potential.
V_{FB}	Flat band voltage.
q	Electron charge ($1.6X10^{-19}$ *coul*)

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1

Introduction

This chapter delineates the evolution of MOSFET as a part of integrated circuit over the last 50 years. It also draws attention towards one of the most daunting problem viz. power crisis of today's nanoelectronics and shows how this unnerving issue can be circumvented by alternative device architectures. Among these alternative architectures, TFET stands out to be the most propitious candidate for future low power applications. Brief overview of TFET, objectives and methodology of this thesis have also been presented in this chapter.

1.1 Scaling Trend of MOSFET and Power Crisis in Nanoelectronics

In logic circuits, MOSFETs operate as switch and in this regime speed and power consumptions are major concerns. To achieve higher speed and lower power consumption, the dimensions of MOSFETs have been shrunk continuously because the capacitance of logic nodes, C, decreases as the dimensions of MOSFETs decrease. A smaller capacitance results in a shorter switching time, t and a smaller switching power, P of a logic circuit. The relationship between capacitance, switching time and switching power are:

$$t = \frac{CV_D}{I_D} \tag{1.1}$$

$$P = \frac{CfV_D^2}{2} \tag{1.2}$$

Where, V_D is the supply voltage and f is the clock frequency. In fact the feature size of MOSFETs or minimum linewidth used for a MOSFET has kept shrinking at an average rate of 0.7 times about every two to three years over the past four decades, which has resulted in a line width reduction of a factor of 1/500 and a MOSFET area reduction of 1/250000 since 1970s.

Because of the downsizing of MOSFETs the number of MOSFETs in an integrated circuit was doubled every two or three years. This is well

known as Moore's Law [1] which was proposed by Gordon Moore in 1966. The downsizing of MOSFETs contributes to the performance enhancement in two ways: shorter switching time of MOSFETs and parallel processing capability. It should also be noted that with downsizing, the cost and power dissipation per MOSFET also become smaller. Clearly, the downsizing of MOSFET is critically responsible for the improvement of density, power and performance of integrated circuits.

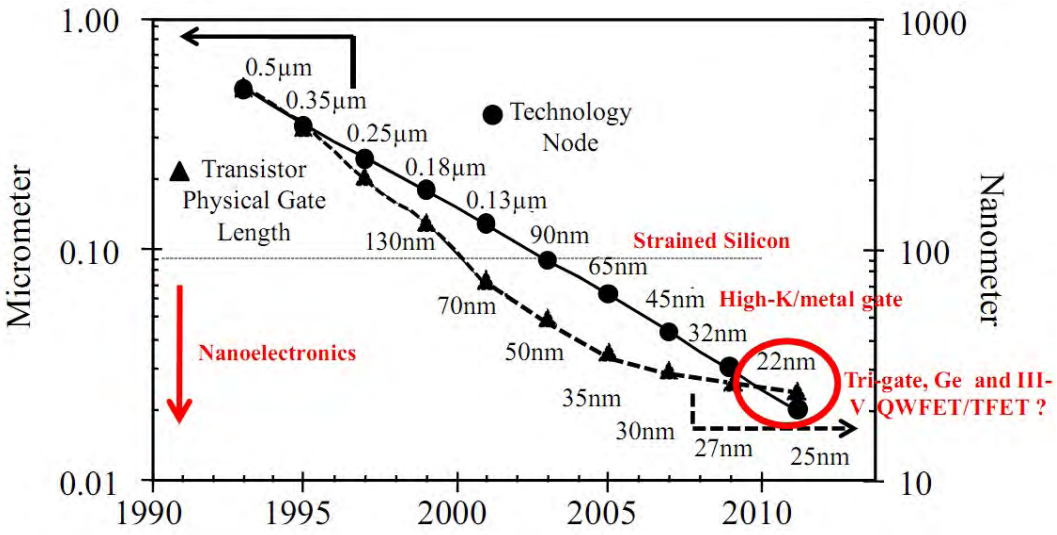

Figure 1.1: Transistor scaling over the years has followed the well known Moore's law resulting in 2X increase in transistor count every two years. With each generation of scaled technology the transistor performance has been improved. But, it's only in the last decade or so that some notable changes have been made to the traditional transistor architecture, like strained Si at 90 nm node and High-κ/metal gate at 45 nm node. Beyond the 22 nm node Tri-gate/Multi-gate devices, Ge and III-V MOSFETs/QW-FETs, TFETs and a host of other novel devices are being explored. [3]

The reduction in the feature size of MOSFET necessitates a corresponding diminution in the supply voltage at which the transistor operates. As can be verified from (1.1) and (1.2), the scaling of the supply voltage is required in order to reduce the dynamic power, P and switching time, t of the transistor. The down sizing of MOSFET attains performance enhancement through a combination of reduced capacitances, increased drive current and scaled supply voltage. The ON current per unit μm width for advanced CMOS transistor [4] is given by

$$I_{DS.SAT} = \beta C_{OX}(V_D - V_T)^{\alpha} \tag{1.3}$$

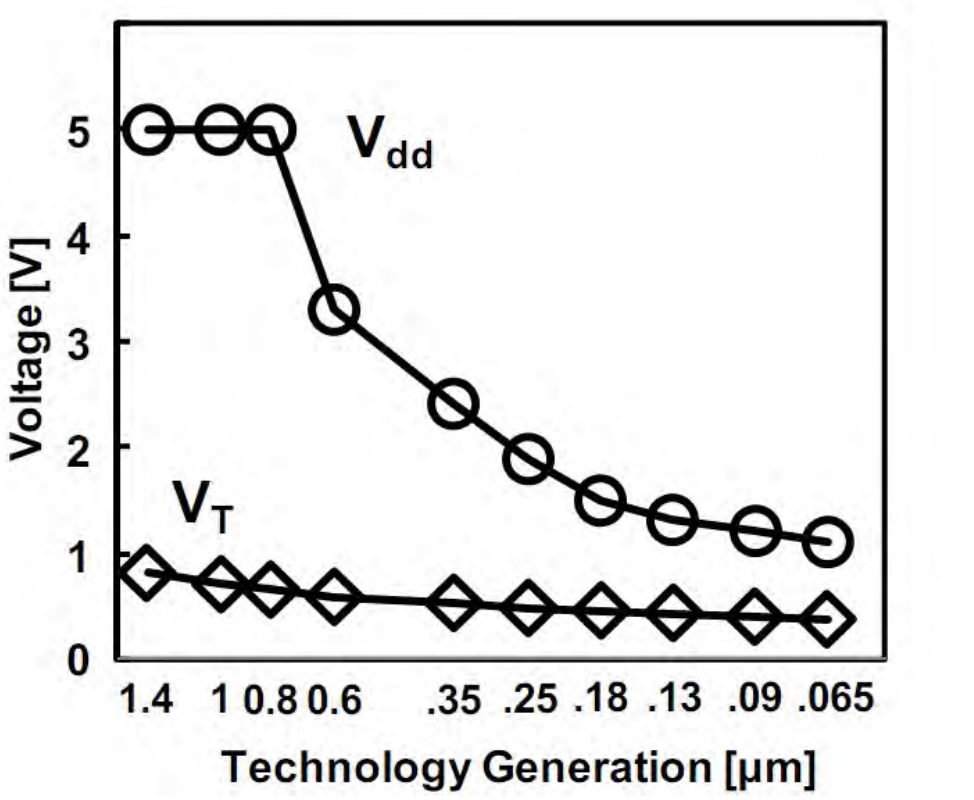

Figure 1.2: To maintain constant power density, both the supply and the threshold voltages of a CMOS integrated circuit should be reduced along with the lithographic dimension of CMOS transistors. But due to MOSFET subthreshold leakage, both V_{dd} and V_T scaling have slowed down in recent technology generations

Where, β is the proportionality constant and α is the fitting parameter which takes a value between 1 and 2 depending on the channel length and V_T is the threshold voltage. It is evident from (1.3) that in order to maintain or enhance ON current I_D, threshold voltage V_T needs to be scaled at least as rapidly as V_D. In traditional MOS transistor the subthreshold swing, S (defined as $\frac{dV_G}{d(logI_D)}$) is dictated by the diffusion of carriers from the source to the channel of the device. Therefore, the carriers at the Boltzmann tail of Fermi-Dirac distribution (*i.e.* hot/high energy carriers) take part in this OFF state transport phenomena, which inevitably puts a thermodynamic limit of $(kT/q)ln(10) = 60mV/decade$ on the subthreshold swing of the device.

In any transistor with subthreshold swing S, I_D at zero V_G is given by the following expression.

$$I_D(V_G = 0) = I_D(V_G = V_T)\exp(-V_T/S) \tag{1.4}$$

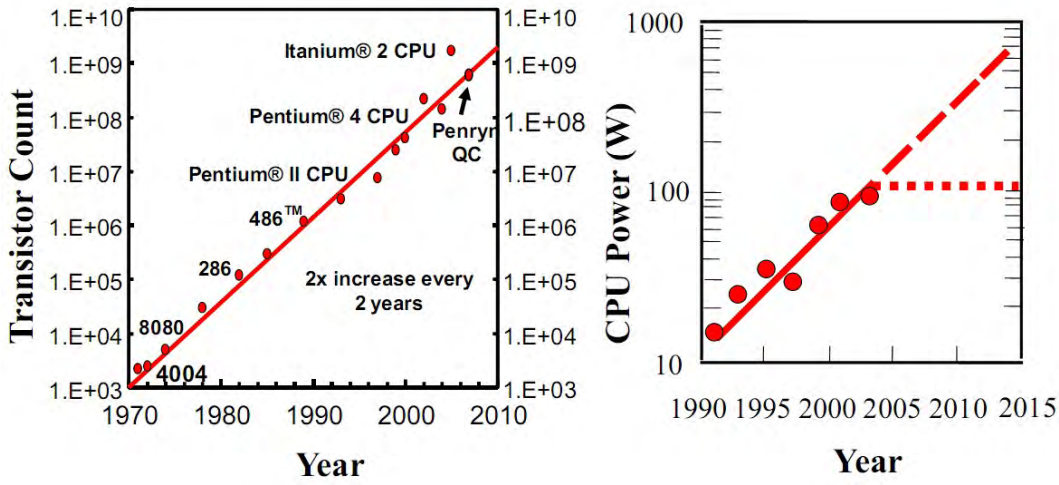

Figure 1.3: (a) Rising transistor count in Intel microprocessor chips (b) The total power dissipation in modern CPU is limited to around 100 W [5].

This current is termed as the static or subthreshold leakage current (I_{LEAK}) of the transistor since it represents the amount of current flowing in the logic gates in the quiescent state. Diminution of V_D and V_T with scaling therefore caused I_{LEAK} to increase exponentially [6]. Apart from that, the number of transistors per chip has doubled every two years [7], [8] and both these factors have caused an exponential rise in the leakage power of the chip. In modern multi-core CPU's the total power dissipation is limited to around 100 W due to thermal issues. But, more transistors are required with each generation of scaled technology to meet the ever increasing demand for higher functionality (see Fig.1.3). For 22 nm node and beyond a host of new devices and materials are being investigated, trying to address this most critical bottleneck to transistor scaling *i.e.* the power dissipation. In order to surmount this limit of $60mV/decade$ a number of super steep subthreshold slope devices has recently been proposed to the literature such as Impact Ionization MOS [6]- [9], NanoelectromechanicalFET [10]- [11], FeFET [12]- [13] and Tunnel FET [14]- [15].

1.1.1 Impact Ionization MOS

The basic device structure for the n-channel version of the I-MOS [6] is shown in Fig.1.4(a) in an silicon-on-insulator (SOI) implementation. Bulk structures work in a similar fashion. In this n-channel device, the p+ is the source and the n+ is the drain because the p-i-n diode is always reverse biased. The device is a gated p-i-n diode and works by modulation

of its channel length. At low V_G, there is no inversion layer under the gate and the effective channel length is the entire intrinsic region. The electric field under these conditions is below break- down because only a fraction of the source/drain voltage (V_{DS}), gets applied across the i-region outside the gate. Consequently,I_{LEAK} is limited by the reverse-leakage current of the p-i-n diode. As V_G is increased, an inversion layer forms under the gate and this reduces the effective channel length of the device. With higher and higher V_G , an increasing fraction of V_{DS} falls across the i-region outside the gate and therefore increases the lateral electric fields in that region. In addition, the transverse electric field also increases with increasing gate voltage. The device breaks down when the ionization integral becomes unity. Note that while the formation of the inversion layer under the gate may be limited by the normal $60mV/decade$ limit, the strong dependency of the impact ionization coefficients on the electric field and the feedback inherent in the avalanche multiplication process produce a very steep subthreshold slope in the I-MOS device. A p-i-n structure as opposed to a p-n structure is used in order to reduce the electric fields required for avalanche breakdown compared to a p-n junction. Conceptually, the I-MOS transistor may be regarded as a combination of a diode and a MOS transistor. These two elements are however not discrete and their operation is closely linked. The vertical gate induced field and the MOS surface carrier concentration affect the breakdown voltage of the diode and the surface concentration of carriers in the ON state of the MOS transistor depends on the number of carriers injected by the avalanche breakdown mechanism in the diode

1.1.2 Nano-Electro-Mechanical FET (NEMFET)

A Nano-Electro-Mechanical Field Effect Transistor [10] is essentially a MOSFET with a movable gate electrode which can be physically separated from the gate dielectric layer by an air gap (or vacuum gap).As shown in Fig.1.5(a), the gate, which is a mechanical beam anchored on both sides of the semiconducting channel, can be modeled as a simple linear spring (with a characteristic spring constant k) suspended over the semiconductor channel. The gate and the channel form a parallel-plate capacitor with an equivalent air-gap. In the off-state ($V_{gs} = 0V$), the gate is separated from the gate dielectric; the gate coupling to the channel is weak and the transistor is therefore turned off. When a positive V_{gs} is applied, the electrostatic force attracts the mechanical gate towards the gate dielectric. While the electrostatic force increases quadratically with increasing displacement, the spring restoring force, which counteracts the electrostatic force, increases only linearly with displacement. Hence, there is a critical pull-in voltage (V_{pi}) beyond which the electrostatic force is always larger

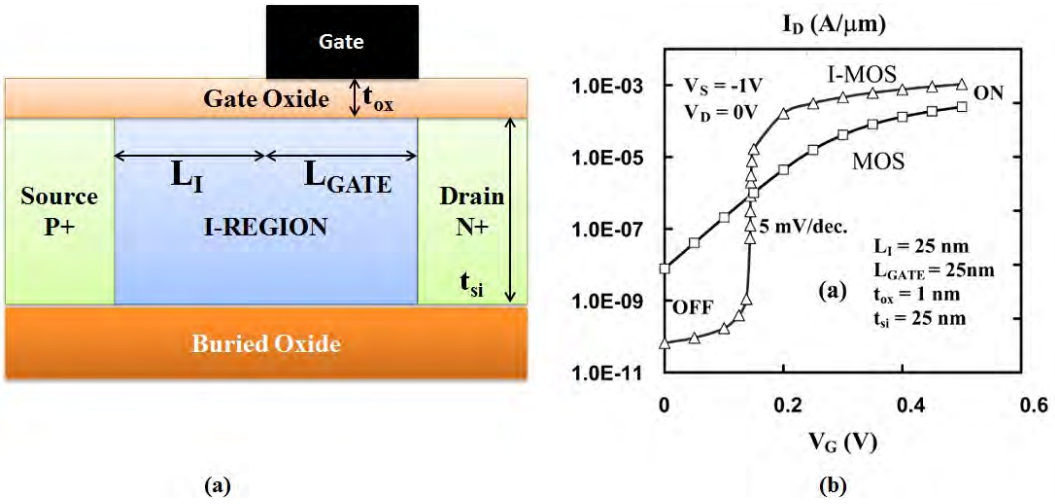

Figure 1.4: (a) Basic device structure for the n-channel SOI version of the I-MOS. This n-channel device has an overlap with the drain of the device (n+) and an offset toward the source (p+) side of the device The I-MOS uses modulation of the channel length to switch from the OFF to the ON state via avalanche breakdown.[6] (b) MEDICI simulated I_D versus V_G characteristic for a n-channel Ge I-MOS device, with $L_I = L_{GATE} = 25nm$. Simulations show that the subthreshold slope is very small ($\approx 5mV/decade$).[9]

than spring restoring force, causing the gap to close abruptly. When the gate is in contact with the gate dielectric, the gate coupling to the channel is maximized and the transistor is turned on. Taking advantage of this pull-in phenomenon, a NEMFET with perfectly abrupt switching transition ($S = 0mV/decade$) at $V_{gs} = V_{pi}$ have been utilized for logic, memory and resonator applications

1.1.3 Negative Capacitance Field Effect Transistor (NCFET)

Salahuddin and Datta [12], [13] showed that by replacing the standard insulator with a ferroelectric insulator (see Fig. 1.6(a))of the right thickness it should be possible to implement a step-up voltage transformer that will amplify the gate voltage thus leading to values of S lower than $60mV/decade$ and enabling low voltage/low power operation. The voltage transformer action can be understood intuitively as the result of an effective negative capacitance provided by the ferroelectric capacitor which arises from an internal positive feedback that in principle could be obtained from other microscopic mechanisms as well. Unlike other methods to reduce S, this involves no change in the basic physics of the FET and thus does not affect its current drive or impose other restrictions. The basic idea of how does

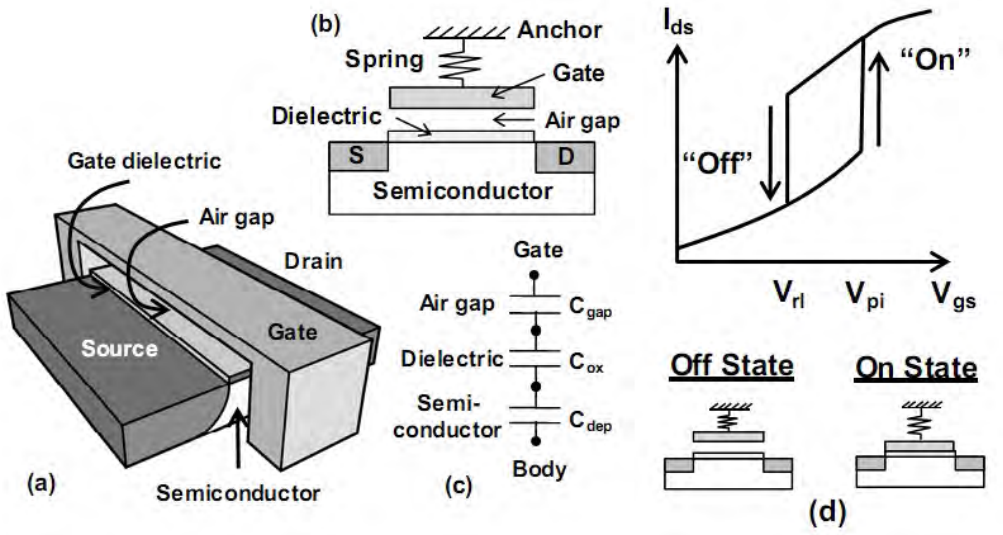

Figure 1.5: (a) Schematic diagrams of a Nano-Electro-Mechanical Field Effect Transistor (NEMFET). (b,c) Simple lumped-parameter model for a NEMFET.[11] (d) The abrupt pull-in/ release of the gate electrode provide for perfectly abrupt ON/OFF transitions.

NCFET obtain sub $60mV/decade$ subthreshold swing can be understood from the following analysis. The subthreshold swing of a conventional MOSFET is defined as follows.

$$S = \frac{dV_G}{dlog10(I_D)} = \frac{dV_G}{d\Psi_G}\frac{d\Psi_G}{dlog10(I_D)} \tag{1.5}$$

Standard FET analysis shows that the second term $\frac{d\Psi_G}{dlog10(I_D)}$ relating the change in the current to the change in the surface potential in the channel cannot be any lower than $60mV/decade$ at room temperature. Since V_G and Ψ_G are related by a capacitive voltage divider as shown in Fig. 1.6(b). It is apparent that the first term $\frac{dV_G}{d\Psi_G}$ (often called the body factor 'm') given by

$$\frac{dV_G}{d\Psi_G} = 1 + \frac{C_s}{C_{ins}} \tag{1.6}$$

must exceed one, thus putting a lower limit of $60mV/decade$ (corresponding to m = 1) on the subthreshold slope S. Even high-κ insulators with phenomenally large values of C_{ins} can only reduce the body factor 'm' so as to approach one, but cannot make it any smaller. But, if conventional insulator is replaced with a ferroelectric insulator, having a P-E (polarization versus electric field) characteristic of the type shown in Fig. 1.6(c), it is

possible to obtain $\frac{dV_G}{d\Psi_G} < 1$ and hence a value of S lower than $60mV/decade$. This can be understood from 1.6 by noting that the ferroelectric capacitor is effectively a negative one, since the slope of P versus E (which is a scaled version of Q versus V) around the origin is negative. Ordinarily this negative slope segment is unstable and not directly observed in experiments which exhibit hysteretic jumps in the polarization. But if the ferroelectric capacitor is placed in series with a normal capacitor, the negative capacitance segment can be effectively stabilized making it possible for the channel potential Ψ_G on an internal node to change more than the voltage V_G applied externally, thus providing a voltage amplifier or more correctly, a step-up voltage transformer.

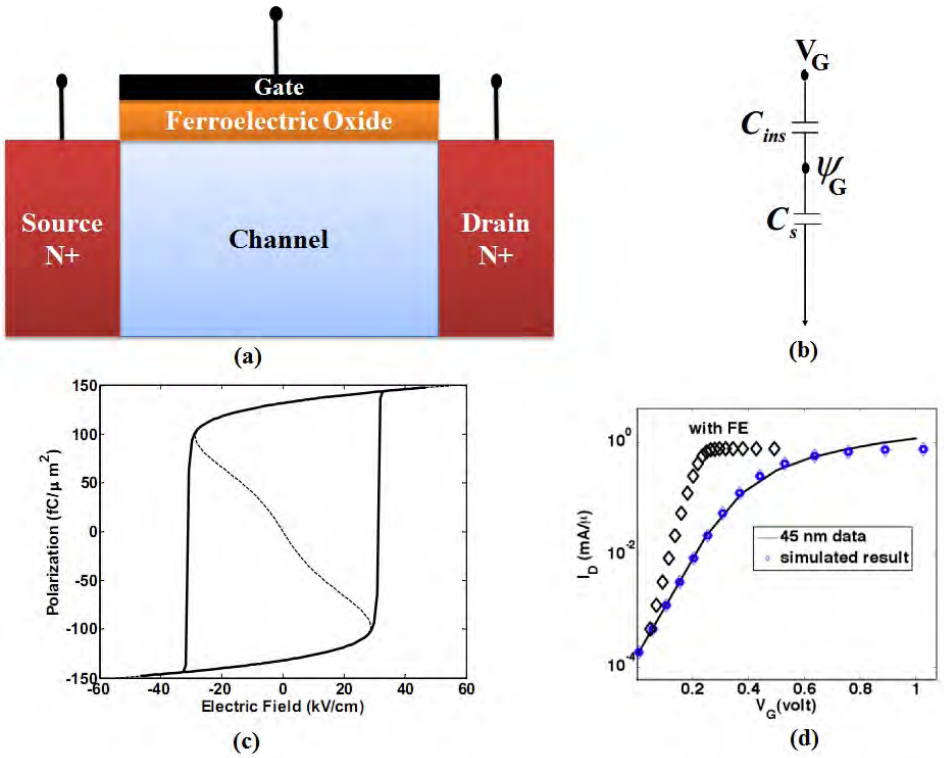

Figure 1.6: (a) Schematic diagram of a Negative Capacitance Field Effect Transistor (NCFET). (b) an equivalent circuit for the division of the gate voltage between the insulator capacitance and the semiconductor capacitance (that comprises of the delpletion, channel to source and channel to drain capacitances).(c) Polarization versus electric field for a typical ferroelectric material (d)Current vs. Gate Voltage with (diamond) and without ferroelectric. The subthreshold swing improves significantly.

1.1.4 Tunneling Field Effect Transistor(TFET)

Among all the alternative super steep subthreshold slope transistor designs, the tunnel field effect transistor (TFET) [14] shows the most promise due to its relative simplicity and resemblance to the conventional MOSFET. Electrons and holes obey the laws of quantum mechanics, which means they have a fuzzy, uncertain size. When an energy barrier has a thickness below about 10 nanometers, there is a small but nonzero probability that an electron that starts on one side of the barrier will appear on the other.In the TFET, this probability is boosted by applying a voltage to the transistor gate. This causes the conduction band in the source and the valence band in the channel to overlap, opening up a tunneling window. Note that in a TFET, the electrons tunnel between conduction and valence bands as they move into the channel. This is in contrast to what happens in a MOSFET, in which electrons or holes travel primarily in either one band or the other all the way from source to channel to drain. Because the tunneling mechanism isn't controlled by the flow of carriers over a barrier, TFETs should be able to switch with a much smaller voltage swing than that required in a MOSFET.Therefore, TFET utilizes band-to-band tunneling (BTBT) current to achieve a more abrupt ON-OFF transition than what is achievable through thermionic emission. Fig.1.7 shows the energy band diagram of the TFET in ON and OFF states. In the OFF state, the wide energy barrier prohibits quantum tunneling between the source and channel regions. When a large V_G is applied, the energy barrier narrows, and allowed energy states in the channel conduction band align with allowed energy states in the source valence band, so that electrons can tunnel from the source to the channel. Since the TFET utilizes a different source injection mechanism from the MOSFET, it can potentially achieve lower S values, which has already been experimentally demonstrated [15]. Note, however, that a TFET achieves $S < 60mV/decade$ only at low current levels and that S increases as I_{DS} increases. Consequently, at high V_D($1V$) values, a silicon TFET has a significantly lower on-state current I_{ON}($1\mu A/\mu m$ *at* $1V$) than a silicon MOSFET ($1mA/\mu m$ *at* $1V$). This remains a principal challenge for TFET designers.

1.2 Objectives

Device modeling refers in general to a suite of models and methods describing carrier transport in materials. Models range from the simple drift diffusion, which solves Poisson and continuity equations, to more complex and CPU intensive ones as the energy balance, which solve some higher moment simplification of the Boltzmann equation. In addition, the complex physics of today's devices mandates at times the usage of Monte Carlo

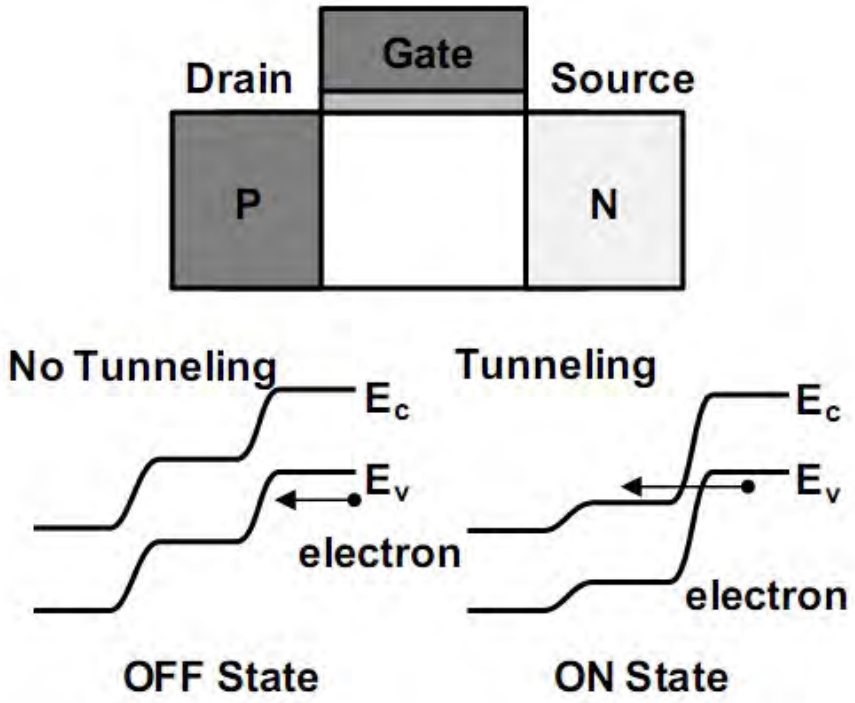

Figure 1.7: Schematic diagram of a tunneling field effect transistor and its energy band diagram in the OFF and ON states (n-channel operation).

codes, which stochastically solve the Boltzmann equation, and the usage of SchrÃűdinger solvers that account for quantum effects. The choice of the appropriate model depends on the problem and the level of details required and it is therefore application dependent. Despite the significant advances of recent years in both numerics and physics, continuous development is required to meet the increasingly challenging industry needs for device exploration and optimization. Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount.

For the fast developing devices and circuits, reliable and predictive analytical models are required. Numerical simulations are not direct for the design of circuits involving many devices interacting with each other and with other circuit elements. Physically based analytical models that are compatible with modern Computer aided design (CAD) tools are more directly applicable for parametric optimization and extraction process than the numerical device simulation processes.

A number of studies based on TCAD simulations [16]- [17] have been performed to anticipate the device performance and to optimize the various device parameters for better performance. However, analytical treatment of the device is necessary to capture better physical insight. But a limited number of 1-D and 2-D modeling [18]-[20] works have been reported to the literature, till date. The purpose of this work is to propose a more accurate 2-D analytical model for the SOI TFET.
The objectives of this work are:

1. To obtain analytical expressions for 2-D electrostatic potential and electric field intensity of the device.
2. To verify the developed potential and electric field model by 2-D COMSOL Multiphysics 4.3b simulation.
3. To evaluate current-voltage characteristics.
4. To verify the proposed model by TCAD simulations.
5. To study the short channel effects based on the analytical model

1.3 Methodology

We will analytically solve 2-D Poisson's equation in the channel, oxide and buried oxide region with appropriate boundary conditions, in order to obtain analytical expression of electrostatic potential and electric field intensity. Then we will employ L. V. Keldysh and E. O. Kane's theory [21]-[22] to evaluate 3-D band to band generation rate and tunneling current. In order to verify the proposed model we will develop a 2-D device simulator in COMSOL Multiphysics 4.3b. TCAD simulation of the same device, incorporating non-local band to band tunneling, will also be performed to calibrate the material based constants of the proposed model and to further verify the proposed model. We will study Short Channel Effects (SCEs) viz. DIBT (Drain Induced Barrier Thinning) and Threshold Voltage roll off of the device and compare them with those of conventional MOSFET.

2

Tunnel Field Effect Transistor

This chapter illustrates the physics of tunneling field effect transistor and explains how it overcomes the fundamental limit of 60 $mV/decade$, commonly termed as Boltzmann Tyranny. The impact of different material and architectural parameters of the device on tunnel current has also been discussed in this chapter.It also reviews various architectural and parameter variation of Tunnel FET to boost up the over all performance of the device.

2.1 Physics of Tunnel FET

Unlike MOSFETs, in which charge carriers are thermally injected over an energy barrier, the fundamental transport mechanism in a Tunnel FET is interband tunneling, whereby charge carriers transfer from one energy band into another at a heavily doped (p+-n+) junction. This tunneling mechanism was first identified by Clarence Zener [23] in 1934, to explain dielectric breakdown, a precipitous rise in current as the field strength is increased.

In a Tunnel FET, band to band tunneling can be switched ON and OFF suddenly by altering the band bending in the channel region by means of the applied gate voltage. This controlling mechanism can be materialized in a reverse-biased p+-i-n+ structure (Fig. 2.1a). In principle, the Tunnel FET is an ambipolar device, showing p-type behavior with dominant hole conduction and n-type behavior with dominant electron conduction. However, by incorporating an asymmetry in the doping level or profile, or by restricting the movement of one type of charge carrier using heterostructures, the tunneling barrier at the drain side can be made thicker to eradicate the ambipolar behavior [24], [25]. The aforementioned asymmetry also yields a very low OFF current [26]. In the TunnelFET OFF state (dashed blue line in Fig.2.1b), the valence band edge of the channel is located below the conduction band edge of the source, so that band to band tunneling is suppressed, leading to very small Tunnel FET OFF current that is dictated by the reverse-biased p-i-n diode. Applying a negative gate voltage (solid red curve in Fig. 2.1b) pulls the energy bands up. A conductive channel opens

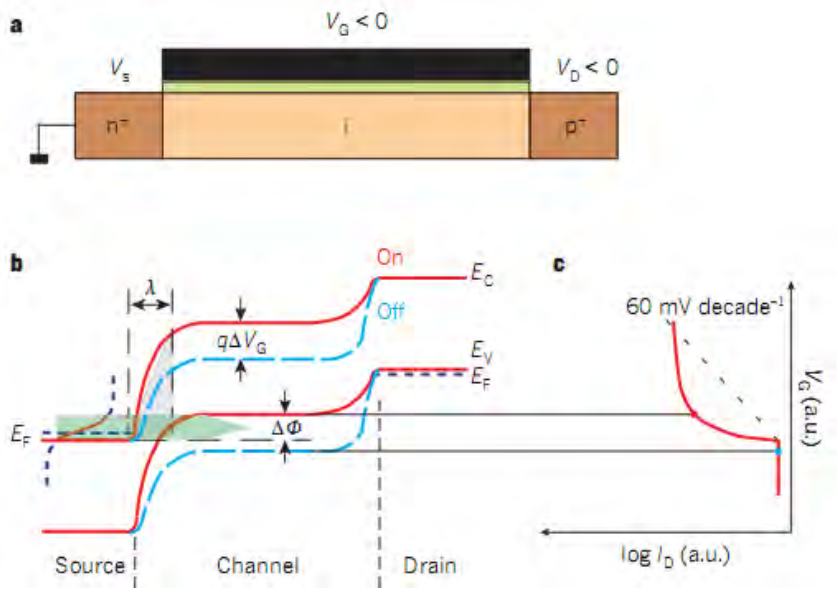

Figure 2.1: (a) Schematic cross-section of p-type TFET. (b) Schematic energy band profile for the off state (dashed blue lines) and the on state (red lines) in a p-type TFET. (c) TFET has a slope that is not linear on a logarithmic scale, which can be explained by the complex dependency of the tunnel current on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions.

as soon as the channel valence band has been lifted above the source conduction band edge because carriers can now tunnel into empty states of the channel. Because only carriers in the energy window $\Delta\Phi$ can tunnel into the channel, the energy distribution of carriers from the source is limited; the high-energy part of the source Fermi distribution is effectively filtered out [27], as shown in Fig. 2.1b. Thus the electronic system is effectively 'cooled down', acting as a conventional MOSFET at a lower temperature. This energy filtering mechanism makes it possible to achieve an S of below 60 mV per decade (Fig. 2.1c). However, the channel valence band can be lifted by a small change in gate voltage, and the tunneling width can effectively be reduced by the gate voltage [28]-[14]. As a consequence of the BTBT mechanism, S in a TunnelFET is not constant, but depends on the applied gate-source bias, as indicated in Fig. 2.1c, increasing with the gate-to-source bias. The key to the better voltage scaling of a TFET than a MOSFET is that S remains below 60 mV per decade over several orders of magnitude of drain current. One challenge in TFETs is to realize high on currents because I_{ON} critically depends on the transmission probability, T_{WKB}, of the interband tunneling barrier. This barrier can be approximated by a triangular potential, as indicated by the Grey shading in Fig.

2.1b, so T can be calculated using the Wentzel-Kramer-Brillouin (WKB) approximation [29], [26].

$$T_{WKB} \approx \exp(-\frac{4\lambda\sqrt{2m^* E_g^3}}{3q\hbar(E_g + \Delta\Phi)}) \tag{2.1}$$

where m_* is the effective mass and E_g is the bandgap. Here, λ is the screening tunneling length and describes the spatial extent of the transition region at the source-channel interface (Fig. 2.1b); it depends on the specific device geometry. In a TFET, at constant drain voltage, V_D, the V_G increase reduces λ and increases the energetic difference between the conduction band in the source and the valence band in the channel ($\Delta\Phi$), so that in a first approximation the drain current is a super-exponential function [37] of V_G. As a result, in contrast to the MOSFET, the point subthreshold swing of the TFET is no longer a constant but strongly depends on V_G. The smallest subthermal values occur at the lowest gate voltages. A high on current requires a high transparency of the tunneling barrier, thus maximizing T_{WKB}, which in the best case should be unity. Equation 3.1 suggests optimized design approaches to boost the on current. Luisier and Klimeck [38] found that the WKB approximation works properly in direct bandgap semiconductors, such as InAs (if one single imaginary path connecting the valence band and the conduction band dominates the tunneling process), but has limited accuracy for Si and Ge structures or when quantum effects and phonon-assisted tunneling become dominant.

2.2 Performance Optimization of TFETs

The objectives of performance optimization of TFETs are:

1. To achieve highest possible I_{ON}
2. To achieve the lowest possible S_{avg} over many orders of magnitude of drain current.
3. To attain the lowest possible I_{OFF}

In order to prove itself as a potential candidate for replacing CMOS transistors, the target parameters for TFETs are:

1. I_{ON} in the range of hundreds of miliamperes.
2. S_{avg} far below 60 $mV/decade$ for five decades of drain current.
3. $\frac{I_{ON}}{I_{OFF}} \geq 10^5$
4. Supply voltage $V_{DD} < 0.5$V.

Since, for TFET S_{avg} decreases with the V_G, TFETs are naturally optimized for low voltage operation. In order to realize high tunneling current

with steep slope the transmission probability of the source tunneling barrier should become close to unity for a small change in V_G. The WKB approximation suggests that the band gap (E_g), the effective carrier mass (m^*) and the screening tunneling length (λ) should be minimized for high barrier transparency. Whereas E_g and m^* depends entirely on material system, λ is strongly influenced by several parameters, such as device geometry, dimensions, doping profiles and gate capacitance. A small λ results in a strong modulation of channel band profile by the gate voltage. This requires a high-k gate dielectric with as low an equivalent oxide thickness as possible. Furthermore, the body thickness of the channel should be minimized , showing in the best case one-dimensional electronic transport behavior. The abruptness of the doping profile at the tunnel junction is also important. To minimize tunneling barrier, the high source doping level must fall off to the intrinsic channel in as short a width as possible. This requires a change in the doping concentration of about 4-5 orders of magnitude within a distance of only a few nano-meters. Increasing the source doping reduces λ and may lead to a slightly smaller energy barrier at the tunnel junction because of bandgap narrowing. However, the energy filtering effect described in the previous section becomes effective only if the Fermi energy in the source is not too large [30].

TFETs do not follow the same scaling rules as MOSFETs, in which many parameters must be scaled simultaneously to keep the same electric field throughout the device [31]. In a TFET, the high electric fields exist only at the junctions. The current is determined by the screening tunneling length, so that the length of the intrinsic region has little effect on the device characteristics, as long as the length is above some critical length, L_{crit} (20 nm for silicon TFETs [31]), at which p-i-n leakage becomes predominant. Experimental results [32] confirmed the lack of dependence of I_{ON} on TFET length.

Device optimization should apply to both n- and p-type TFETs simultaneously, to offer a complementary TFET (C-TFET) technology for logic circuits. In a heterostructure TFET, the materials are chosen such that the source material has a small bandgap, so that the width of the energy barrier at the source junction is reduced in the on state, whereas the drain material has a large bandgap, which creates the largest possible energy barrier width at the drain side in the off state to keep the off current low. The way in which the bands line up with each other at the heterojunction is also crucial [33] , [34]. Knoch [35] suggested that although a broken line-up yields the best I_{ON}, only $S \geq 60mV$ per decade is obtained; therefore, a combination of steep S and high I_{ON} can been achieved with moderate doping and a staggered band lineup ($S = 33mV$ per decade and an intrinsic cutoff fre-

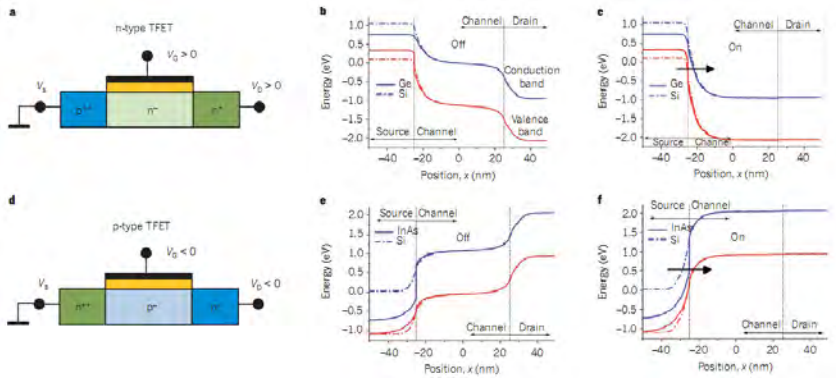

Figure 2.2: Band diagrams of heterostructure C-TFETs. C-TFET device n-type (a-c) and p-type (d-f) architectures (a, b) and related band diagrams in the off (b, e) and on (c, f) state for two major implementations: all-silicon n- and p-type devices (dashed lines) and heterostructures with a Ge source and Si channel for the n-type switch and an InAs source and silicon channel for the p-type switch (solid lines). Band diagrams correspond to device architectures with a channel length of 50 nm and a high- κ dielectric thickness of 3 nm. The graphs show the conduction band (blue) and the valence band (red)

quency of 4.74 THz) [36]. Koswatta et al. [37] included electron-phonon scattering in the transport model and found the best TFET performance for a broken-gap heterojunction.

Another optimization criterion is maximizing the gate modulation of the tunneling barrier width by an appropriate alignment of the tunnelling path with the direction of the electric field modulated by the gate. By overlapping the gate with the tunneling region, or designing a source region covered with an epitaxial intrinsic channel layer under the top gate, I_{ON} can be improved by a factor of more than 10 and a low S_{avg} can be obtained [38]- [39].

The effect of a staggered bandgap at the TFET source-to-channel junction as a technology booster is shown in Fig. 2.2. The aim is to find a solution for an optimized C-TFET. The simulated devices have a silicon channel length of 50 nm, a 20 nm thick film and asymmetric doping to avoid ambipolarity. The cross-section and bands in the off and the on state of the n-type TFET are shown in Fig. 2.2 a-c. Changing the source material from Si to Ge considerably improves λ and $\Delta\Phi$ at the same applied V_G in the on state. A similar band-engineering optimization performed for the p-type device with an InAs source is shown in Fig. 2.2 (d-f). The corresponding reduction of the screening tunnelling length and its dependence on the V_G when the source bandgap is changed is depicted in Fig. 2.3.

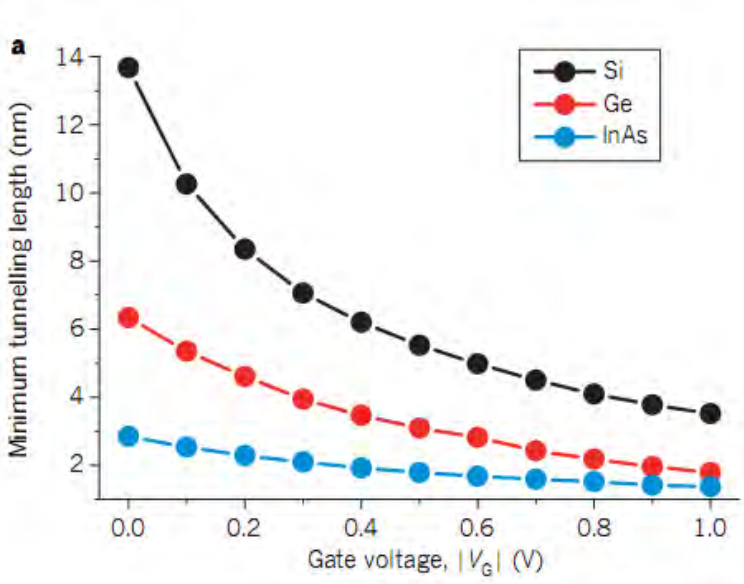

Figure 2.3: Modulation of the minimum screening tunnelling length with the applied gate voltage in all-silicon (black), Ge-source (red) and InAs-source (blue) TFETs, showing the beneficial effect of a higher tunnelling rate due to the shorter tunnelling length in a heterostructure TFET with a low bandgap source material compared with silicon. By contrast, a higher ratio between

2.3 Silicon-TFET

TFETs offer the potential for a low off current and a small S, but they generally have a lower on current than conventional MOSFETs, so a smart design strategy could achieve a small S_{avg} and a high I_{ON} without degrading I_{OFF}. The major technology boosters for all-silicon TFETs include [40], [41] the use of a high-k gate dielectric, a more abrupt doping profile at the tunnel junction, a thinner body, higher source doping, a double gate, a gate oxide aligned with the intrinsic region, and a shorter intrinsic region (and gate) length.

2.4 III-V TFET

A further strategy to improve I_{ON} and S is to use low-bandgap and low-effective-mass materials and band engineering to increase BTBT. For this, group III-V materials are very attractive as they can provide small tunnelling mass and allow different band-edge alignments.Simulation showed that by reducing only the bandgap of the TFET material from Si to InAs or InSb, the I_{ON} increases by several orders of magnitude and can be reached at lower electric fields [26]. Recent experimental results for InGaAs TFETs

indicate that a higher I_{ON} at a lower V_G than with Si TFETs seems possible [42], [43]. The first InGaAs TFET by Mookerjea et al. [42] achieved an on current of $20\mu A/\mu m$ with an S of 250 mV per decade, whereas Zhao et al. [43] improved I_{ON} to $50\mu A/\mu m$ with an S of around 90 mV per decade, which is the best local swing achieved so far for III-V-based TFETs but is still above the thermal limit of MOSFETs. The degraded S is attributed to parasitic tunnelling mechanisms involving traps in the source tunnel junction [44]. The effective bandgap for tunnelling can be decreased even further by using heterostructures. Although there is not yet full agreement on whether a staggered or a broken gap alignment works best, all theoretical studies predict that the TFET performance can be significantly enhanced compared with homojunctions [34]- [36], [45]. The first experimental implementations of III-V heterojunction TFETs have only recently been demonstrated [46]. To reduce the tunnelling barrier, InAs and GaAsSb were chosen for the source, with AlGaSb and InGaAs for the channel. Another reason for selecting these materials is that they allow lattice-matched growth, and thus the use of conventional III-V growth and processing technologies.

For the C-TFET technology, the combination of an InAs source with a Si drain and channel yields the best on-state performance for the p-TFET [34]. However, InAs and Si possess a lattice mismatch of about 11%, which results in highly defective material growth and prevents integration onto Si in a conventional approach. This challenge can be met by using grown nanowires. They are attractive materials as they can be grown epitaxially via metal-organic chemical vapour deposition directly on Si(111) (ref. [47]).

Moreover, the vertical nanowire provides an optimal geometry for minimizing the screening tunnelling length, λ, by using a 'gate-all-around' (GAA) architecture, in which the gate is wrapped around the cylindrical nanowire channel to provide the best electrostatic control. Simulations have shown that λ is reduced three- to fourfold when using the GAA nanowire architecture compared with using a single-gate device with a channel thickness or diameter of 10 nm [48]. The cross-section of a recently fabricated vertical n-i-p InAs-Si-Si nanowire heterojunction TFET with InAs as a low-bandgap source [49] is shown in Fig. 2.4 b. The single-nanowire TFET exhibits switching operation under reverse-bias conditions with an S of $220mV$ per decade and a drive current of $0.4\mu A/\mu m$ (see Fig. 2.4 d). This first InAs-source, Si-channel TFET implementation needs further optimization. It is anticipated that the drive current can be improved by introducing n-type doping in the InAs wire, by scaling the equivalent oxide thickness, and by reducing the contact resistance.

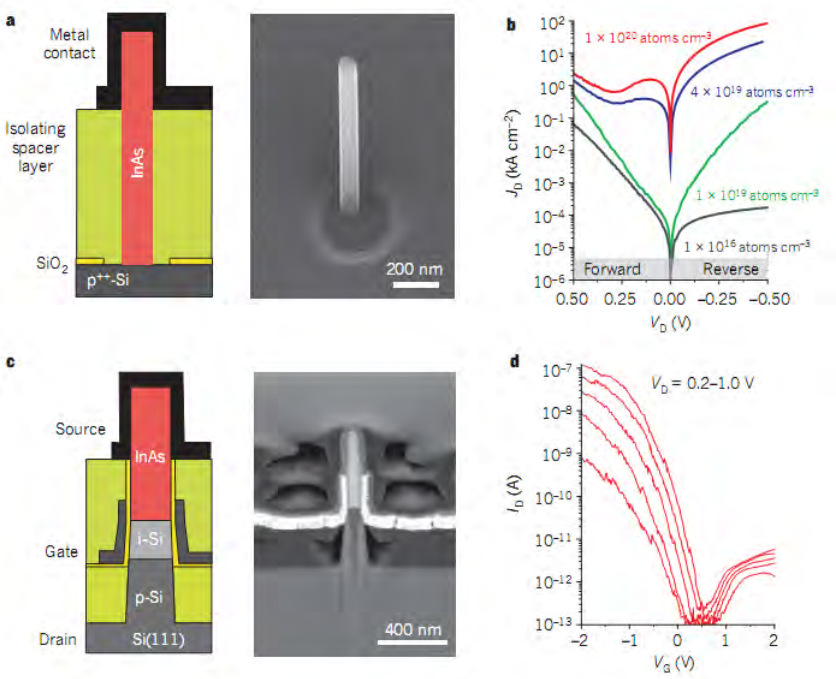

Figure 2.4: InAs-Si heterojunction diodes and TFETs for improved performance. (a)Left, schematic cross-section of an InAs-Si heterostructure nanowire diode. Right, scanning electron micrograph of an InAs nanowire grown epitaxially on Si. (b) Current density-voltage (J_D-V_G) characteristics of Si-InAs heterojunction single-nanowire tunnel diodes. The high tunnel current densities required for TFETs are achieved for high doping levels. Different colours refer to different doping densities. (c) Left, schematic cross-section of a vertical InAs-Si heterostructure nanowire TFET. Right, scanning electron micrograph showing a cross-section of the fabricated TFET. The InAs nanowire has a diameter of 100 nm, and the undoped Si channel on the p-type substrate is 150 nm long. (d) Transfer characteristics, I_D-V_G, for various source-drain biases of the TFET shown in c.

2.5 Fe-TFET

Ionescu ei. el. [50] presented the fabrication and electrical characterization of Ferroelectric-Tunnel FETs (Fe-TFETs). The main focus of their work was to combine the low subthreshold power of band to band tunneling devices with the retention characteristics of Fe gate stacks, offering some interesting features for future One-Transistor (1T) memory cells. They have reported I_{ON}/I_{OFF} larger than 10^5 and I_{OFF} on the order of $100fA/\mu m$ in micro-meter p-type Fe-TFETs fabricated on ultra-thin film (fully depleted silicon on insulator) with $SiO_2/Al_2O_3/PVDF$ as gate stack processed at low temperature (see Fig. 2.5). No evidence of negative capacitance has been found in this experimental work but hysteric characteristics of TFET with Fe gate stack exhibiting a retention time on the order of few minutes at room temperature, has been reported in this work.

2.6 Negative Capacitance TFET

Whereas the objective of Ref. [50] was to investigate the hysteric behavior of TFET with Fe-gate stack , Nadim et. el.[51] proposed and theoretically investigated the application of Ferroelectric oxide operating in the negative capacitance zone, on TFET as complementary gate dielectric (see Fig. 2.7 (a)). Using simple theoretical methods they have demonstrated that NCTFET effectively combines two different method of lowering subthreshold swing (SS) for a transistor, garnering a further lowered one compared to conventional TFET. The $I-V$ model for NCTFET proposed in this work is based on the work of Verhulst et. el. [18] and Ref. [12]. In principle, NCTFET can perform better than conventional TFET in terms of lower subthreshold swing and higher ON current.(see Fig. 2.7 (b))

2.7 Dual Material Gate TFET

Saurabh and Kumar [52] propose the application of a dual material gate (DMG) in a tunnel field-effect transistor (TFET)(see Fig. 2.8) to simultaneously optimize the ON-current, the OFF-current, and the threshold voltage and also improve the average subthreshold slope, the nature of the output characteristics, and immunity against the drain-induced barrier lowering effects.

As has been discussed previously, a conventional DGTFET suffers from an unacceptably low I_{ON}. The DMG technique alone cannot bring the I_{ON} of a DGTFET to that of the MOSFET levels. It has also been shown that, when the channel is composed of a smaller band-gap material, the I_{ON} in a TFET improves dramatically [53] - [55]. In [53], the strained DGT-

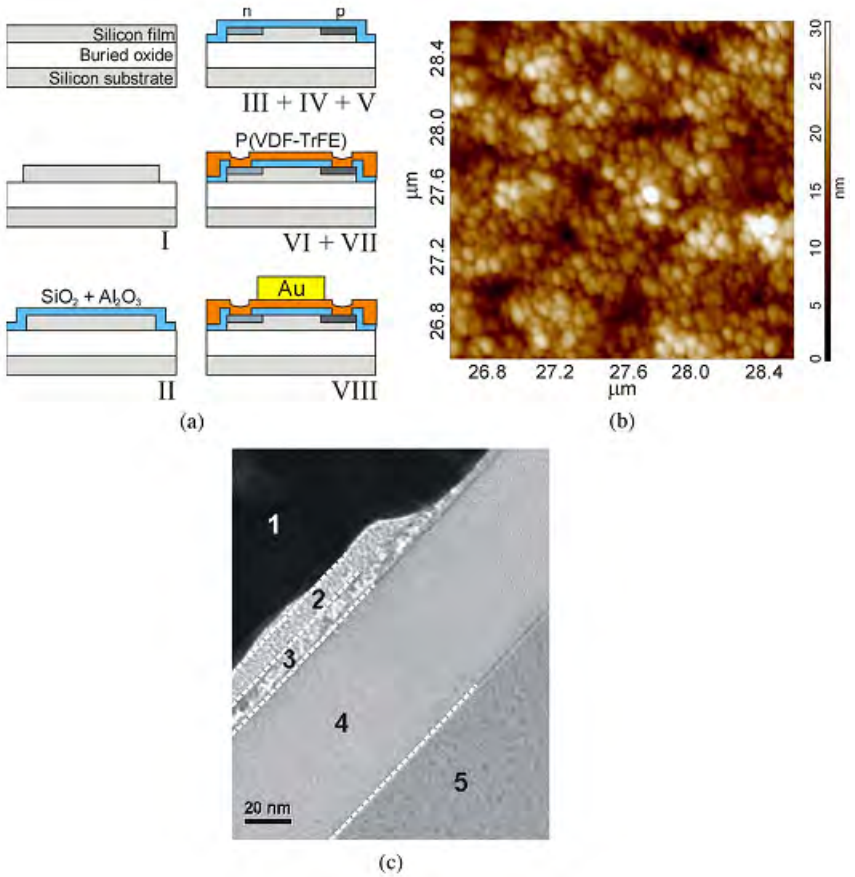

Figure 2.5: (a) Process flow for the fabrication of the Fe-TFET on a SOI substrate (b) AFM image of the surface of the gate on a $2\mu mX2\mu m$ area, showing the P(VDF-TrFE) roughness of the order of 30 nm (c) High resolution TEM micrograph showing the cross section of the fabricated gate stack

FET (SDGTFET) has been demonstrated to improve the I_{ON} and the subthreshold swing. SDGTFET is structurally the same as a DGTFET, except that the silicon body is composed of SiGe-free sSOI. The strain in an SDGTFET is controlled by the Ge mole-fraction (x) that has been used to fabricate the sSOI. Since the introduction of strain decreases the band gap of the silicon, an SDGTFET shows a remarkably improved device performance. Ref.[52] demonstrate the application of the DMG technique in an SDGTFET with a high-k gate dielectric to not only achieve an improved I_{ON} and SS_{AVG} but also improve the overall performance of the device. It is also demonstrated that, using the additional handle of the DMG, the scalability of the TFET can be extended below 20-nm channel lengths. Fig. 2.9 shows the Transfer-characteristics of DMG-SDGTFET with optimized device parameters as demonstrated in Ref.[52]

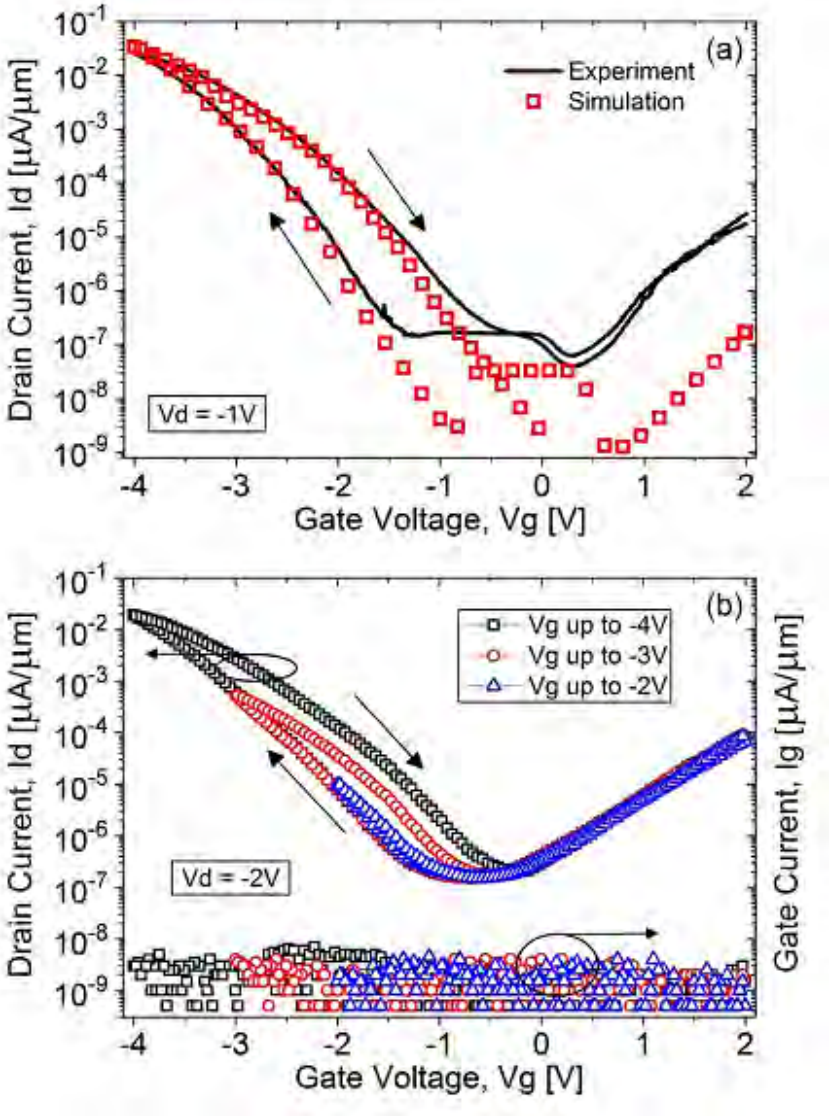

Figure 2.6: (a) Experimental and simulated Id-Vg of a Fe-TFET ($L = 5\mu m; W = 20\mu m$) showing a hysteresis of about 1 V. Numerical simulations are in good agreement with the experimental data, both in terms of ON-CURRENT and subthreshold slope behavior. (b) Experimental hysteretic Id-Vg behavior for another p-type Fe-TFET with $L = 5\mu m$ and $W = 20\mu m$. The hysteresis is larger when Vg is swept to higher values since the polarization in the Fe layer increases.

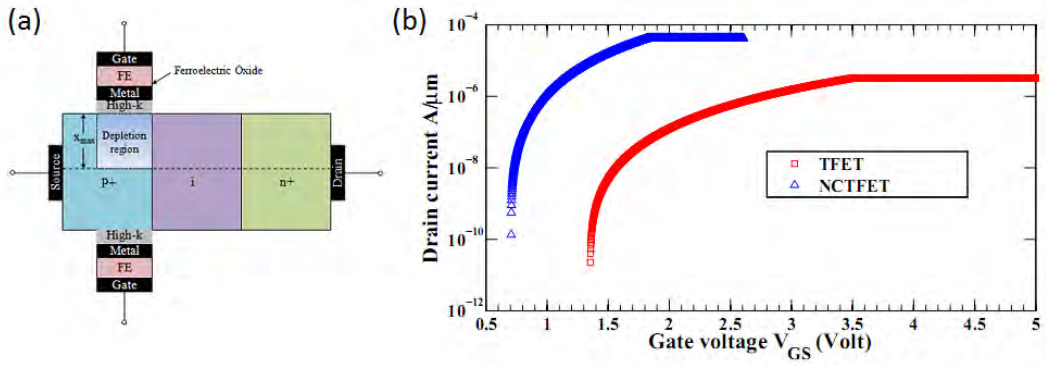

Figure 2.7: (a) Schematic cross-sectional view of the NCTFET (b) I_{DS}-V_{GS} characteristics of NCTFET and conventional TFET

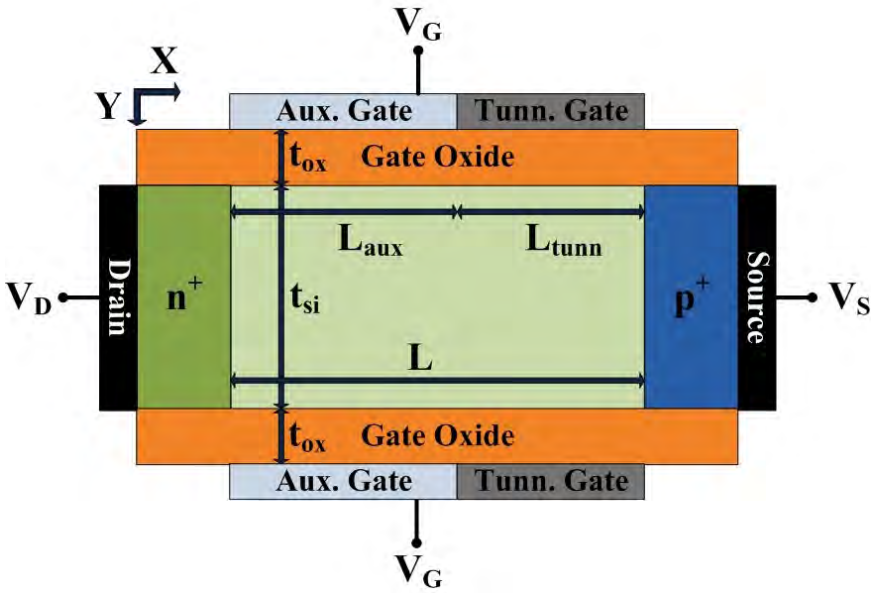

Figure 2.8: Schematic cross-sectional view of the DMG-DGTFET

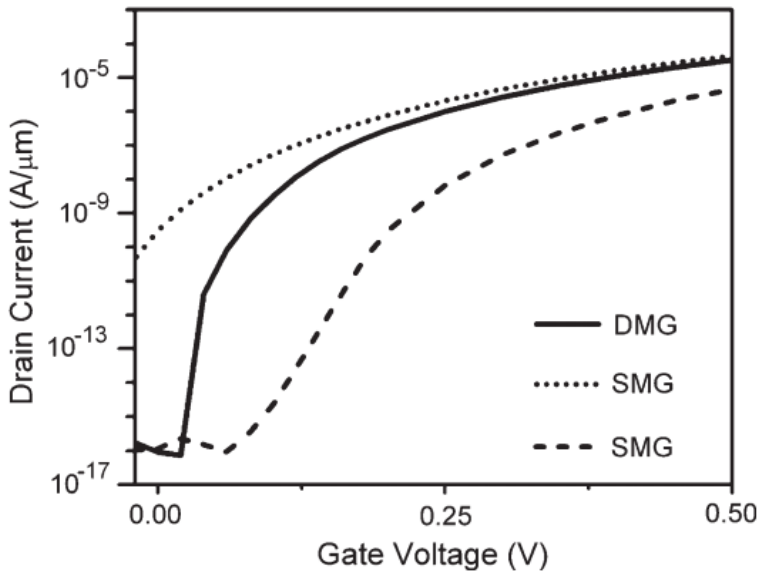

Figure 2.9: Transfer characteristics of the DMG-SDGTFET ($\Phi_{tunnel} = 4.5$ eV, $\Phi_{aux} = 4.7$ eV, x = 0.5, $L_{tunn} = 10$ nm, $L_{aux} = 15$ nm, and V_{DS}=0.5 V) and SMG-SDGTFET (...$\Phi_m = 4.5$ eV, $\Phi_m = 4.7$ eV, x = 0.5, L = 25 nm, and $V_{DS} = 0.5$ V).

2.8 Carbon based TFET

Carbon nanotubes and graphene nanoribbons are appealing materials for use in TFETs. The light effective mass of their charge carriers, their small and direct bandgap, and their excellent electrostatic control of the gate over the channel owing to the ultrathin body make them among the best choices in terms of both materials and device geometry. The first ever TFET demonstrating an S of less than 60 mV per decade was achieved with a carbon nanotube structure by Appenzeller et al. [56] in 2004. In their device, the electrostatics in the carbon nanotube were controlled by two independent gates. A common back gate electrostatically doped both the source and drain, and another gate allowed control of the channel bands, creating a p-i-p FET device. Although the on current was low because the carriers had to tunnel through two barriers, an S of 40 mV per decade was achieved for the first time. Furthermore, simulation and temperature-dependent measurements provided clear evidence that a carbon nanotube TFET had indeed been realized [56], [27]. More advantageous would be the implementation of a p-i-n-structured carbon nanotube TFET. Progress has been hampered by the difficulty of establishing appropriately doped carbon nanotube regions and abrupt junctions. So far there has been little experimental verification of carbon nanotube TFETs,

but several theoretical studies have been conducted [57]. The influence of electron-phonon scattering on the performance of carbon nanotube TFETs has also been investigated [58], and there is strong evidence that BTBT is dominated by optical phonon-assisted inelastic transport, which can lead to a degradation of the S.

Furthermore, simulations have shown that the specific energy dependence of the one-dimensional density of states (which arises because the nanowire radius is so small) can be exploited to reach the quantum capacitance limit, resulting in better control of the channel potential. In this regime, the quantum capacitance, C_q, which is determined by the change of the charge in the channel resulting from a change in gate potential, is far smaller than the oxide capacitance, C_{ox}, due to the BTBT, and thus almost equals the total capacitance. This leads to a reduced total capacitance and improves the gate delay [59].

TFETs based on graphene nanoribbons theoretically offer the same benefits as carbon nanotube TFETs and may also provide planar processing compatibility. But so far, only theoretical studies have been performed, and these demonstrate the high potential of graphene nanoribbons in significantly improving I_{ON} to several hundred $\mu A/\mu m$, with an I_{OFF} of only a few $pA/\mu m$ and a slope of less than 20 mV per decade [60].

However, for a practical implementation using graphene nanoribbons, the influence of the line edge roughness on the bandgap and the transport properties, and thus on the TFET performance, must be considered. Luisier and Klimeck [61] found that with rougher edges, the off current significantly increases because of a lowering of the graphene nanoribbon bandgap and an increase in the source-to-drain tunnelling leakage through the gate potential barrier. This leads to a deterioration of S and I_{ON}/I_{OFF}, which are no longer sufficient and thus limit the switching performance of graphene nanoribbon TFETs. The theoretical investigations done so far show that graphene nanoribbon TFETs have great potential, although for a practical implementation, significant technical challenges need to be met. Fiori and Iannaccone [62] suggested using bilayer graphene to fabricate TFETs, presenting an attractive alternative to graphene nanoribbons. The benefit of this approach is that the required energy gap is opened by applying a vertical electric field to the graphene bilayer, rather than by preparing small ribbons, which would require single-atom precision patterning.

3

Analytical Model Development

In this chapter, the analytical models of electrostatic potential and electric field in Oxide, Channel and Buried Oxide region for a SOI TFET are developed. Here, a step by step detailed mathematical description of the proposed model is presented.First, simplified 2-D Poisson's equation on oxide, channel and buried oxide region with appropriate boundary conditions is solved for electrostatic potential and electric field intensity. Then the obtained expression for electric field is used to calculate drain current by extracting band to band tunneling generation rate.

3.1 2-D Electrostatic Potential

Fig.3.1 exhibits the schematic cross section of a SOI TFET whose channel is intrinsic. It also illustrates the device dimension parameters and griding

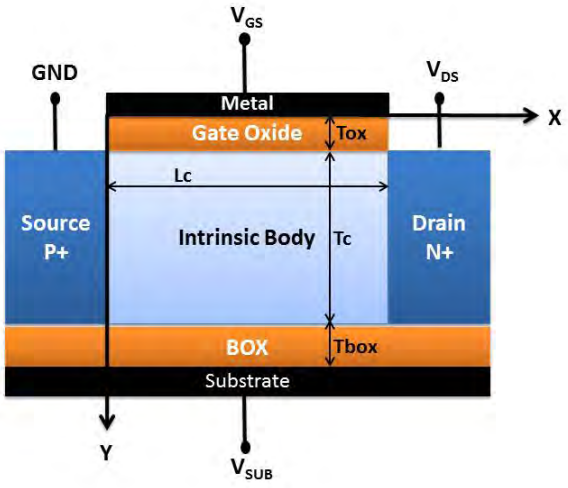

Figure 3.1: Schematic cross sectional view of modeled device

system for developing the 2-D model. This model is about anticipating the characteristics of the device from OFF state to the commencement of ON state. Throughout this sub threshold regime, the impact of mobile charge on the channel potential is negligible. For simplicity, no depletion in the source and drain region has been assumed. Under these aforementioned simplification the electrostatic potential distribution in the oxide, channel and buried oxide is dictated by following 2-D Poisson's equation.

$$\frac{\partial^2\Phi\left(x,y\right)}{\partial x^2}+\frac{\partial^2\Phi\left(x,y\right)}{\partial y^2}=0 \;\;:\;\; 0\leq x\leq L_c\,;\,0\leq y\leq(T_{ox}+T_{si}+T_{box}) \quad (3.1)$$

Equation 3.1 is solved under the assumption that gate oxide and box region is replace by silicon material considering permittivity difference in order to eradicate two Neumann boundary conditions which will be explained later in this section. In order to compensate for this assumption, the physical gate oxide thickness (t_{ox}) and BOX thickness (t_{box}) are converted to T_{ox} and T_{box} respectively.

$$T_{ox}=\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox} \quad (3.2)$$

$$T_{box}=\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{box} \quad (3.3)$$

Here, ϵ_{Si} and ϵ_{ox} are relative permittivity of Si and SiO_2 respectively.

3.1.1 Boundary Conditions

The Dirichlet boundary conditions in the channel region are

$$\Phi(0,y)=-V_{bi}=-E_g/2q=V_S \quad (3.4)$$

$$\Phi(L_c,y)=V_{bi}+V_{DS}=E_g/2q+V_{DS}=V_D \quad (3.5)$$

Where, E_g is the band gap of Silicon, L_c is the channel length and V_{DS} is the applied drain bias.
The Dirichlet boundary conditions in the gate oxide region are

$$\Phi(x,0)=V_{GS}-V_{FB}=V_G \quad (3.6)$$

According to [64] two-dimensional simulation (ISE) results show that in the insulator gap regions between the source/drain and gates, the potential is approximately a linear function of x when $T_{ox}/T_{si}<0.3$ The potential in the insulator gap region can then be expressed by linear interpolation. The linearity of potential in the side border of insulator region has also been checked by FEM simulation.

$$\Phi(0,y)=V_G-\frac{V_G-V_S}{T_{ox}}y \quad (3.7)$$

$$\Phi(L_c, y) = \frac{V_D - V_G}{T_{ox}} y + V_G \tag{3.8}$$

Where, $V_G = V_{GS} - V_{FB}$ and $V_{FB} = \phi_m - \phi_s$ Here, ϕ_m is the metal work function and ϕ_s is the semiconductor work function which can be written as

$$\phi_s = \chi_{si} + \frac{E_g}{2q} + \phi_f \tag{3.9}$$

Where, $\phi_f = V_T \ln(N_I/n_i)$ is the Fermi potential, χ_{si} is the Electron affinity, V_T is the thermal voltage and n_i is the intrinsic carrier concentration.
The Dirichlet boundary conditions in the buried oxide region are

$$\Phi(x, L_y) = V_{sub} \tag{3.10}$$

Here, V_{sub} is the substrate bias.

$$\Phi(0, y) = V_S - \frac{(V_S - V_{sub})\{y - (T_{ox} + T_{si})\})}{T_{box}} \tag{3.11}$$

$$\Phi(L_c, y) = V_D - \frac{(V_D - V_{sub})\{y - (T_{ox} + T_{si})\})}{T_{box}} \tag{3.12}$$

Where, $L_y = T_{ox} + T_{si} + T_{box}$. Except these Dirichlet boundary conditions there are two Neumann boundary conditions at the top and bottom Si/SiO_2 interface.

$$\epsilon_{ox} \frac{d\Phi}{dy}\Big|_{y=T_{ox}} = \epsilon_{si} \frac{d\Phi}{dy}\Big|_{y=T_{ox}} \tag{3.13}$$

and

$$\epsilon_{si} \frac{d\Phi}{dy}\Big|_{y=T_{ox}+T_{si}} = \epsilon_{ox} \frac{d\Phi}{dy}\Big|_{y=T_{ox}+T_{si}} \tag{3.14}$$

Fig.3.2 illustrates all the boundary conditions in the oxide, semiconductor and buried oxide region. As can be seen from Fig.3.2, if we can omit the two Neumann boundary conditions at the two Si/SiO_2 interface, then it would be a lot more easier to explicitly solve Poisson's equation under the aforementioned boundary conditions. [63] pointed out that the discontinuity of electric field at the two oxide/semiconductor interfaces can be eliminated by simply scaling the oxide thickness by $r = \epsilon_{si}/\epsilon_{ox}$ and using ϵ_{si} as its dielectric constant. But, this scaling of oxide thickness has already been done. So, we effectively transformed our problem to solving Laplace equation with rectangular boundary conditions.

By using separation of variable method it can be shown that $\Phi(x, y)$ is given by the following expression

$$\Phi(x, y) = u(x, y) + v(x, y) \tag{3.15}$$

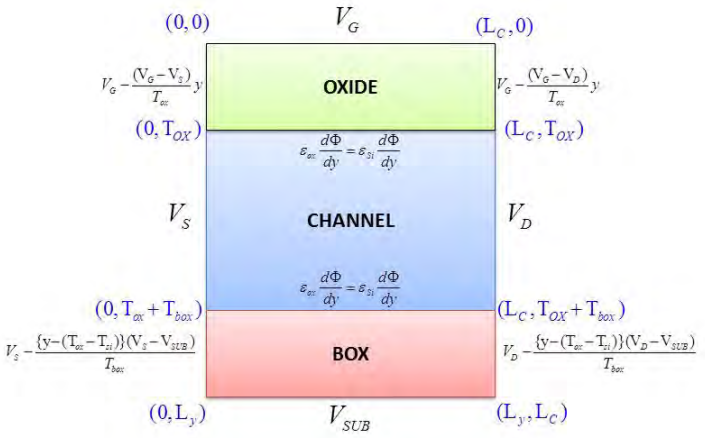

Figure 3.2: Schematic diagram of the reduced region over which the Poisson's equation is solved and expanded view of boundary conditions.

Where, $u(x, y)$ takes care of top and bottom boundary conditions and $v(x, y)$ takes care of left and right boundary conditions shown in Fig. 2.

3.1.2 Effect of Gate and Substrate Voltage

The explicit expression of $u(x, y)$ can be obtained by solving the following partial differential equation.

$$\frac{\partial^2 u\,(x,y)}{\partial x^2} + \frac{\partial^2 u\,(x,y)}{\partial y^2} = 0 \tag{3.16}$$

With boundary conditions.

$$u(x,0) = V_G \tag{3.17}$$

$$u(x,L_y) = V_{SUB} \tag{3.18}$$

$$u(0,y) = 0 \tag{3.19}$$

$$u(L_c,y) = 0 \tag{3.20}$$

So, we have a homogeneous partial differential equation with some homogeneous boundary conditions. If we assume that $u(x, y)$ has a product form $u(x, y) = X(x)Y(y)$ then eqn. 3.1 becomes

$$Y(y)X(x)'' + X(x)Y(y)'' = 0 \tag{3.21}$$

This equation can be separated by dividing through by XY to yield.

$$\frac{X(x)''}{X(x)} = -\frac{Y(y)''}{Y(y)} \tag{3.22}$$

The non homogeneous conditions eqn. 3.17 and 3.18 will not, in general, become conditions on X or Y, but homogeneous conditions eqn. 3.19 and 3.20 require that

$$X(0) = 0 \qquad X(L_c) = 0 \tag{3.23}$$

Now, both sides of eqn. 3.22 must be constant but the sign of the constant is not obvious. If we try positive constant (say, μ^2), eqn. 3.22 represents two ordinary differential equation

$$X'' - \mu^2 X = 0 \qquad Y'' + \mu^2 Y = 0 \tag{3.24}$$

The solution of these equations are

$$X(x) = A\cosh(\mu x) + B\sinh(\mu x) \qquad Y(y) = C\cos(\mu y) + D\sin(\mu y) \tag{3.25}$$

In order to make $X(x)$ satisfy the boundary conditions eqn. 3.23 both A and B must be zero, leading to a solution $u(x, y) = 0$. Thus, we try the other possibility for sign, taking both members in eqn. 3.22 to equal $-\lambda^2$. Under the new assumption eqn. 3.22 separates into

$$X'' + \lambda^2 X = 0 \qquad Y'' - \lambda^2 Y = 0 \tag{3.26}$$

The first of these equations along with the boundary conditions is recognizable as eigen value problem, whose solutions are.

$$X_n(x) = \sin(\lambda_n x) \tag{3.27}$$

Where,

$$\lambda_n = \frac{n\pi}{L_c} \tag{3.28}$$

The function Y that accompany the X's are

$$Y_n(y) = a_n\cosh(\lambda_n y) + b_n\sinh(\lambda_n y) \tag{3.29}$$

The a's and b's are for the moment unknown. We see that $X_n(x)Y_n(y)$ is a solution of the homogeneous potential which satisfies the homogeneous

conditions eqn. 3.19 and 3.20. A sum of these functions should satisfy the same conditions and equation. So, $u(x, y)$ may have the form

$$u(x,y) = \sum_{n=1}^{\infty} \sin(\lambda_n x)(a_n \cosh(\lambda_n y) + b_n \sinh(\lambda_n y)) \tag{3.30}$$

The non-homogeneous boundary conditions eqn. 3.16 and 3.17 are yet to be satisfied. If $u(x, y)$ is to be of the form eqn. 3.30, the boundary condition eqn. 3.17 becomes

$$u(x,0) = \sum_{n=1}^{\infty} a_n \sin(\lambda_n x) = V_G \quad : \quad 0 \leq x \leq L_c \tag{3.31}$$

So, a_n must be the Fourier sine coefficients of V_G

$$a_n = \frac{2}{L_c} \int_0^{L_c} V_G \sin(\frac{n\pi x}{Lc}) dx = \frac{2V_G}{n\pi} \{1 - \cos(n\pi)\} \tag{3.32}$$

Now, the second boundary condition reads

$$u(x,y) = \sum_{n=1}^{\infty} \sin(\lambda_n x)(a_n \cosh(\lambda_n L_y) + b_n \sinh(\lambda_n L_y)) = V_{SUB} \quad : \quad 0 \leq x \leq L_c \tag{3.33}$$

The constant $(a_n \cosh(\lambda_n L_y) + b_n \sinh(\lambda_n L_y))$ must be the nth Fourier sine co-efficient of V_{SUB}. Since a_n is known b_n can be determined from the following computation.

$$a_n \cosh(\lambda_n L_y) + b_n \sinh(\lambda_n L_y) = \frac{2}{L_c} \int_0^{L_c} V_{SUB} \sin(\frac{n\pi x}{Lc}) dx = \frac{2V_G}{n\pi} \{1 - \cos(n\pi)\} = c_n \tag{3.34}$$

$$b_n = \frac{c_n - a_n \cosh(\lambda_n L_y)}{\sinh(\lambda_n L_y)} \tag{3.35}$$

If we use this last expression for b_n and substitute into eqn. 3.30 we find the following solution.

$$u(x,y) = \sum_{n=1}^{\infty} \sin(\lambda_n x) \frac{a_n \sinh\{\lambda_n (L_y - y)\} + c_n \sinh(\lambda_n y)}{\sinh(\lambda_n L_y)} \tag{3.36}$$

Where,

$$c_n = \frac{2}{L_c} \int_0^{L_c} V_{SUB} \sin(\frac{n\pi x}{Lc}) dx = \frac{2V_{SUB}}{n\pi} \{1 - \cos(n\pi)\} \tag{3.37}$$

and a_n is defined by eqn. 3.32

3.1.3 Effect of Source and Drain Boundaries

Similarly, the explicit mathematical expression for $v(x, y)$ can be obtained by solving the following partial differential equation.

$$\frac{\partial^2 v\,(x,y)}{\partial x^2} + \frac{\partial^2 v\,(x,y)}{\partial y^2} = 0 \tag{3.38}$$

With the following boundary conditions.

$$v(x,0) = 0 \tag{3.39}$$

$$v(x,L_y) = 0 \tag{3.40}$$

$$v(0,y) = \begin{cases} \frac{(V_S - V_G)y}{T_{ox}} + V_G & : 0 \le y \le T_{ox} \\ V_S & : T_{ox} \le y \le T_y \\ V_S - \frac{(V_S - V_{SUB})(y-(T_{ox}+T_{si}))}{T_{box}} & : (T_{ox}+T_{si}) \le y \le L_y \end{cases} \tag{3.41}$$

$$v(L_c,y) = \begin{cases} \frac{(V_D - V_G)y}{T_{ox}} + V_G & : 0 \le y \le T_{ox} \\ V_D & : T_{ox} \le y \le T_y \\ V_D - \frac{(V_D - V_{SUB})(y-(T_{ox}+T_{si}))}{T_{box}} & : (T_{ox}+T_{si}) \le y \le L_y \end{cases} \tag{3.42}$$

Solving equation 3.38 according to the aforementioned procedure yields the following expression

$$v(x,y) = \sum_{n=1}^{\infty} \sin(\mu_n y) \frac{A_n \sinh(\mu_n x) + B_n \sinh\{\mu_n (L_c - x)\}}{\sinh(\mu_n L_c)} \tag{3.43}$$

Where,

$$\mu_n = \frac{n\pi}{L_y} \tag{3.44}$$

$$A_n = \frac{2}{L_y} \int_0^{L_y} v(L_c,y) \sin(\mu_n y) dy \tag{3.45}$$

$$B_n = \frac{2}{L_y} \int_0^{L_y} v(0,y) \sin(\mu_n y) dy \tag{3.46}$$

Carrying out the integration we can get the following expressions for A_n and B_n

$$A_n = A_{n1} + A_{n2} + A_{n3} + A_{n4} + A_{n5} \tag{3.47}$$

With

$$A_{n1} = \frac{2(V_D - V_G)L_y}{n^2\pi^2 T_{ox}} \{sin(\mu_n T_{ox}) - \mu_n T_{ox}\cos(\mu_n T_{ox})\} \tag{3.48}$$

$$A_{n2} = \frac{2V_G}{n\pi} \{1 - \cos(\mu_n T_{ox})\} \tag{3.49}$$

$$A_{n3} = \frac{2V_D}{n\pi} \{1 + \cos(\mu_n T_{ox})\} \tag{3.50}$$

$$A_{n4} = \frac{2(V_D - V_{SUB})L_y}{n^2\pi^2 T_{box}} \{sin(\mu_n(T_{ox} + T_{si})) - \mu_n(T_{ox} + T_{si})\cos(\mu_n(T_{ox} + T_{si})) - n\pi\} \tag{3.51}$$

$$A_{n5} = \frac{2(V_D - V_{SUB})(T_{ox} + T_{si})}{n\pi T_{box}} \{1 + \cos(\mu_n(T_{ox} + T_{si}))\} \tag{3.52}$$

And

$$B_n = B_{n1} + B_{n2} + B_{n3} + B_{n4} + B_{n5} \tag{3.53}$$

With

$$B_{n1} = \frac{2(V_S - V_G)L_y}{n^2\pi^2 T_{ox}} \{sin(\mu_n T_{ox}) - \mu_n T_{ox}\cos(\mu_n T_{ox})\} \tag{3.54}$$

$$B_{n2} = \frac{2V_G}{n\pi} \{1 - \cos(\mu_n T_{ox})\} \tag{3.55}$$

$$B_{n3} = \frac{2V_S}{n\pi} \{1 + \cos(\mu_n T_{ox})\} \tag{3.56}$$

$$B_{n4} = \frac{2(V_S - V_{SUB})L_y}{n^2\pi^2 T_{box}} \{sin(\mu_n(T_{ox} + T_{si})) - \mu_n(T_{ox} + T_{si})\cos(\mu_n(T_{ox} + T_{si})) - n\pi\} \tag{3.57}$$

$$B_{n5} = \frac{2(V_S - V_{SUB})(T_{ox} + T_{si})}{n\pi T_{box}} \{1 + \cos(\mu_n(T_{ox} + T_{si}))\} \tag{3.58}$$

3.2 2-D Electric Field Intensity

The electric field intensity along the channel ($E_x(x,y)$) and perpendicular to the channel ($E_y(x,y)$) can be obtained by analytical derivation of the channel electrostatic potential $\Phi(x,y)$

$$E_x(x,y) = -\frac{\partial \Phi(x,y)}{\partial x} = -\left\{\frac{\partial u(x,y)}{\partial x} + \frac{\partial v(x,y)}{\partial x}\right\} = -\left\{u_x(x,y) + v_x(x,y)\right\} \tag{3.59}$$

Where,

$$u_x(x,y) = \sum_{n=1}^{\infty} \lambda_n \cos(\lambda_n x) \frac{a_n \sinh\left\{\lambda_n (L_y - y)\right\} + c_n \sinh(\lambda_n y)}{\sinh(\lambda_n L_y)} \tag{3.60}$$

and

$$v_x(x,y) = \sum_{n=1}^{\infty} \mu_n \sin(\mu_n y) \frac{A_n \cosh(\mu_n x) - B_n \cosh\left\{\mu_n (L_c - x)\right\}}{\sinh(\mu_n L_c)} \tag{3.61}$$

Similarly,

$$E_y(x,y) = -\frac{\partial \Phi(x,y)}{\partial y} = -\left\{\frac{\partial u(x,y)}{\partial y} + \frac{\partial v(x,y)}{\partial y}\right\} = -\left\{u_y(x,y) + v_y(x,y)\right\} \tag{3.62}$$

Where,

$$u_y(x,y) = \sum_{n=1}^{\infty} \lambda_n \sin(\lambda_n x) \frac{c_n \cosh(\lambda_n y) - a_n \cosh\left\{\lambda_n (L_y - y)\right\}}{\sinh(\lambda_n L_y)} \tag{3.63}$$

and

$$v_y(x,y) = \sum_{n=1}^{\infty} \mu_n \cos(\mu_n y) \frac{A_n \sinh(\mu_n x) + B_n \sinh\left\{\mu_n (L_c - x)\right\}}{\sinh(\mu_n L_c)} \tag{3.64}$$

Up to this point we have developed explicit expressions for horizontal and vertical component of the electric field as a function of (x,y) for 2-D plane under consideration. So, the total electric field can be found by applying Pythagorean theorem, which is as follows,

$$E(x,y) = \sqrt{E_x(x,y)^2 + E_y(x,y)^2} \tag{3.65}$$

3.3 Drain Current

The tunnel current I_{DS} can be found by numerical integration of band to band carrier generation rate G_{btb} over the channel region.

$$I_{DS} = qW_{ch} \int_{x=0}^{x=L_c} \int_{y=T_{ox}}^{y=T_{ox}+T_{si}} G_{btb} dx dy \tag{3.66}$$

Where, W_{ch} refers to the channel width. In order to evaluate band to band generation rate we used Kane's Model [21] which is as follows:

$$G_{btb} = A\frac{E(x,y)^D}{\sqrt{E_g}}exp(-B\frac{E_g^{3/2}}{E(x,y)}) \tag{3.67}$$

In this expression, $E(x,y)$ is the electric field and E_g is the band-gap of the channel material. A, B and D are the material based parameters. Although the mobile charge was neglected in the model derivation, the current can be predicted with this approach because eqn. 3.67 depends upon the electric field distribution in the channel. From the OFF state to the ON state the electric field intensity distribution is mainly controlled by the fixed charge and is therefore accurately predicted by our model.

4

Development of Simulation Model

Benchmarking of an analytical model is inevitable to make the proposed model acceptable to the scientific community. In this chapter two simulation models have been developed, one in COMSOL Multiphysics 4.3b and the other in SILVACO ATLAS, to check the validity of the proposed model. A detailed description of various commands and their contextual meaning are also presented in this chapter.

4.1 SILVACO ATLAS

Silicon Valley Company (Silvaco) is a leading vendor in technology computer aided design (TCAD). Established in 1984 and located in Santa Clara, California, Silvaco has developed a number of exceptional CAD simulation tools to aid in semiconductor process and device simulation. Silvaco has an extensive support team to assist with the broad area of semiconductor technologies. The ability to accurately simulate a semiconductor device is critical to industry and research environments. The ATLAS device simulator is specifically designed for 2D and 3D modeling to include electrical, optical and thermal properties within a semiconductor device. ATLAS provides an integrated physics-based platform to analyze DC, AC and time-domain responses for all semiconductor-based technologies. The powerful input syntax allows the user to design any semiconductor device using both standard and user-defined material of any size and dimension. ATLAS also offers a number of useful device examples to assist one's unique design. DeckBuild is the run time environment used to input a command file or deck and is given the extension ".in". To run ATLAS in the DeckBuild environment, the user must first call the ATLAS simulator with the command:

```
go atlas
```

There is other simulation software available that can be used in conjunction with DeckBuild, such as ATHENA and DevEdit, but in this work we have used only ATLAS.

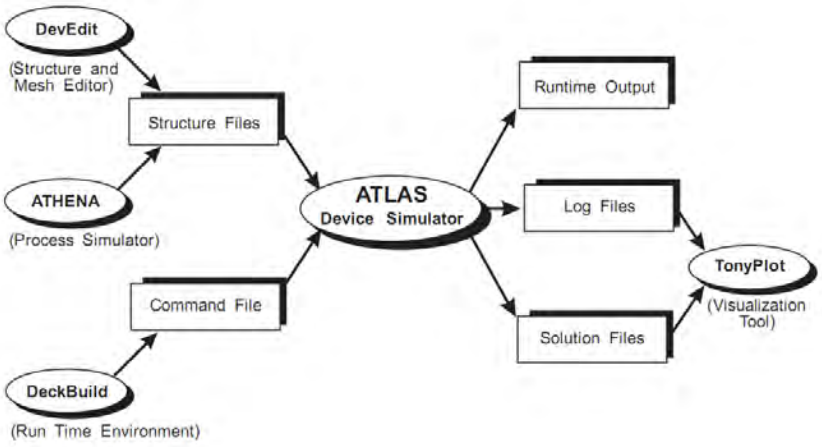

Figure 4.1: Atlas Inputs and Outputs Ref.[65]

4.1.1 ATLAS Commands

Once ATLAS is called there is a syntax structure that must be followed in order for ATLAS to execute the command file successfully. Table. 4.1 shows a list of primary group and statement structure specifications. Although there are a few input exceptions, the input file statements follow the general format of:

```
<STATEMENT><PARAMETER>=<VALUE>
```

The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order. Otherwise, an error message will appear, which may cause incorrect operation or termination of the program. For example, if the material parameters or models are set in the wrong order, then they may not be used in the calculations. The order of statements within the mesh definition, structural definition, and solution groups is also important. Otherwise, it may also cause incorrect operation or termination of the program.

4.1.2 Model Development in ATLAS

Meshing

The mesh statement is used to define the structure in an inverted 2D or 3D Cartesian grid. The x-axis is positive from left to right, the y-axis is negative from bottom to top. The reason for the inverted y-axis is that the manufacturing coordinates are usually described as depth below the surface. All coordinates are entered in microns and the spacing is used to refine the sharpness and accuracy at an assigned location. ATLAS produces

Table 4.1: ATLAS Command groups with primary statements in each group Ref.[65]

Group	Statements
Structure Specification	MESH, REGION, ELECTRODE, DOPING
Material Models Specification	MATERIAL, MODEL, CONTACT, INTERFACE
Numerical Method Selection	METHOD
Solution Specification	LOG, SOLVE, LOAD, SAVE
Results Analysis	EXTRACT, TONYPLOT

a series of triangles to form the mesh based on the user input parameters. Fig.4.2 shows the mesh of a Tunnel FET along with the parameters entered in ATLAS.

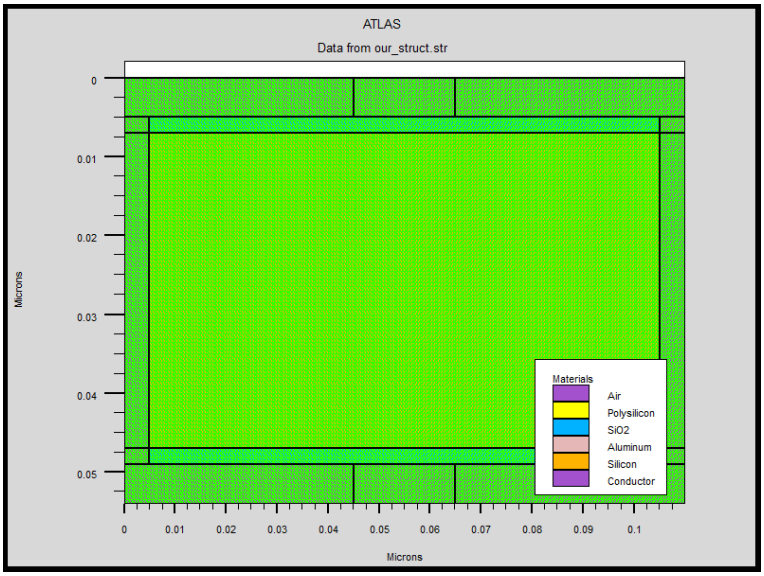

Figure 4.2: Meshing of SOI Tunnel FET

The accuracy of any calculated value in ATLAS is dependent on the refinement of the mesh at the junction of interest. The `x.mesh` and `y.mesh` is much finer in the region under the gate to have a better calculation at the areas where tunneling occurs.

Regions

The region statement is used to separate the initial mesh statement into distinct blocks and sets the initial material parameters that can be referred to later by region number. All meshed areas of a structure must be assigned

a region and the regions must be ordered from lowest to highest region. For instance, region 3 cannot be defined before region 2.

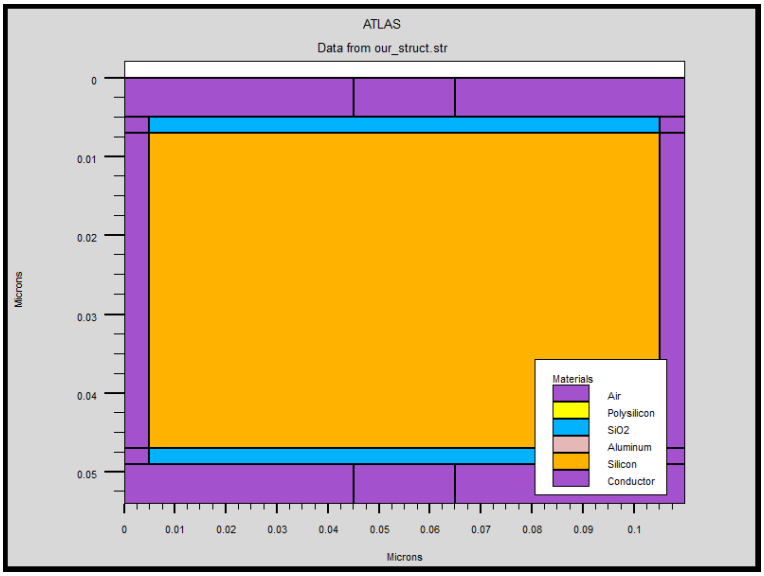

Figure 4.3: Different regions of SOI Tunnel FET

Electrode

Once the regions are set, the electrodes must be assigned to the desired region so that it can be electrically analyzed. The electrodes can be assigned to any region or portion of a region. ATLAS has some fixed names for electrodes e.g. Anode, Cathode, Gate, Source, and Drain. The following statements were used to define these parameters:

```
ELECTRODE <position_parameters> NAME=<electrode name>
```

The position parameters are specified in microns using the `X.MIN`, `X.MAX`, `Y.MIN`, and `Y.MAX` parameters. Multiple electrode statements may have the same electrode name. Nodes that are associated with the same electrode name are treated as being electrically connected.

Doping

The last required input of the structure specification is the doping statement. The doping statement is used to assign the doping level within the previously assigned regions. Various properties can be appended to the doping statement to specify how the semiconductor was doped and of whether the region is n or p type. The following statements were used to

define doping parameters:

```
DOPING <distribution_type> <dopant_type> <position_parameters
```

Analytical doping profiles can have uniform or Gaussian forms. The position parameters X.MIN, X.MAX, Y.MIN, and Y.MAX can be used instead of a region number. With the doping statement complete, the structure specifications are complete and it is possible to continue with the simulation following the guidelines in Table. 4.1. Unlike the structure specifications, the remaining four groups to be specified do not require all statements to run without error.

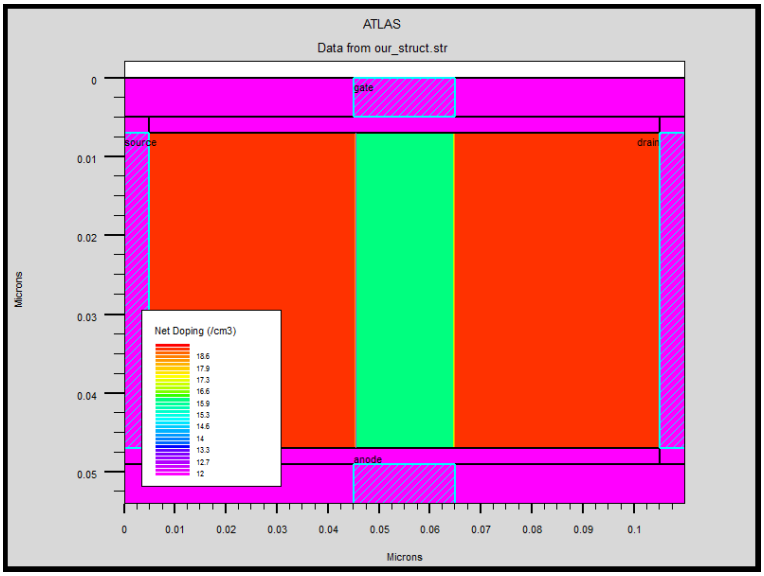

Figure 4.4: Cross section of SOI Tunnel FET showing doping in different regions and electrodes

Material

The material statement relates physical parameters with the materials assigned to the mesh. The important material parameters for most standard semiconductors are already defined by ATLAS and therefore do not require any changes. We utilized the extensive model libraries in ATLAS since the developed tunnel junctions were based in Si which is very well researched and documented.

Models

The models statement is essential to the accurate modeling of a particular phenomenon because it sets flags for ATLAS to indicate the inclusion of different mathematical models, physical mechanisms and other global

Table 4.2: Description of different models used in this research

Model	Syntax	Comments
Band Gap Narrowing	BGN	Important in heavily doped regions. Critical for bipolar gain. Use Klaassen Model
Lombardi(CVT) Model	CVT	Complete Model including N, T, $E_{\|\|}$ and $E_{\perp}$ effects. Good for non-planar devices.
Shockley-Read-Hall	SRH	Uses fixed minority carrier lifetime. Should be used in most simulations
Band to Band Tunneling (Kane)	BBT.KANE	Allows modeling of forward and reverse tunneling current

parameters such as substrate temperature. The model statement and parameters used in this research are listed below:

Statement used in our code:

```
MODELS BGN cvt fermi SRH PRINT bbt.kane
```

As with all ATLAS statements, a complete list of modeling parameters and their definitions can be found in the ATLAS User's Manual [65].

Contact

CONTACT statement used for shorting the two gates. These can be also done by naming the two electrodes same. Two gates are shorted by this statement for double gate structure.

```
CONTACT NAME=<contact_name> COMMON=<contact_name>
```

Numerical Method Selection

The NEWTON method is useful when the system of equations is strongly coupled and has quadratic convergence. The NEWTON method may however spend extra time solving for quantities which are essentially constant or weakly coupled. NEWTON also requires a more accurate initial guess to the problem to obtain convergence.

```
METHOD NEWTON CLIMIT=1.0 DVMAX=0.005
```

Here the DVMAX statement sets the maximum allowed potential update per Newton Iteration, and the CLIMIT specifies a concentration normalization factor.

Output

Several quantities are saved by default within a structure file. For example,doping, electron concentration, and potential. We specified additional quantities (such as conduction band potential, valence band potential, hole quasi Fermi level, electron quasi Fermi level) by using the OUTPUT statement.

```
OUTPUT CON.BAND VAL.BAND qfn qfp
```

Solution Specification

The log/solve/save statements are used to create data files in ATLAS simulations. These statements work together to be provide data to be analyzed by other functions. In this research we used these statements to analyze drain current with respect to gate voltage or drain voltage.

Log

The LOG statement allows all terminal characteristics generated by a solve statement to be saved to a file.

Solve

The SOLVE statement specifies which bias points are to be applied to produce an output. The bias points can be set in a number of different way including step, initial and lambda depending on what stimulus is desired.

Save

The SAVE statement is used to save all node point data into an output file. A common use of the LOG/SOLVE/SAVE statements for the tunnel junction studied is shown below:

```
   solve name=gate vgate=-0.2 vfinal=1 vstep=0.2
save outfile = our_struct.str
tonyplot our_struct.str
```

```
tonyplot IvsVgs_SG_20nm_conventional_Vds_01.log
```

Here the output file `IvsVgs_SG_20nm_conventional_Vds_01.log` has been set aside to store data from the solve statements and then saved so that the data can be called at a later time. The solve statements simply sweep the voltage from -0.2V to 1V in varying voltage steps depending on the degree of accuracy at the desired range. With the date stored in an outfile, it is ready to be displayed so that it can be analyzed.

Results

The TONYPLOT statement is used to start the graphical post-processor tool.

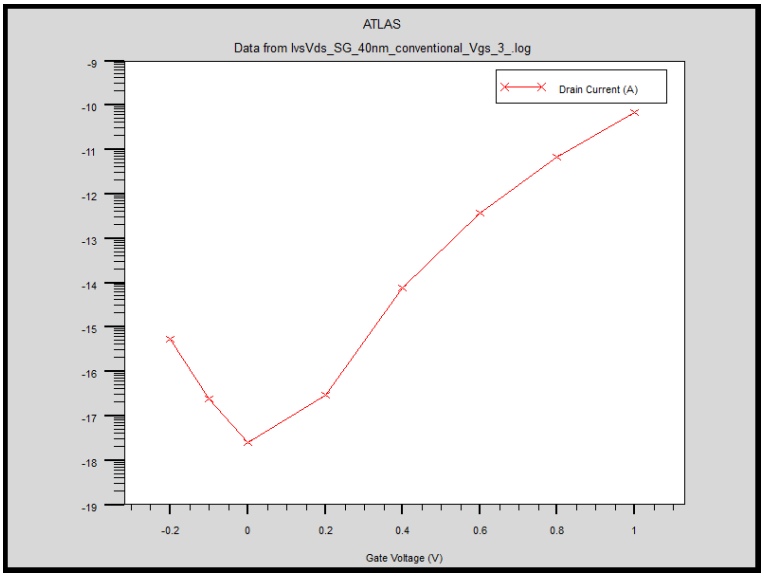

Figure 4.5: I_{DS} vs V_{GS} characteristics for $V_{DS} = 0.1V$

Calling tonyplot to visualize `IvsVgs_SG_20nm_conventional_Vds_01.log` displays the output file in Fig 4.5 .

Simulation parameters and results

Here we used the 2D simulator as we don't need to simulate our structure in 3D. It will save our time also as 2D simulation is much faster than the other one. Followings are the simulation parameters used in this work.
Material used : Si
Source Doping $(p+)$: $10^{19}cm^{-3}$
Drain Doping $(n+)$: $10^{19}cm^{-3}$
Intrinsic Channel Doping : $10^{16}cm^{-3}$ (to resolve convergence issue)
Channel Length : 20 nm

Channel Thickness : 40 nm
Oxide Used : SiO_2
Oxide Thickness : 2 nm
BOX Thickness : 2 nm
Models Used : Band gap narrowing, nonlocal band to band tunneling, Lombardi(CVT) Model, Shockley-Read-Hall(SRH).

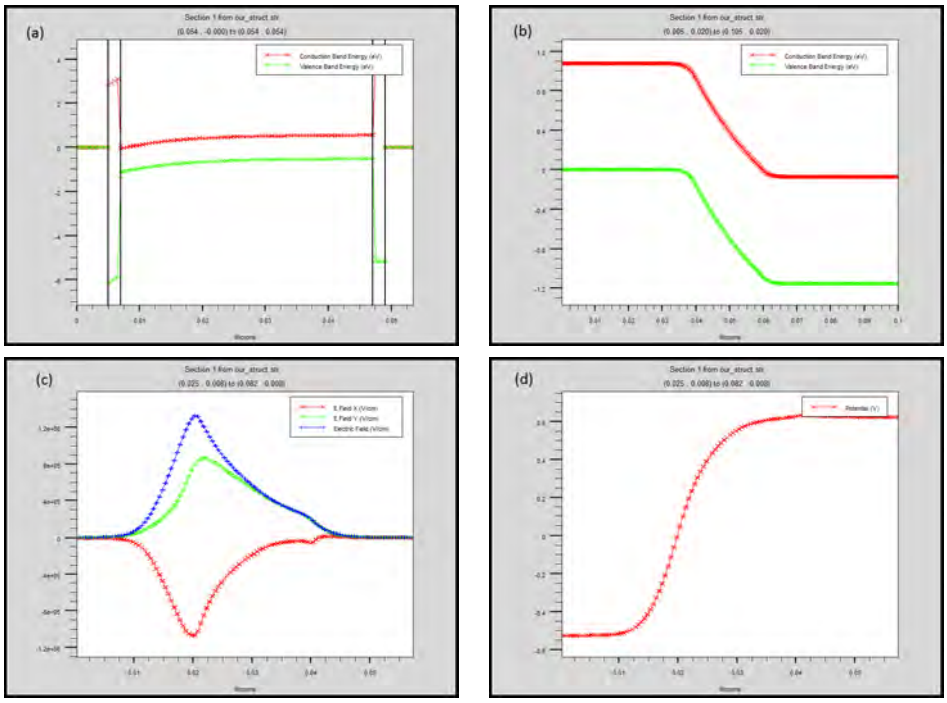

Figure 4.6: (a) Conduction and valance band energy perpendicular to the channel (b) Conduction and valance band energy along the channel (c) Electric field, its horizontal and vertical component along the channel (d) Potential variation from the source to drain terminal

After the simulation have been done a number of different other parameters can be observer. By drawing a cutline along an arbitrary direction specified by two points in the xy plane, we can examine the variation of several important parameters such as electric field, potential, conduction band energy, valance band energy etc., along the direction of cutline. Fig. 4.6 shows energy band profile, electric field and potential along various direction through the channel.

4.2 COMSOL Multiphysics

COMSOL Multiphysics [66] is a finite element analysis, solver and Simulation software package for various physics and engineering applications, es-

pecially coupled phenomena, or multiphysics. COMSOL Multiphysics also offers an extensive interface to MATLAB and its toolboxes for a large variety of programming, preprocessing and postprocessing possibilities. The packages are cross-platform (Windows, Mac, Linux). In addition to conventional physics-based user interfaces, COMSOL Multiphysics also allows for entering coupled systems of partial differential equations (PDEs). The PDEs can be entered directly or using the so-called weak form (see finite element method for a description of weak formulation). An early version (before 2005) of COMSOL Multiphysics was called FEMLAB.

In 1986, COMSOL was started by graduate students, Svante Littmarck and Farhad Saeidi, to Germund Dahlquist based on code developed for a graduate course at the Royal Institute of Technology (KTH)in Stockholm, Sweden.

4.2.1 Model Development in COMSOL Multiphysics 4.3b

To develop a Tunnel FET simulator in COMSOL we have solved 2-D Poisson's equation on oxide, channel and box region. After solving Poisson's equation in COMSOL we have extracted potential and electric field and write a MATLAB code to tunnel evaluate current.

The Model Wizard

When COMSOL Multiphysics is first opened, or when one starts creating a new model, the GUI displays the Model Builder, Graphics, and Model Wizard windows. The Model Wizard window contains a series of pages to help one in starting to build a model-*Select Space Dimension, Select Physics* and *Select Study Type*.

The Select Space Dimension Page

The final geometry dimension is specified on the Select Space Dimension page-3D, 2D axisymmetric, 2D, 1D axisymmetric, 1D, or 0D. 0D is used for physics interfaces modeling spatially homogeneous systems. In this study since we are solving 2-D Poisson's equation so we will select 2-D option.

The Add Physics Page

On the Add Physics page, one or more physics interfaces can be selected to include in the model. The **Add Selected** or **Remove Selected** buttons are used to easily add or remove physics interfaces respectively for multiphysics models. In this study we used **Poisson's Equation**

The Select Study Type Page

From the branches under **Studies** , one can select the type of study one wants to perform. The available options on the Select Study Type page depend on the set of physics interfaces (and mathematics interfaces) included in the model. We have selected **Stationary** for our study.

So the basic steps to build a model file in COMSOL are as follows:

- In the **Model Wizard**, **Select a Space Dimension** for the model: 2D
- Click the **Next** button. The **Add Physics page** opens.
- In the **Add Physics page** go to **Mathematics>Classical PDEs>Poisson's Equation**. Then, Double-click the physics interface, click the **Add Selected**
- Click the **Next** button
- On the **Select Study Type page**, select: **Preset Studies > Stationary**
- click the **Finish** button

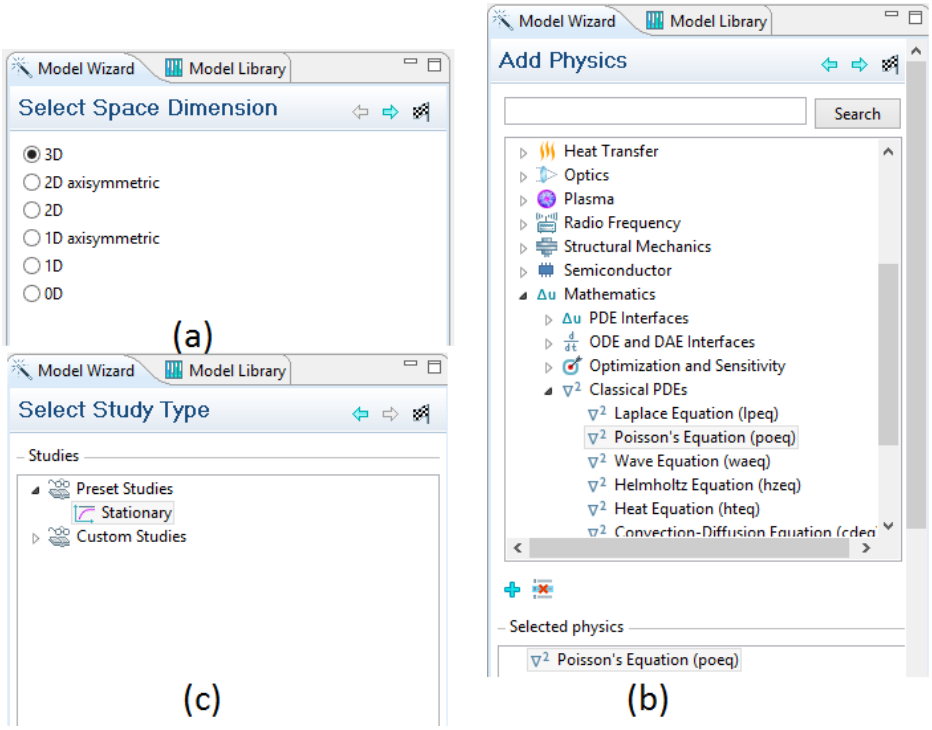

Figure 4.7: (a) Select Space Dimension Page (b) Add Physics Page (c) Select Study Type Page

After the development of **model** file in COMSOL, we can now move forward to the model builder window.

The Model Builder Window

The modeling procedure is controlled through the **Model Builder window**, which includes a model tree with all the functionality and operations for building and solving models and displaying the results.

Branches in the Model Tree

The main branches include:

- The *Global Definitions* branch : This branch defines parameters and functions that can be used everywhere. In our study we have defined device dimensions Channel length, channel thickness, oxide thickness and applied bias in this branch; Fig. [] shows the defined values of these parameters.
- The *Model branches*: for defining models. A Model branch includes the associated subbranches of *Definitions* , for locally defining parts of the model, Geometry, Materials, Physics, and Meshes. A Model branch includes functionality for local Definitions because several models can separately be defined in one multiphysics file, for example, when treating certain parts of the model in 2D and other parts in 3D, or when setting up a system model with several components. This branch will be discussed in detail, later.
- The *Study branch*: For setting up study steps and solver configurations.
- The *Results branch*: for presenting and analyzing results.

Sub Branches in the Model Branch

- *Definitions*: In this sub-branch three variables, are defined which are basically electric permittivity for different regions such as oxide, channel, buried oxide.
- *Geometry*: In this sub-branch three rectangles of same length but different width have been drawn in order to define three regions: oxide, channel, buried oxide which together constitute Poisson's equation solving zone.
- *Poisson's Equation*: In this sub-branch *Dirichlet Boundary Conditions*, *Zero Flux Boundary Condition* and source (f) of Poisson's equation ($\nabla.(-c\nabla u) = f$) is defined.
- *Mesh*: For our study we have defined the following *Mesh Settings*: Sequence type: Physics Controlled Mesh, Element size : Extremely fine.

Computation

After all the aforementioned steps have been done, we need to press *Build All* and then *Compute* to finally evaluate the electrostatic potential of the device on the defined plane subject to the applied bias. The obtained potential is then extracted to compute electric field and tunneling current.

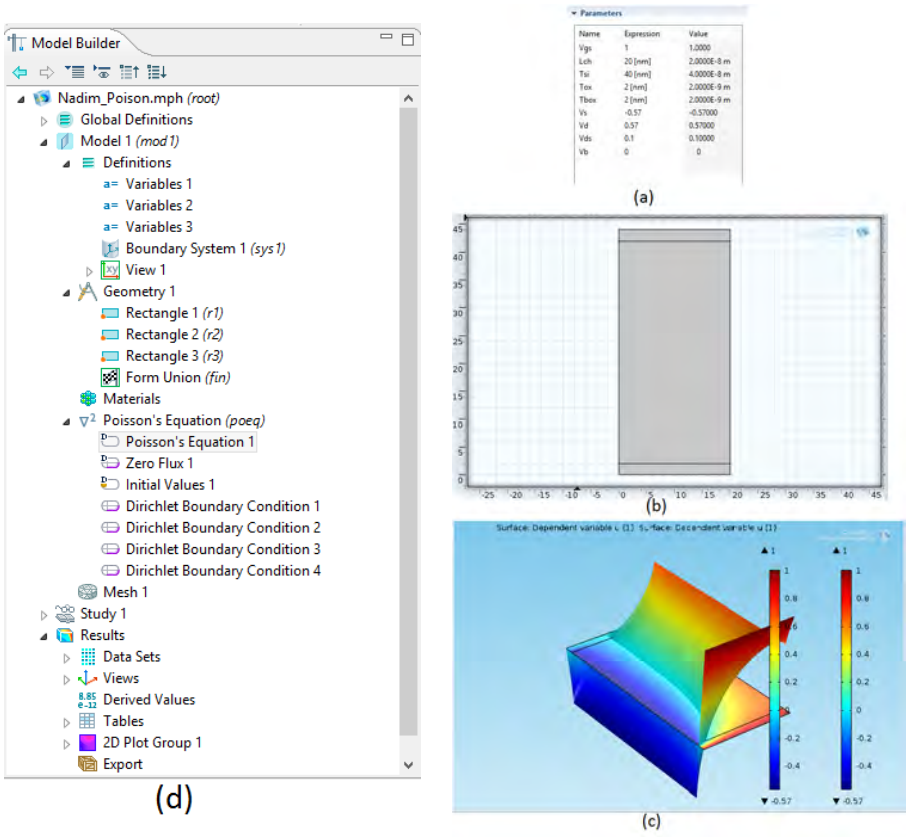

Figure 4.8: (a) Global Definitions:Parameters(Device dimensions and applied bias) (b) Device Geometry (c) Solution:Surface Plot of obtained potential variation (d) Model Wizard Window

5

Results and Discussion

This chapter presents the results obtained from analytical model as well as the simulation models developed in ATLAS and COMSOL Multiphysics. In all cases analytical modeling results show excellent agreement with the COMSOL simulation results. Since ATLAS includes a number of effects such as the width of depletion region, SHR which has been overlooked while developing the analytical model; matching with ATLAS results need slight calibration of material based parameters such as A, B and D in the Kane's model. Variation of Drain Induced Barrier Thinning (DIBT) with several device parameters such as channel length, channel thickness have also been presented in this chapter.

5.1 COMSOL Simulation Results

A device simulator in COMSOL has been developed in order to anticipate the $I_D - V_G$ characteristics of Single Gate SOI Tunnel FET. The parameters that have been used for simulator development are mentioned in Table 5.1. Fig. 5.1, 5.2, 5.5, 5.6, 5.9 and 5.10 show the two dimensional color and surface plot of channel electrostatic potential for different gate voltage (namely, $V_{GS} = 0V,\ 0.5V,\ 1V$). From these figures it is evident that the higher the gate voltage the higher the curvature of its channel potential profile; Fig. also corroborates this fact. Potential at the front gate oxide/semiconductor interface for different gate voltages are shown in Fig. 5.13. It is worth noticing that at higher gate voltage the potential profile takes the form of a parabola which can be attributed to the fact of very short channel length (here 20 nm).

Fig. 5.3,5.4,5.7,5.8,5.11,5.12 portray the two dimensional color and surface plot of channel electric field intensity for different gate voltages. No significant change of electric field is observed in the middle of the channel whereas notable enhancement of electric field is observed at the oxide channel and source intersection point(see Fig. 5.14) which is consistent with the previous studies. Fig. 5.15 exhibits the horizontal and vertical component of electric field for a particular gate voltage.

Table 5.1: Values of various device parameters used in this simulation

Parameter description	Symbol	Value
Channel Length	L_c	20 nm
Channel Width	W_{ch}	1 μ m
Channel Thickness	T_C	40 nm
Oxide Thickness	T_{ox}	2 nm
Buried Oxide Thickness	T_{box}	2 nm

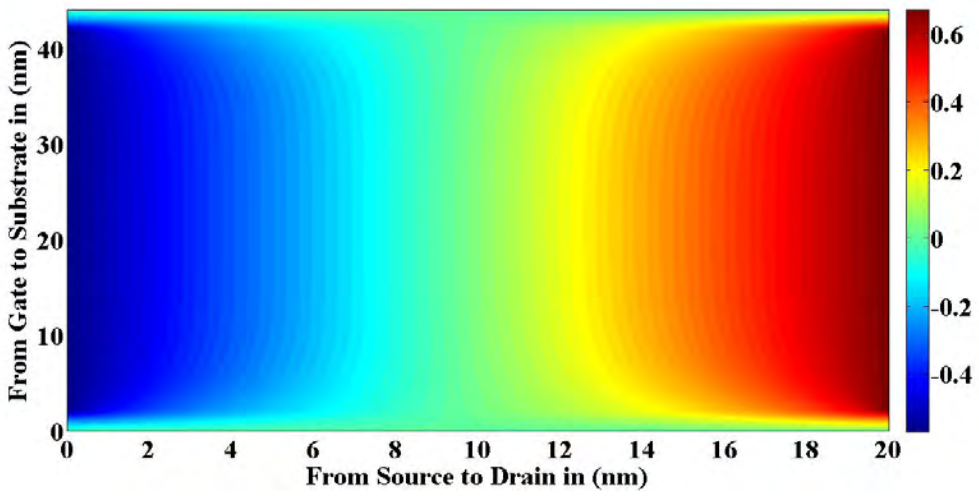

Figure 5.1: Color plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

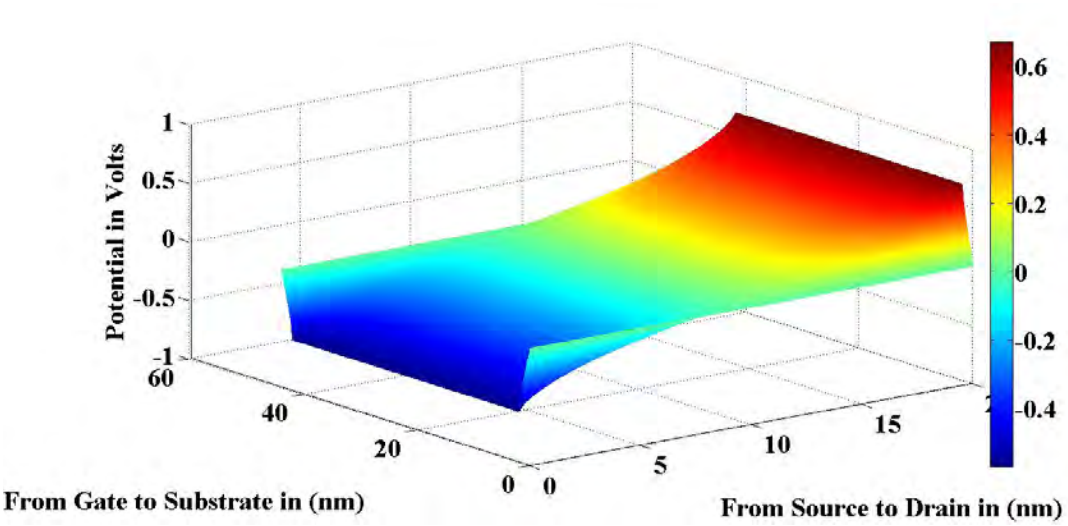

Figure 5.2: Surface plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

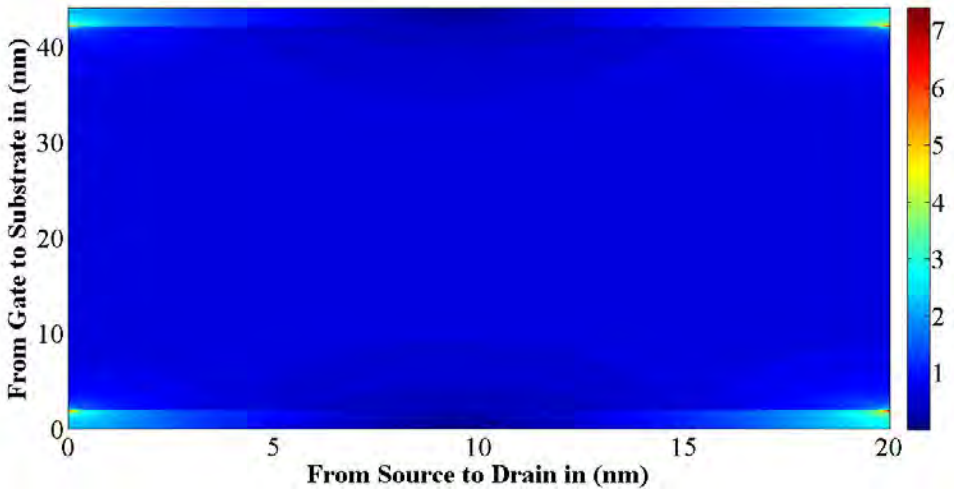

Figure 5.3: Color plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

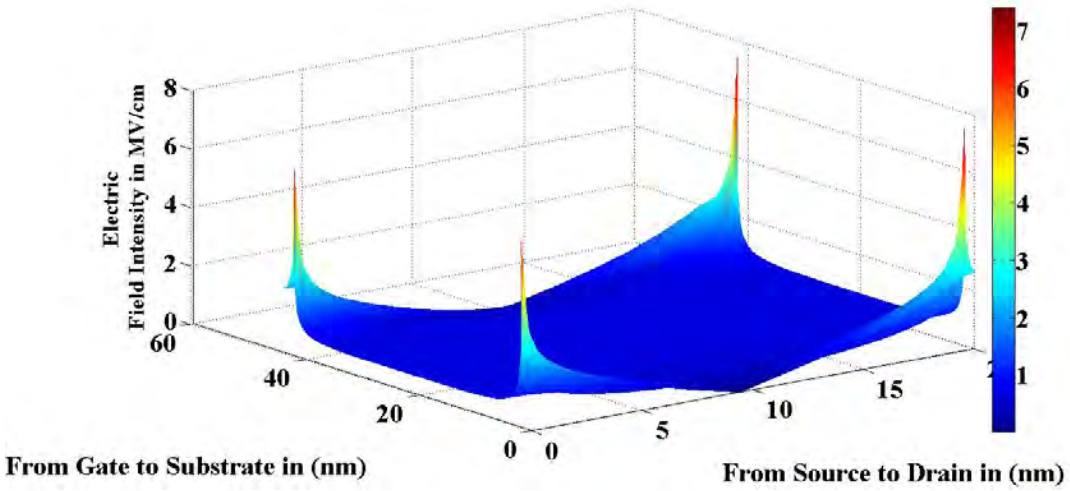

Figure 5.4: Surface plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

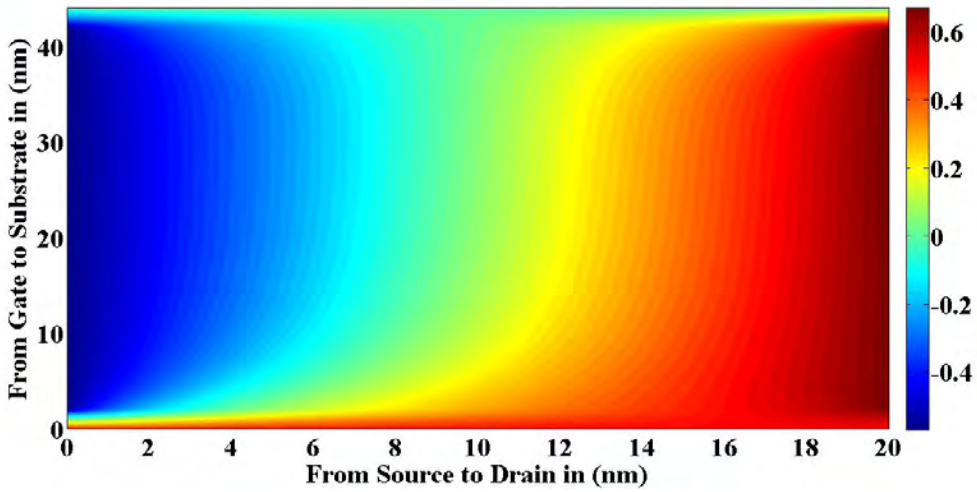

Figure 5.5: Color plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

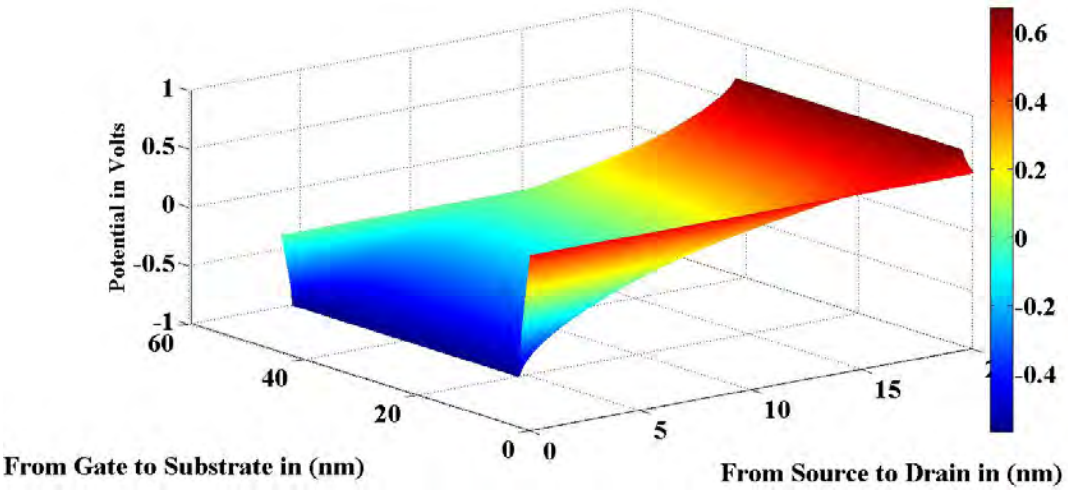

Figure 5.6: Surface plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

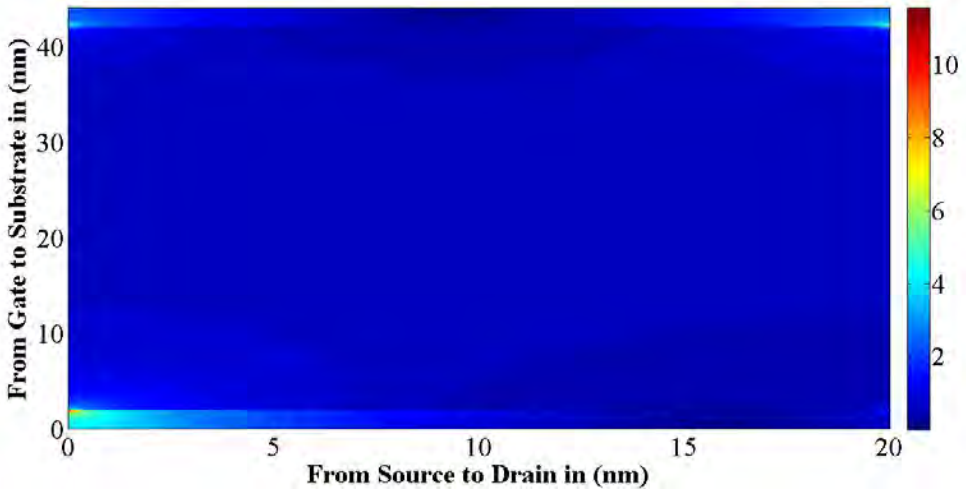

Figure 5.7: Color plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

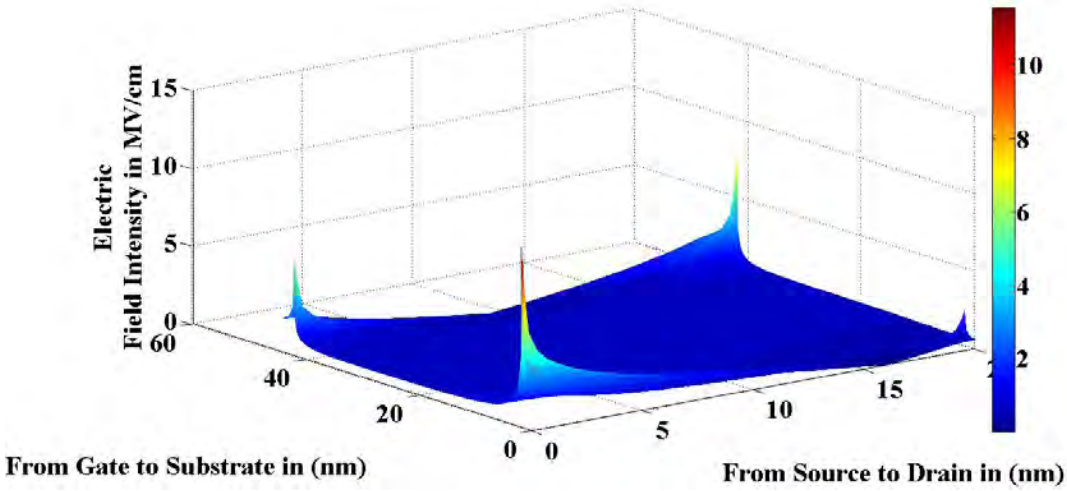

Figure 5.8: Surface plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

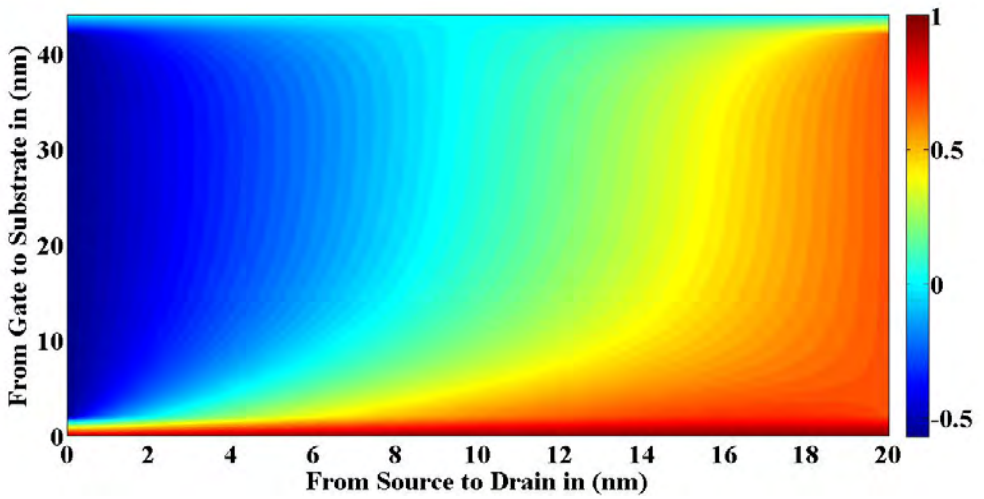

Figure 5.9: Color plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

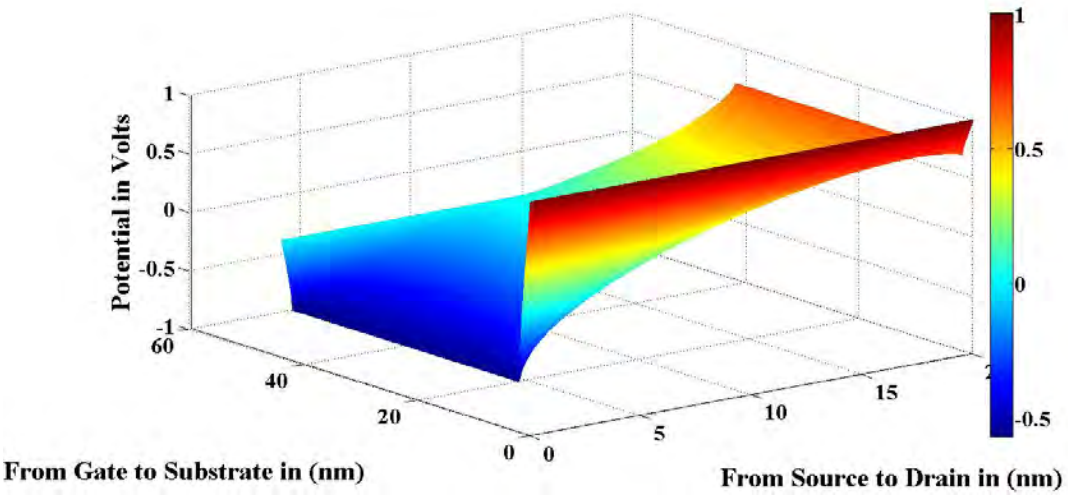

Figure 5.10: Surface plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

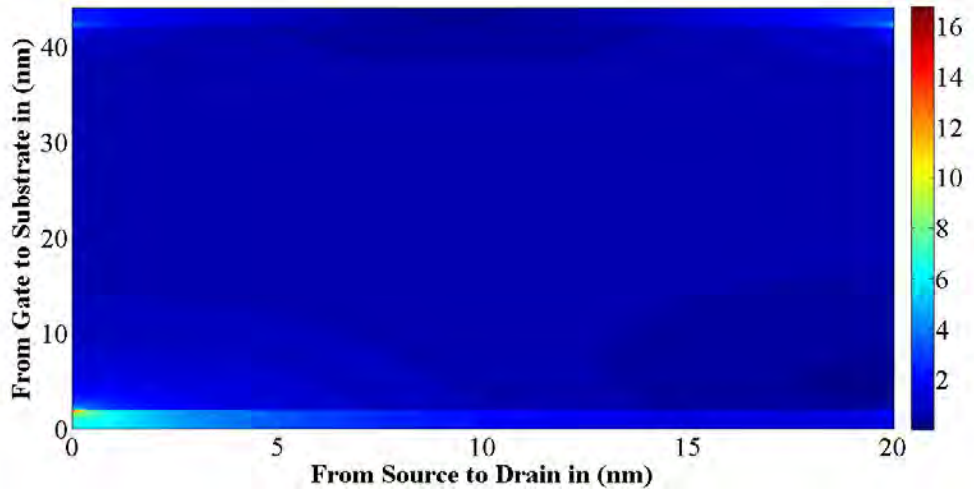

Figure 5.11: Color plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

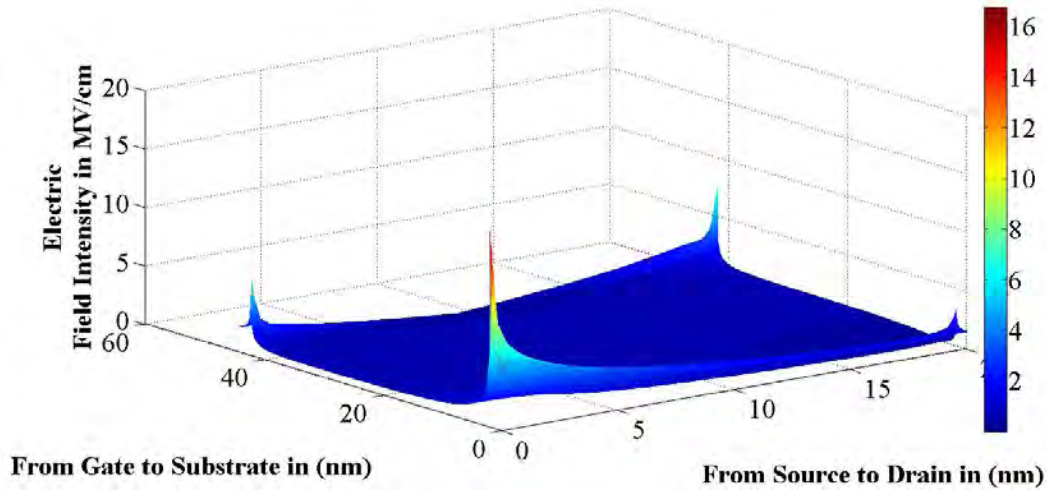

Figure 5.12: Surface plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained from COMSOL simulation

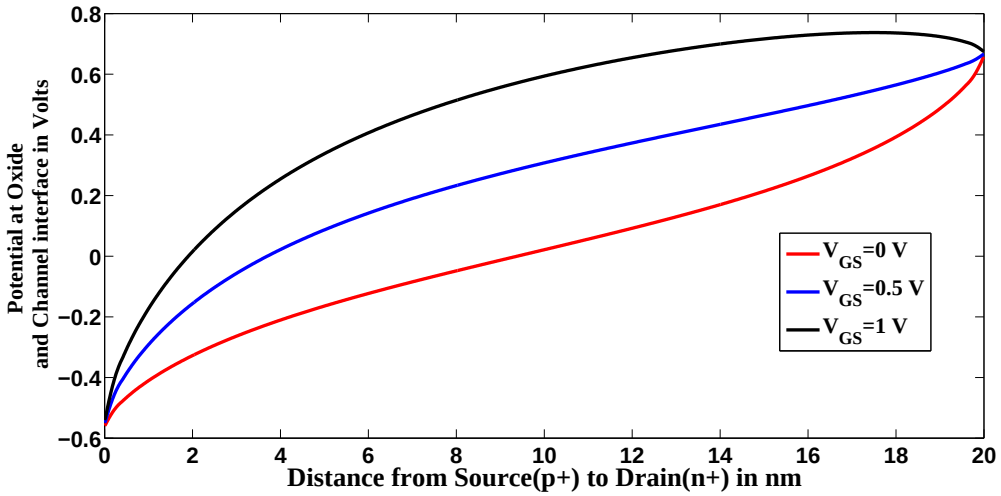

Figure 5.13: Surface potential profiles with variation of V_{GS} at $V_{DS} = 0.1V$ obtained via COMSOL simulation

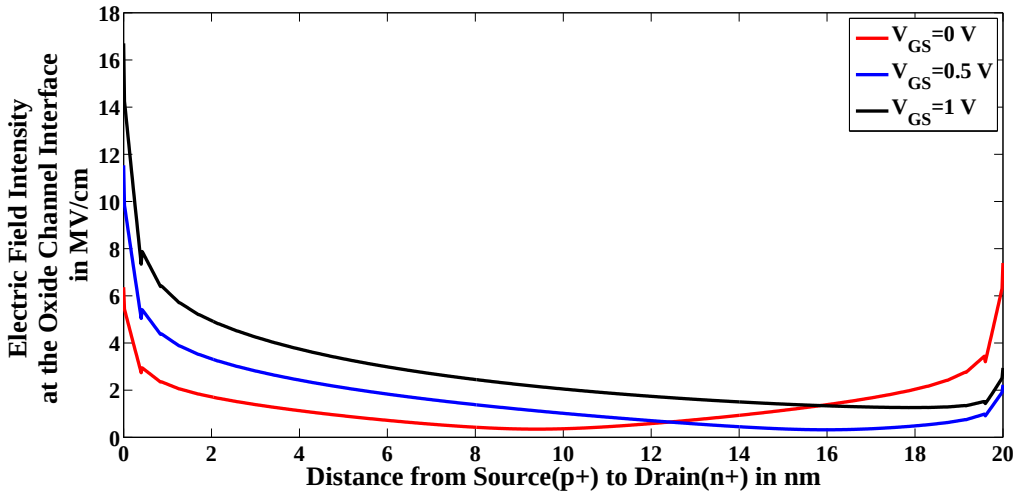

Figure 5.14: Electric field intensity at front oxide/channel interface with variation of V_{GS} at $V_{DS} = 0.1V$ obtained via COMSOL simulation

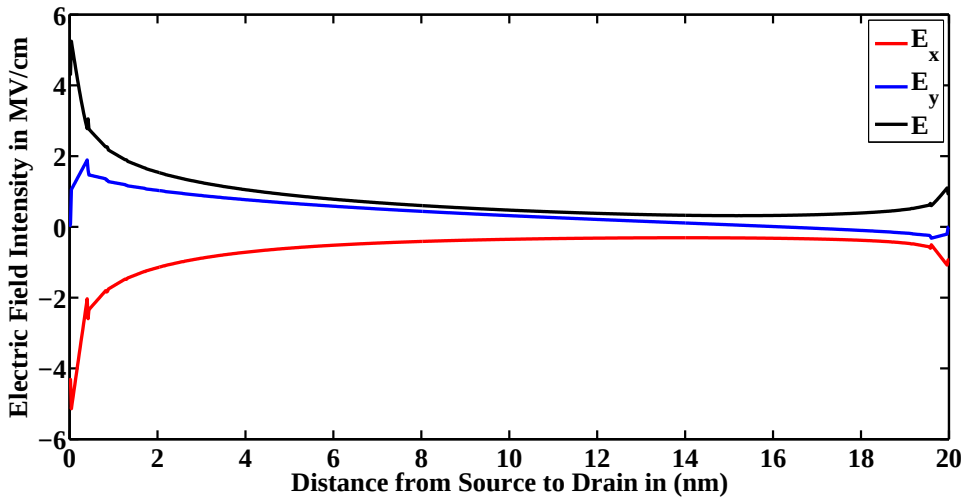

Figure 5.15: Electric field intensity and it's horizontal and vertical components at front oxide/channel interface with $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via COMSOL simulation

5.2 Analytical Model Results

In this section, the same results as that of the previous section has been presented. But in this case the results have been obtained from the analytical model developed. Fig. 5.16, 5.17, 5.20, 5.21, 5.24 and 5.25 show the two dimensional color and surface plot of channel electrostatic potential for different gate voltage (namely, $V_{GS} = 0V,\ 0.5V,\ 1V$) obtained from eqation (3.15), (3.33) and (3.43). Similar to COMSOL simulations, these figures show that higher gate voltage yields greater curvature (see Fig. 5.28) in the channel potential profile. Fig. 5.18,5.19,5.22,5.23,5.26 and 5.27 portray the two dimensional color and surface plot of channel electric field intensity for different gate voltages obtained from eqn. (3.61), (3.62) and (3.65). No significant change of electric field is observed in the middle of the channel whereas notable enhancement of electric field is observed at the oxide channel and source intersection point(see Fig. 5.29) which is consistent with COMSOL simulations presented in the previous section. Fig. 5.30 exhibits the horizontal and vertical component of electric field for a particular gate voltage.

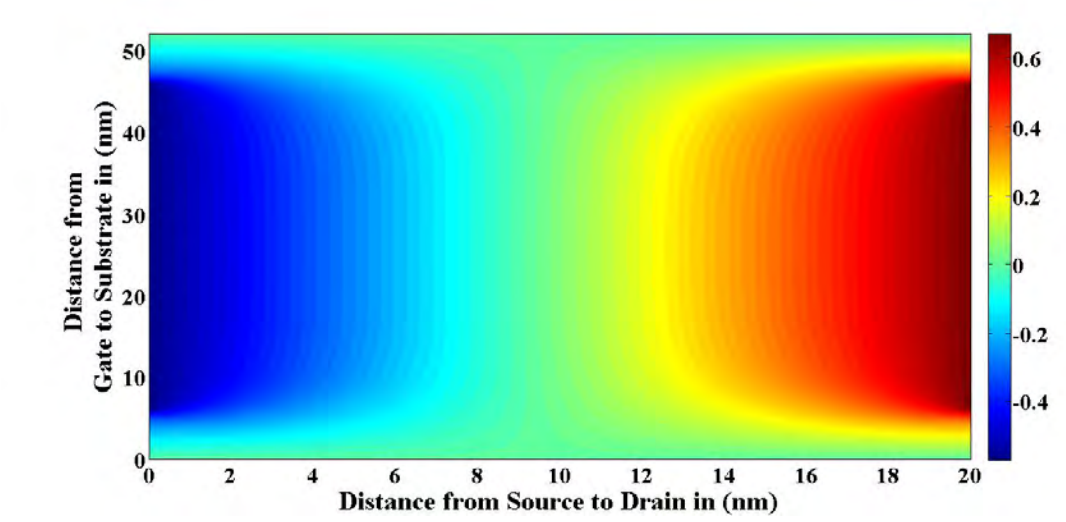

Figure 5.16: Color plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained via analytical model

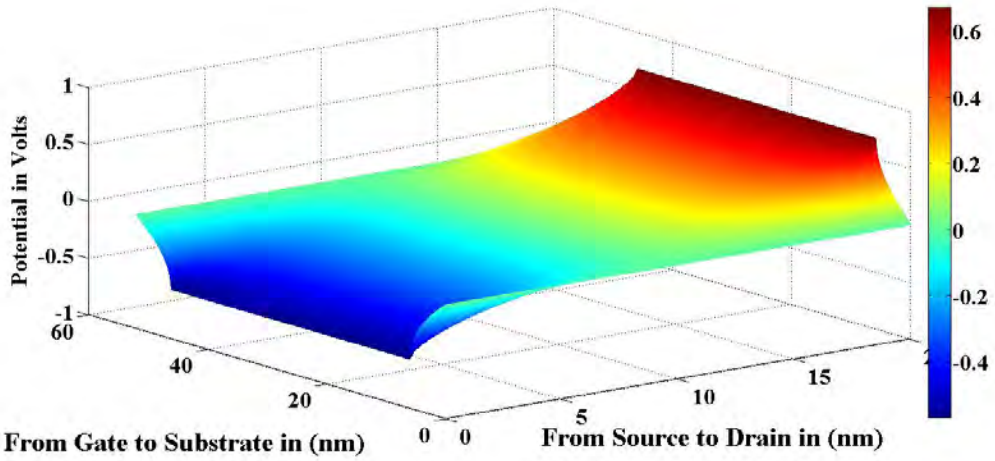

Figure 5.17: Surface plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained via analytical model

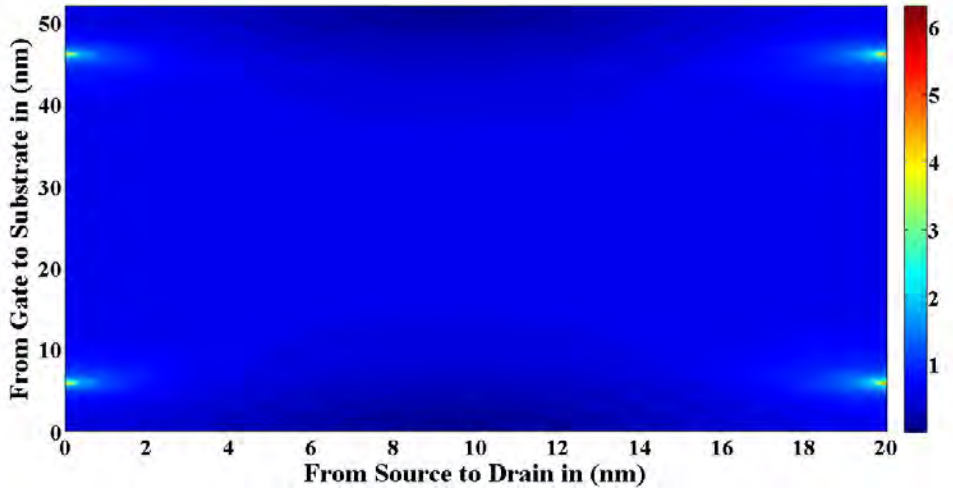

Figure 5.18: Color plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained via analytical model

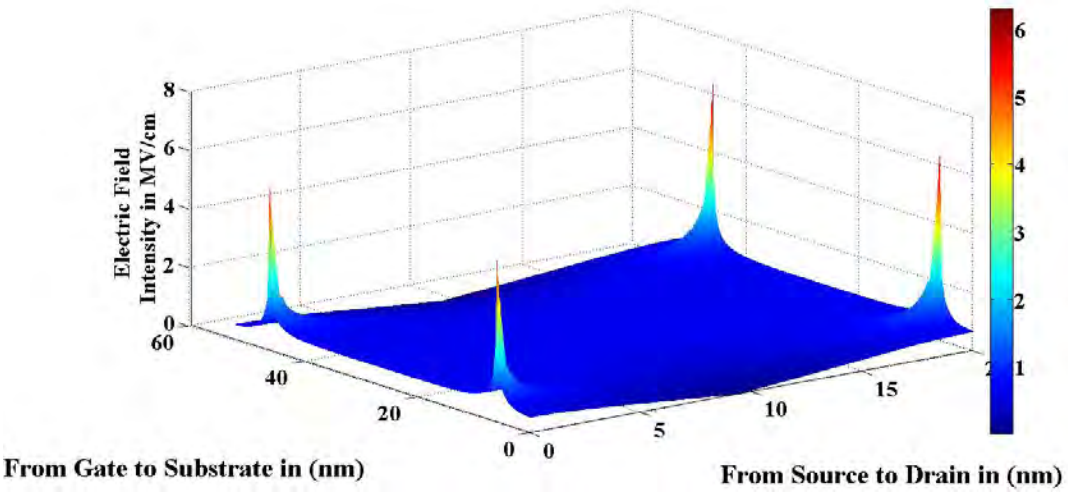

Figure 5.19: Surface plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0V$ and $V_{DS} = 0.1V$ obtained via analytical model

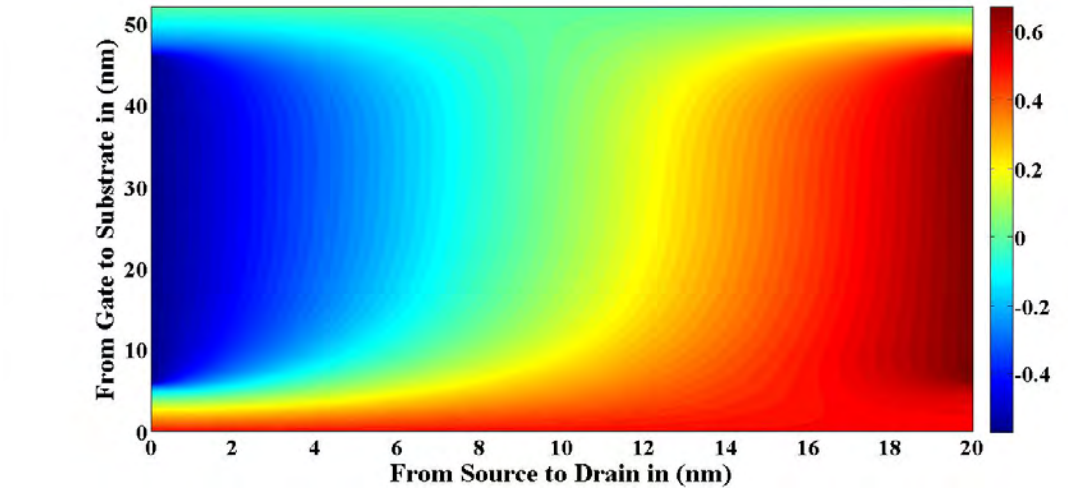

Figure 5.20: Color plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via analytical model

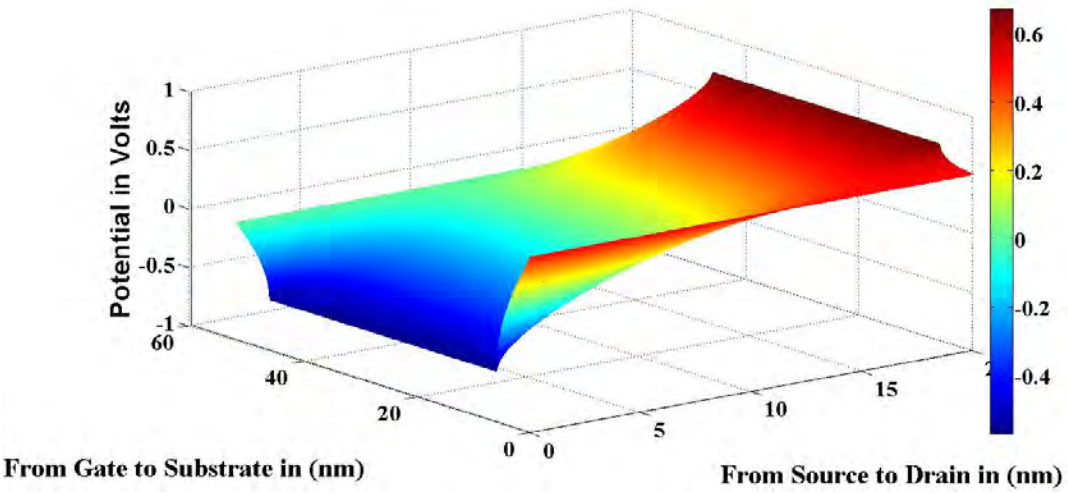

Figure 5.21: Surface plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via analytical model

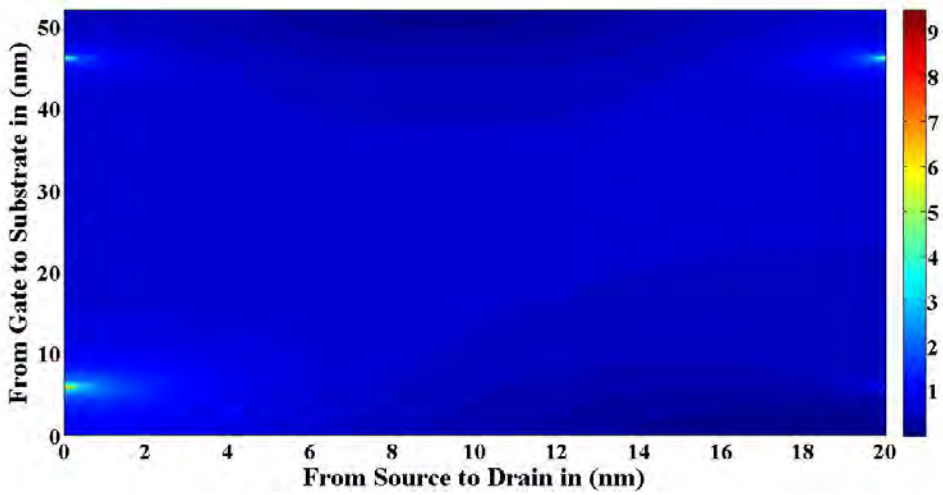

Figure 5.22: Color plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via analytical model

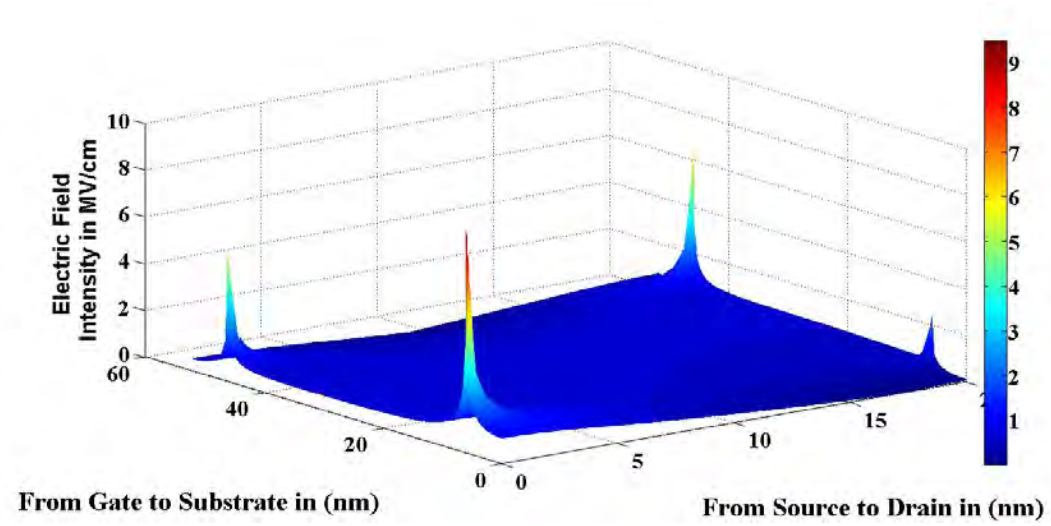

Figure 5.23: Surface plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via analytical model

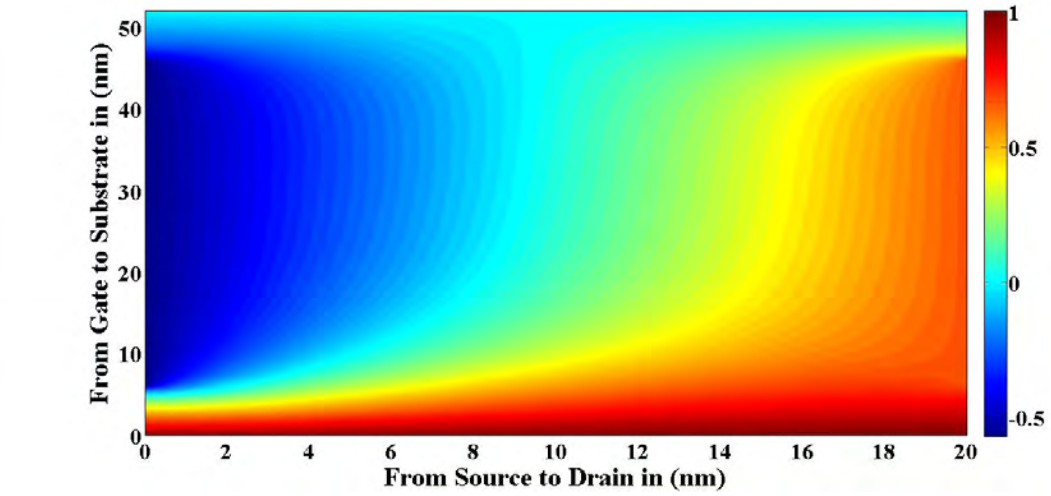

Figure 5.24: Color plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained via analytical model

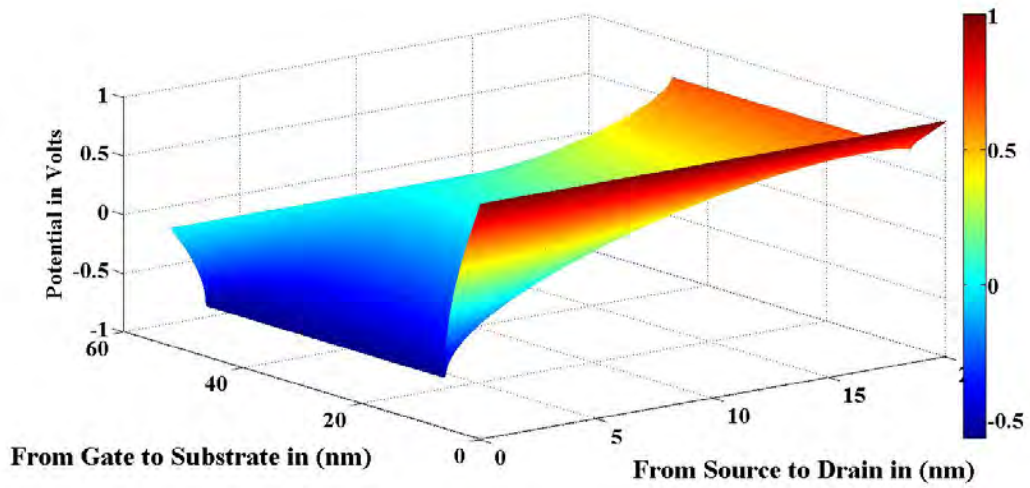

Figure 5.25: Surface plot of two dimensional electrostatic potential distribution in the oxide, channel and buried oxide region (in volts) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained via analytical model

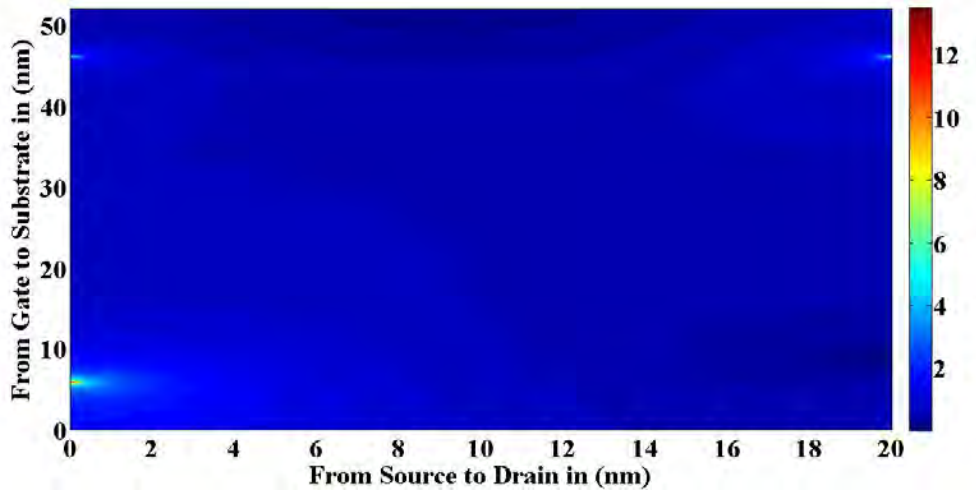

Figure 5.26: Color plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained via analytical model

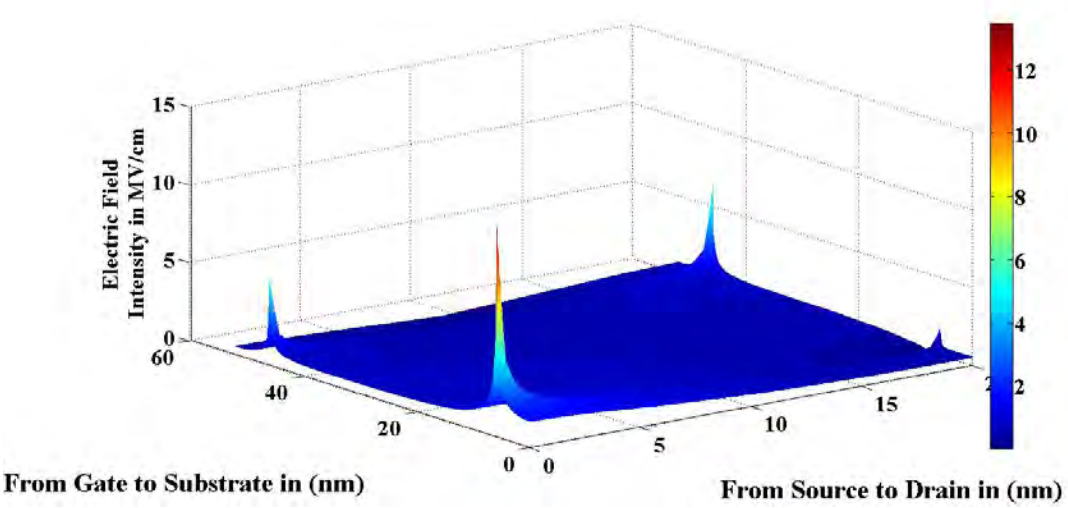

Figure 5.27: Surface plot of two dimensional electric field intensity distribution in the oxide, channel and buried oxide region (in MV/cm) at $V_{GS} = 1V$ and $V_{DS} = 0.1V$ obtained via analytical model

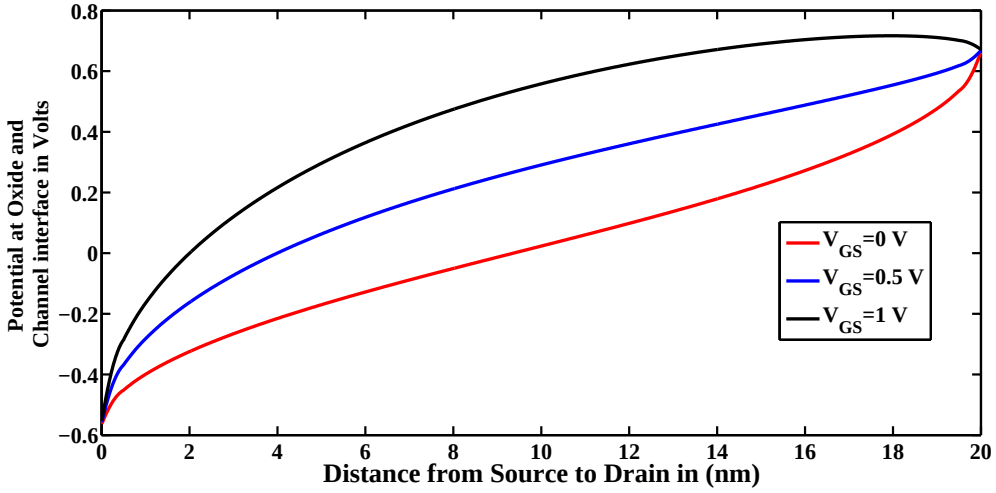

Figure 5.28: Surface potential profiles with variation of V_{GS} at $V_{DS} = 0.1V$ obtained via analytical model

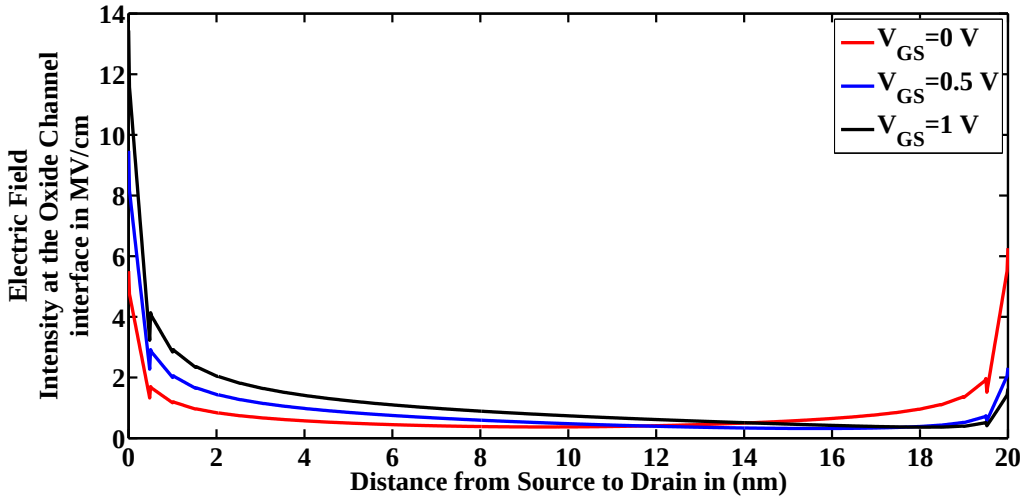

Figure 5.29: Electric field intensity at front oxide/channel interface with variation of V_{GS} at $V_{DS} = 0.1V$ obtained via analytical model

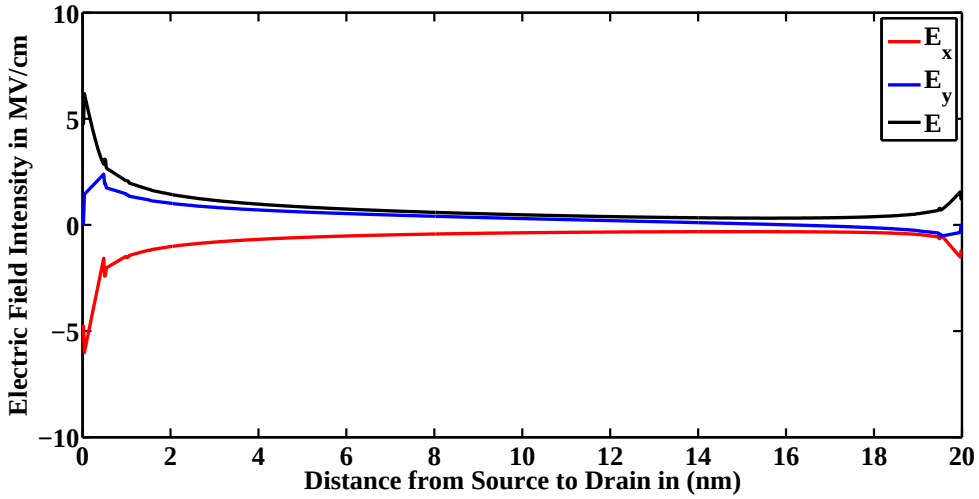

Figure 5.30: Electric field intensity and it's horizontal(E_x) and vertical(E_y) components at front oxide/channel interface with $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via analytical model

5.3 TCAD Simulation Results

In order for further verification of the developed analytical model a TCAD device simulation model has also been developed in SILVACO ATLAS to simulate the $I_D - V_G$ characteristics of SG SOI TFET. The parameters used for simulation is shown in Table 5.2.

Table 5.2: Values of various device parameters used in TCAD simulation

Parameter description	**Symbol**	**Value**
Channel Length	L_c	20 nm
Channel Width	W_{ch}	1 μ m
Channel Thickness	T_C	40 nm
Oxide Thickness	T_{ox}	2 nm
Buried Oxide Thickness	T_{box}	2 nm
Source Length	L_{source}	40 nm
Drain Length	L_{drain}	40 nm
Channel Doping	N_{ch}	10^{16} cm^{-3} n type
Source Doping	N_{source}	10^{19} cm^{-3} p type
Drain Doping	N_{drain}	10^{19} cm^{-3} n type

Fig. 5.31 and 5.32 exhibits the variation potential profile and electric field intensity respectively, along the horizontal direction. Electron energy band diagrams along the horizontal and vertical direction of the channel are shown in Fig. 5.33 and 5.34 respectively.

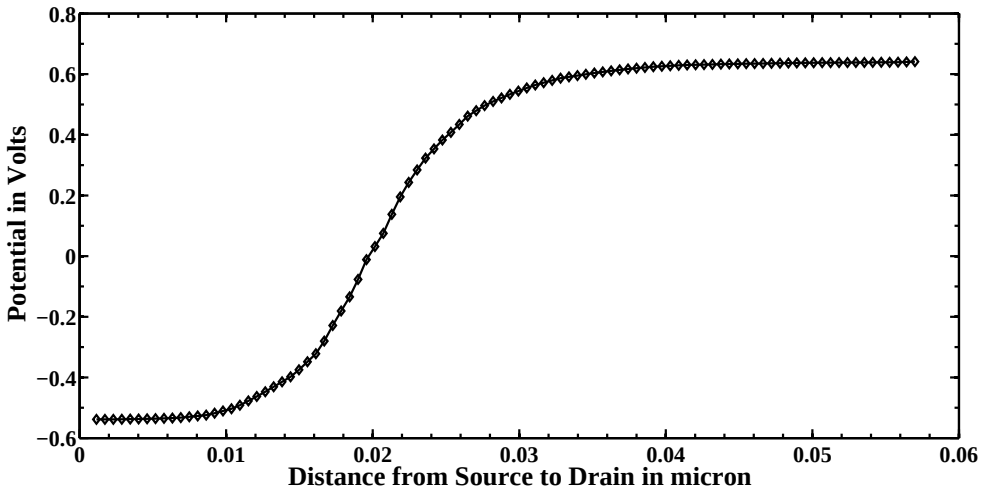

Figure 5.31: Potential along the horizontal direction from source to drain with $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via TCAD simulation.

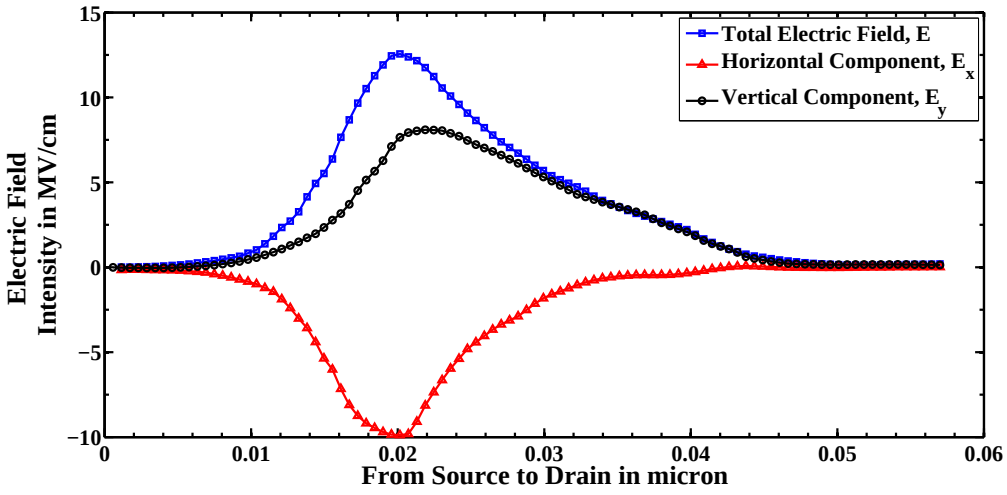

Figure 5.32: Electric field intensity(E) and its horizontal (E_x) and vertical component (E_y) along the horizontal direction from source to drain with $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$ obtained via TCAD simulation.

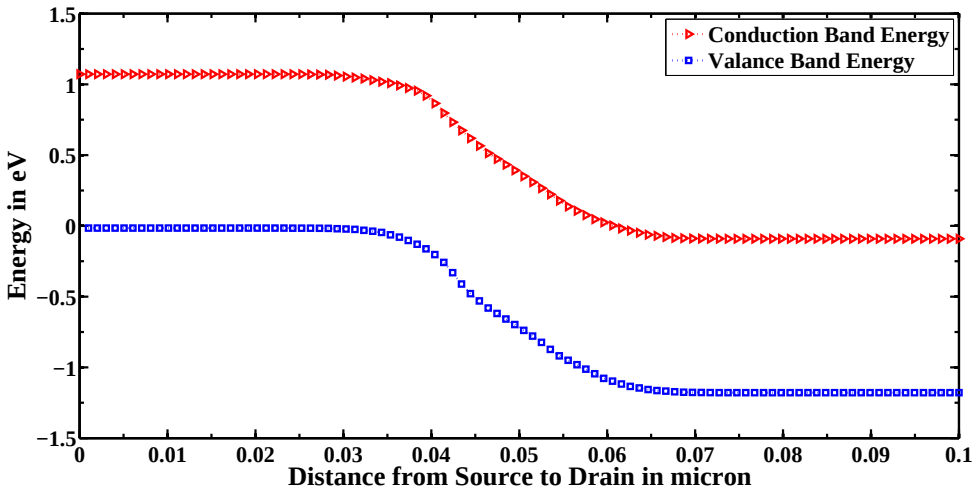

Figure 5.33: Electron energy band diagram along the horizontal direction from source to drain obtained via TCAD simulation.

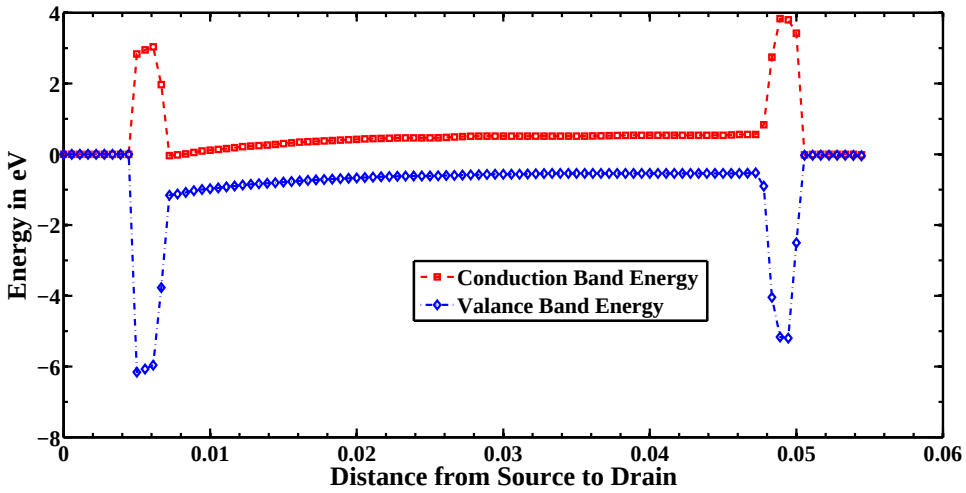

Figure 5.34: Electron energy band diagram along the vertical direction from gate to substrate obtained via TCAD simulation.

5.4 Benchmarking of the proposed Model

Validation of any model is necessary to make it acceptable to scientific community. Two fold validation has been performed in this work; firstly the proposed model is compared with COMSOL simulation model and M. J. Lee's model [20] and secondly it is matched with TCAD simulation.

5.4.1 Comparison with COMSOL Simulation Results and Lee's Model [20]

Fig. 5.35, 5.36 and 5.37 show the comparison potential profile obtained from analytical model with that of COMSOL simulation and Lee's Model [20] and Fig. 5.38, 5.39 and 5.40 show the comparisons among electric field intensity obtained from those. In all cases, analytical model show better match with the COMSOL Simulation model than the Lee's Model [20].

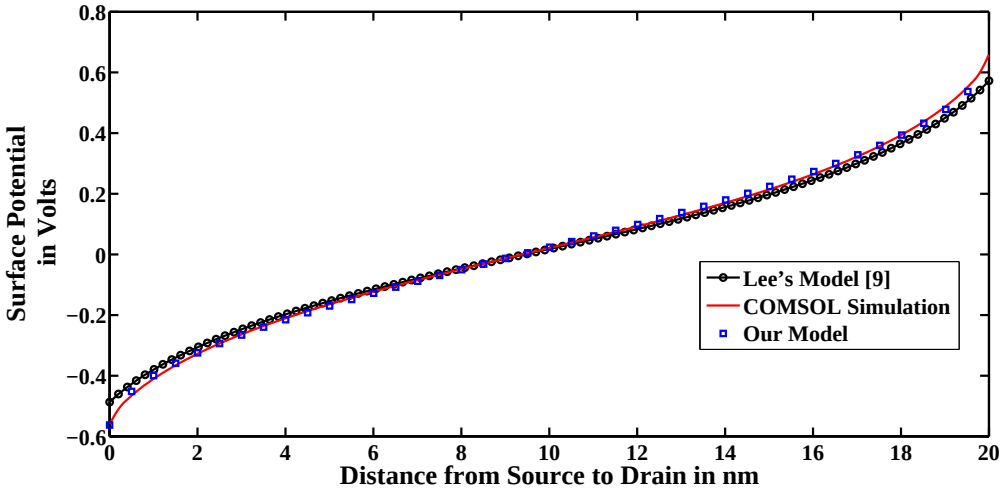

Figure 5.35: Comparison of surface potential with $V_{GS} = 0V$ and $V_{DS} = 0.1V$

Comparison of $I_D - V_G$ characteristics obtained from different is shown in Fig. 5.41. And analytical model shows better agreement with that of COMSOL simulation results than the results obtained from Lee's Model which attributed to the very fact that our model incorporates box voltage drop whereas Lee's model doesn't.

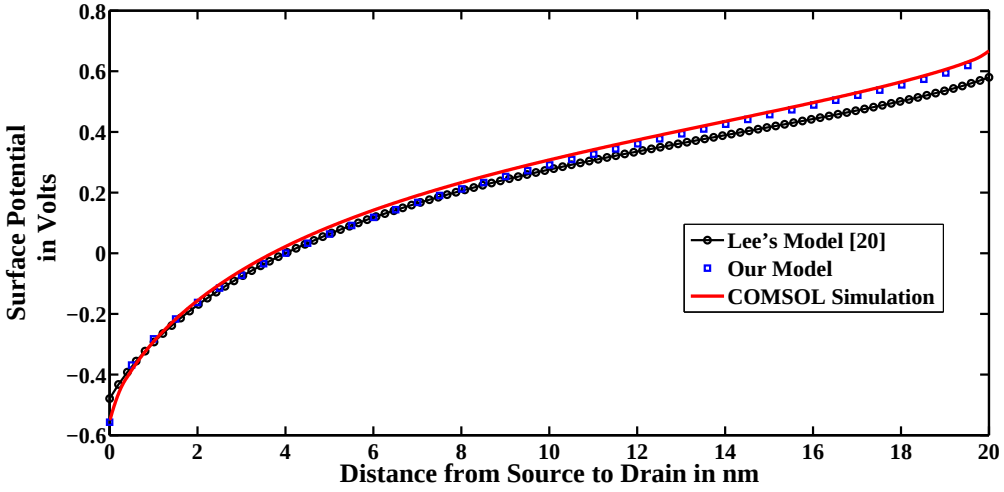

Figure 5.36: Comparison of surface potential with $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$

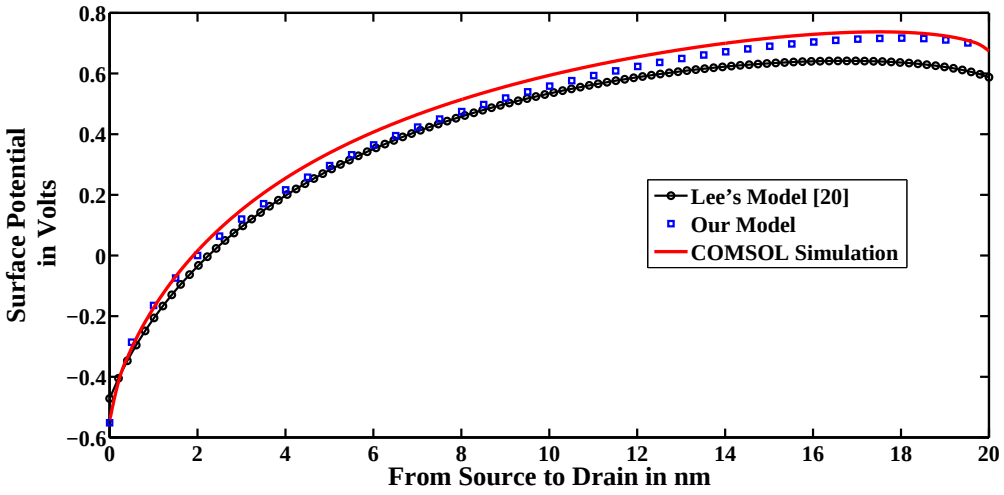

Figure 5.37: Comparison of surface potential with $V_{GS} = 1V$ and $V_{DS} = 0.1V$

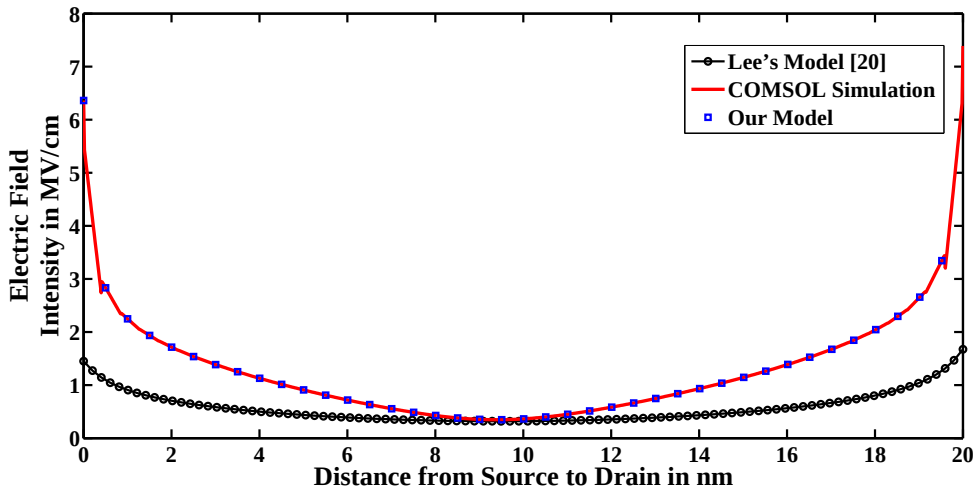

Figure 5.38: Comparison of Electric Field Intensity at the front oxide/channel interface with $V_{GS} = 0V$ and $V_{DS} = 0.1V$

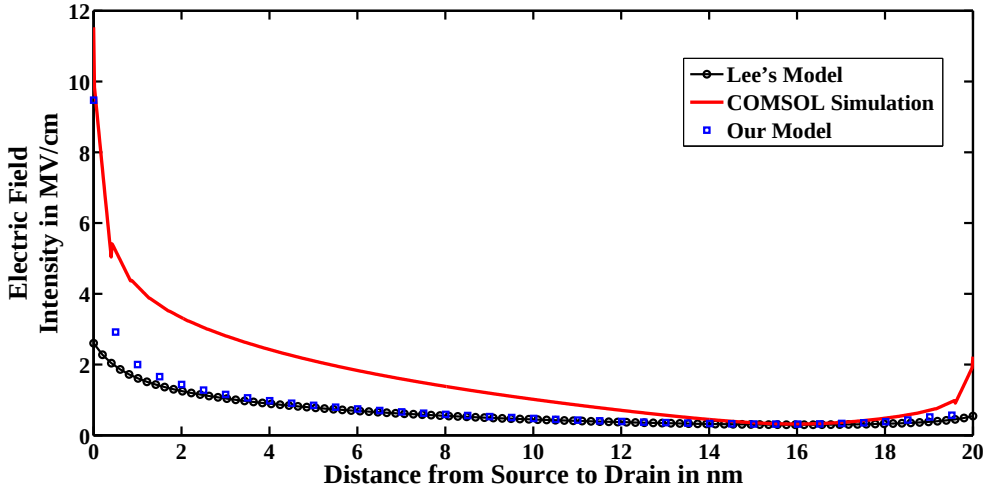

Figure 5.39: Comparison of Electric Field Intensity at the front oxide/channel interface with $V_{GS} = 0.5V$ and $V_{DS} = 0.1V$

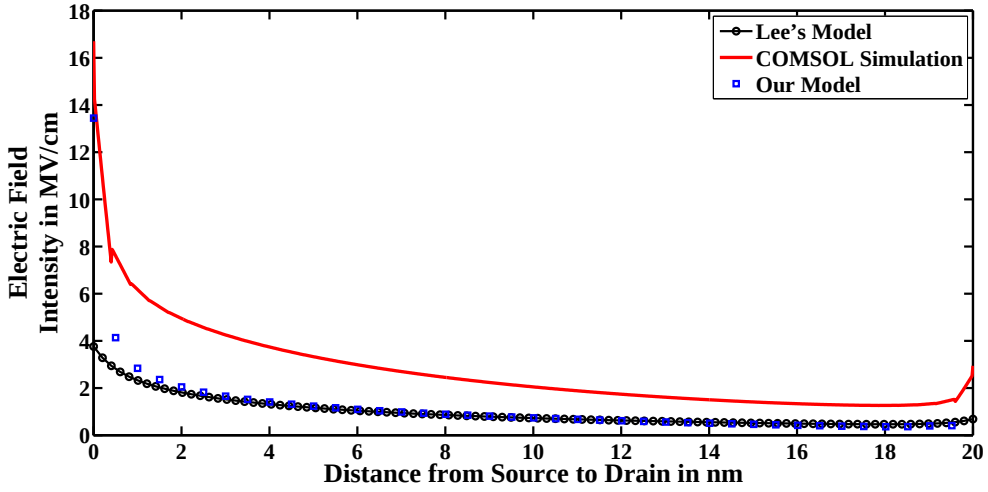

Figure 5.40: Comparison of Electric Field Intensity at the front oxide/channel interface with $V_{GS} = 1V$ and $V_{DS} = 0.1V$

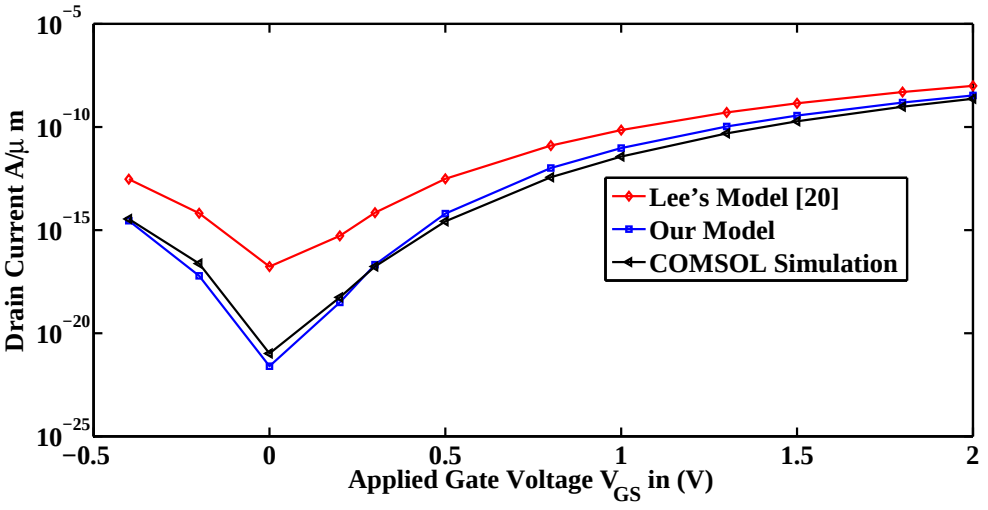

Figure 5.41: Comparison of I_{DS}-V_{GS} characteristics with $V_{DS} = 0.1V$

5.4.2 Comparison with TCAD Results

Since TCAD simulation includes a number of physical effects such as the width of depletion region, SHR which has been overlooked while developing the analytical model; matching with TCAD results need slight calibration of material based parameters such as A, B and D in the Kane's model. Fig.5.42 shows the comparison of calibrated analytical model $I_D - V_G$ characteristics with TCAD $I_D - V_G$ characteristics. It is evident that excellent agreement is obtained between them.

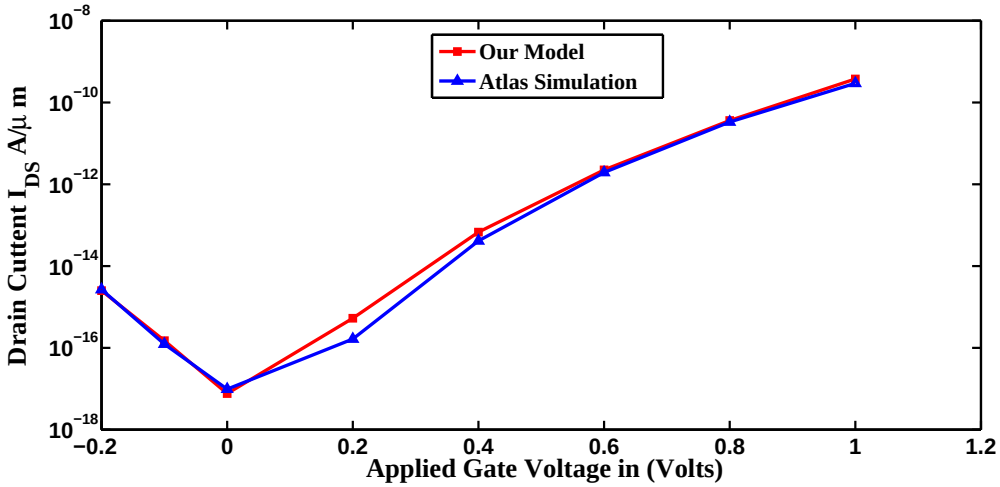

Figure 5.42: Comparison of I_{DS}-V_{GS} characteristics with $V_{DS} = 0.1V$

5.5 Study of Short Channel Effects

Using the analytical model, which includes the effect of drain bias and substrate bias, the short-channel effect of the TFET is studied and compared with that of the MOSFET. While the short-channel effects in MOSFETs are directly related to the phenomenon of drain-induced potential barrier lowering (DIBL), a similar phenomenon called drain-induced barrier thinning (DIBT) exists in the TFET. While the short-channel effects in MOSFETs are directly related to the phenomenon of drain-induced potential barrier lowering (DIBL), a similar phenomenon called drain-induced barrier thinning (DIBT) exists in the TFET. TFETs, the threshold voltage is simply defined as the gate voltage for a specific drain current of $0.1\mu A/\mu m$

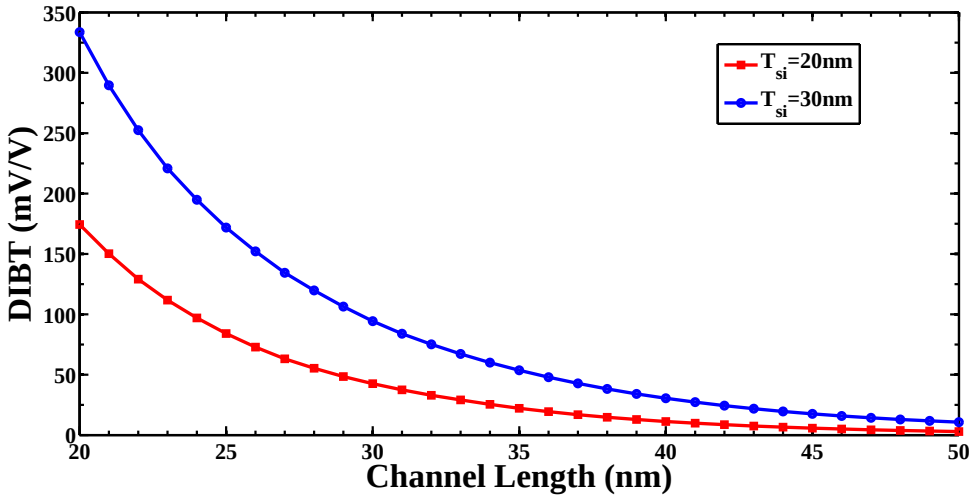

Figure 5.43: Variation DIBT with channel length for different channel thickness

Fig. 5.43 exhibits the variation of DIBT with respect to the variation of channel length. As the channel length is decreased DIBT increases. This is due to the increment of horizontal component of electric field. We know the tunnel barrier for a TFET becomes thinner as the horizontal component of channel electric field gets decreased.

Fig. 5.44 presents the variation of DIBT with channel thickness where we can observe that with the increment of channel thickness DIBT increases. This is due to the fact that contribution of gate bias on channel electric field is reduced and drain bias contribution is enhanced as the channel thickness is increased. Since barrier thinning in TFET largely depends on horizontal electric field and as T_{si} is reduced horizontal component is increased so thus the DIBT.

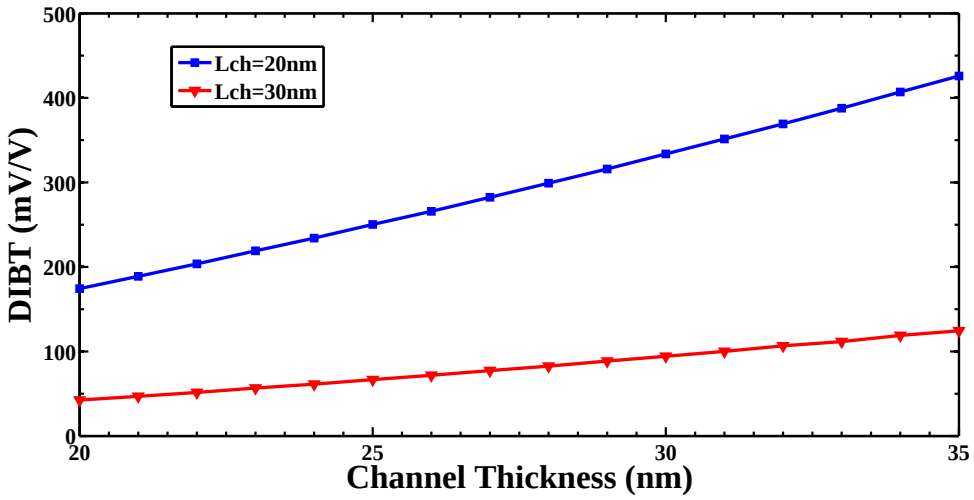

Figure 5.44: Variation of DIBT with channel thickness for different channel length.

5.6 Characterizing NCTFET with the Proposed Model

Nadim *et. el.* [51] combines the physics of Tunnel FET and FeFET to propose a device called Negative Capacitance Tunnel FET (NCTFET) which yields two fold reduction in sub-threshold swing.It presented a 1-D model for NCTFET but here we report a 2-D analytical treatment of the device based on the proposed model. Fig. 5.45 (a) shows the schematic cross section of NCTFET.

Here tunnel current for NCTFET is calculated on the basis of 2D electric field intensity but the impact of Ferroelectric Oxide is incorporated through 1D Landau model [67]. Consider Fig. 5.45 (b) which shows a 1D capacitance model from gate to the substrate terminal. First 2D Poisson's equation is solved in the intrinsic channel region assuming V_{gs} and V_{sub} are the applied voltages at metal 2 and metal 3 respectively. Then 1D Landau model is used to evaluate V_{FE} across the ferroelectric oxide. Fig. 5.46 shows the $I_D - V_{GS}$ characteristics of the NCTFET along with the traditional TFET both obtained through the application of proposed model and it is conspicuous that NCTFET shows better performance than TFET in terms of subthreshold swing.

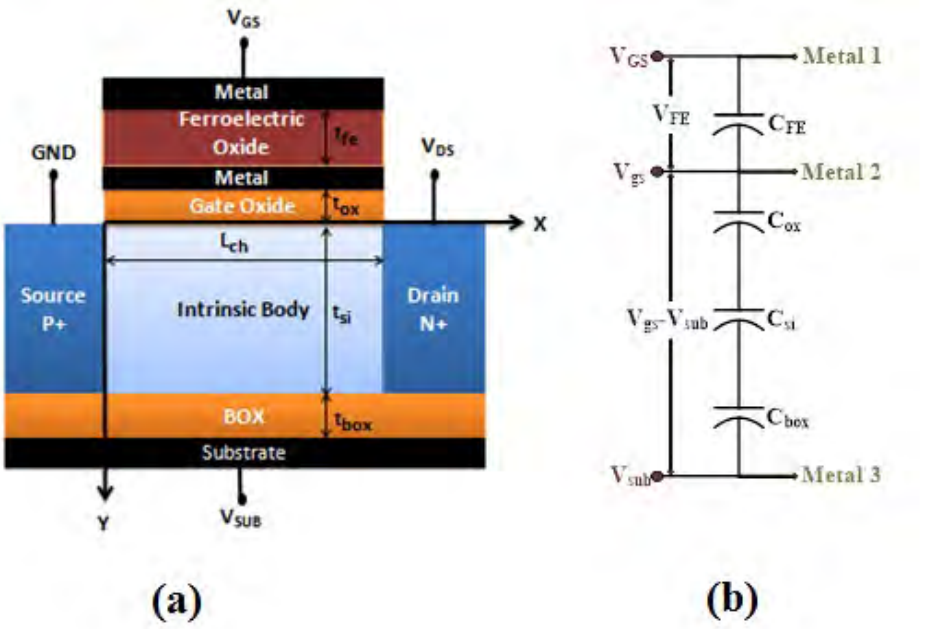

Figure 5.45: (a)Schematic cross-section of the NCTFET (b) 1D capacitance model of NCTFET.

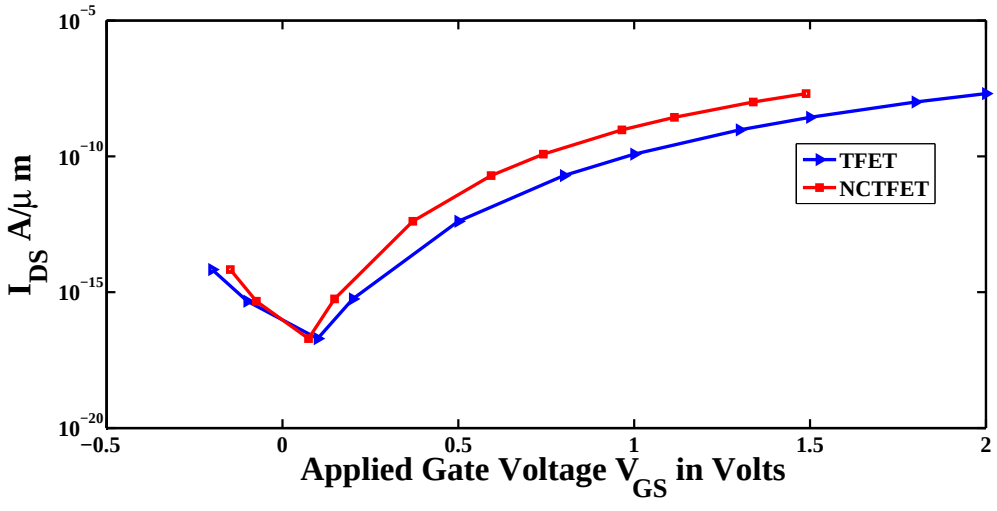

Figure 5.46: $I_D - V_{GS}$ characteristics of NCTFET obtained through application of the proposed model.

6

Conclusion

This chapter succinctly recapitulates the whole work and proposes some unexplored facets of this work which can be put under extensive research.

6.1 Succinct Recapitulation

In this work we have developed a physically based 2-D analytical model for SOI TFET. For modeling TFET the channel electric field distribution is a paramount parameter as it dictates the generation of carrier through band to band tunneling in the channel region. In this work we have shown through numerical simulation that the channel potential and electric field distribution is inherently a 2-D phenomena and any attempt to model it in 1-D would introduce a severe error while anticipating the performance of the device unless some fitting parameters are included in the model. Therefore, in case of TFET 2-D modeling is a must condition for accurate prediction of device performance. Unlike other 2-D models already available in the literature [20], proposed model takes into account the effect of substrate bias. Previous models take 1-D approximations while incorporating the effect of gate and substrate bias in the channel region making their models pseudo-2-D. But in this work we assumed no such approximations and performed complete 2-D analysis for developing the model. The accuracy and applicability of the proposed model has been bolstered through benchmarking of the model results against those of the results obtained from numerical and TCAD simulations. It is well known that [70] in principle Tunnel FET is immune to short channel effects such as DIBT. Based on the analytical model, we also studied the DIBT of the device and verify the previous statement.

The proposed model can be applied to other structures like DG TFET, DMG TFET, NCTFET and Heterojunction TFET with slight or no modifications. Since TFET is a potential candidate for the next generation low power high speed electronics and the proposed model accurately predicts the performance of the device incorporating the effect of substrate bias; so

the work presented here can have huge impact in the upcoming low power computational era as far as the device modeling is concerned.

6.2 Suggestions for future work

1. The effect of source and drain depletion regions can be incorporated in the model to obtain a more accurate one.
2. To simplify mathematical formulation the effect of mobile charge and depletion charge in the channel region are not taken into account. A study can be carried out including the effects of these charges in the channel region.
3. In this work, we have used separation of variable technique to solve 2-D Poisson's equation. Green's function method can also be used to solve Poisson's equation which would yield a different model.
4. Reducing the thickness of the channel below 10 nm will cause the quantization of mobile charges in the channel region which is basically a quantum mechanical effect. Similar study can be carried out incorporating the QM effects in the channel region.
5. The proposed model can be extended for heterojunction Tunnel FETs.

Bibliography

[1] Moore, Gordon E. "Cramming more components onto integrated circuits.".Vol. 38 No. 8, April 19, 1965.

[2] Transistor counts, reported in the International Solid State Circuits Conference.

[3] Mookerjea, S. A. "Band-to-band tunneling field effect transistor for low power logic and memory applications: Design, fabrication and characterization" (Doctoral dissertation, The Pennsylvania State University).(2010).

[4] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," IEEE J.Solid-State Circuits, vol. 25, no. 4, pp. 584-494, April 1990.

[5] T. Ghani, "Challenges and Innovations in Nano CMOS Transistor Scaling," http://microlab.berkeley.edu/text/seminars/slides/TahirGhani.pdf, Nov. 2009.

[6] K. Gopalakrishnan, P. B. GrifiňĄn, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q," in IEDM Tech. Dig., 2002, pp. 289-292

[7] International Technology Roadmap for Semiconductors (ITRS). Available at hppt://www.itrs.net

[8] B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS scaling for high performance and low power-the next 10 years," Proc. IEEE, vol. 85, no.4, pp. 595-606, Apr. 1995.

[9] Gopalakrishnan, K., Griffin, P. B., & Plummer, J. D. "Impact ionization MOS (I-MOS)-Part I: device and circuit simulations.", Electron Devices, IEEE Transactions on, 52(1), 69-76.(2005).

[10] N. Abele, N. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. M. Ionescu, "Suspended-gate MOSFET: Bringing new MEMS functionality into solid-state MOS transistor," in IEDM Tech. Dig., 2005, pp. 1075-1077.

[11] H. Kam, D. T. Lee, R. T. Howe, and T.-J. King, "A new nano-electromechanical field effect transistor (NEMFET) design for low-power electronics," in IEDM Tech. Dig., 2005, pp. 463-466.

[12] Salahuddin, S., & Datta, S. " Use of negative capacitance to provide voltage amplification for low power nanoscale devices.", Nano letters, 8(2), 405-410.(2008).

[13] S. Salahuddin and S. Datta, "Can the subthreshold swing in a classical FET be lowered below $60mV/decade$?," in IEDM Tech. Dig., 2008, pp. 693-696.

[14] Zhang, Q., Zhao, W. & Seabaugh, A. ,"Low-subthreshold-swing tunnel transistors.," IEEE Electron Device Lett. 27, 297-300 (2006).

[15] S. H. Kim, H. Kam, C. Hu and T.-J. King-Liu, "Germanium-Source Tunnel Field Effect transistors with Record High ION/IOFF", Symposium on VLSI Technology Digest of Technical Papers, pp. 178-179, 2009.

[16] Bhuwalka, K. K., Schulze, J., & Eisele, I., "A simulation approach to optimize the electrical parameters of a vertical tunnel FET." IEEE Transactions on Electron Devices, vol. 52, no. 7 (2005): 1541-1547.

[17] Toh, E. H., Wang, G. H., Chan, L., Samudra, G., & Yeo, Y. C., "Device physics and guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction." Applied Physics Letters 91 (2007): 243505.

[18] Verhulst, A. S., Leonelli, D., Rooyackers, R., & Groeseneken, G. "Drain voltage dependent analytical model of tunnel field-effect transistors.", Journal of Applied Physics, 110(2), 024510.(2011)

[19] Bardon, M. G., Neves, H. P., Puers, R., & Van Hoof, C., "Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions", IEEE Transactions on Electron Devices, 57(4), 827-834.(2010)

[20] Lee, M. J., and Choi, W. Y.,"Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs)" Solid-State Electronics, 63(1), 110-114.(2011)

[21] Kane, E. O., "Theory of tunneling." ,Journal of Applied Physics, 32(1), 83-91. (1961)

[22] Keldysh, L. V. ,"Behaviour of Non-Metallic Crystals in Strong Electric Fields.," Soviet Physics: J. Exptl. Theoret. Phys., vol. 33, pp. 994âĂŞ1003, 1957.

[23] Zener, C., "A theory of electrical breakdown of solid dielectrics.," Proc. R. Soc. Lond.ÂăA 145, 523-529 (1934).

[24] Boucart, K. & Ionescu, A. M. ,"Double-gate tunnel FET with high-κ gate dielectric.," IEEE Trans. Electron Devices 54, 1725-1733 (2007).

[25] Wang, P-F., K. Hilsenbeck, Th Nirschl, M. Oswald, Ch Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch. "Complementary tunneling transistor for low power application." Solid-State Electronics 48, no. 12 (2004): 2281-2286.

[26] Seabaugh, A. C. & Zhang, Q., "Low voltage tunnel transistors for beyond CMOS," logic. Proc. IEEE 98, 2095-2110 (2010).

[27] Knoch, J. & Appenzeller, J., "A novel concept for field-effect transistors the tunneling carbon nanotube FET.," Digest Device Res. Conf. 153-156 (IEEE, 2006).

[28] Knoch, J., Mantl, S. & Appenzeller, J. ,"Impact of the dimensionality on the performance of tunneling FETs: bulk versus one-dimensional devices.," Solid- State Electron. 51, 572-578 (2007).

[29] Sze, S. M. Physics of Semiconductor Devices, 1st edn (John Wiley, 1969).

[30] A. M. Ionescu & H. Reil, "Tunnel Field-Effect Transistors as Energy Efficient Electronic Switches," Nature 479, 329 (2011).

[31] Boucart, K. & Ionescu, A. M. ,"Length scaling of the double gate tunnel FET with a high-κ gate dielectric.," Solid State Electron. 51, 1500-1507 (2007).

[32] Sandow, C., Knoch, J., Urban, C., Zhao, Q.-T. & Mantl, S., "Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors.," Solid State Electron. 53, 1126-1129 (2009).

[33] Bhuwalka, K., Schulze, J. & Eisele, I., "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δ p+ layer.," Jpn. J. Appl. Phys. 43, 4073-4078 (2004).

[34] Verhulst, A. S., Vandenberghe, W. G., Maex, K., De Gendt, S., Heyns, M. M., & Groeseneken, G. "Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates." ,IEEE electron device letters, 29(12), 1398-1401.(2008).

[35] Knoch, J. ," Optimizing tunnel FET performance-impact of device structure, transistor dimensions and choice of material.," Int. Symp. VLSI-TSA 45-46 (IEEE, 2009).

[36] Knoch, J. & Appenzeller, J. ,"Modeling of high-performance p-type III-V heterojunction tunnel FETs.," IEEE Electron Device Lett. 31, 305-307 (2010)

[37] Koswatta, S. O., Koester, S. J. & Haensch, W., "On the possibility of obtaining MOSFET-like performance and sub-60-mV/dec swing in 1-D broken-gap tunnel transistors.," IEEE Trans. Electron Devices 57, 3222-3223 (2010).

[38] Hu, C. ,"Green transistor as a solution to the IC power crisis.", Proc. 9th Int. Conf. Solid-State Integrated-Circuit Technol. 16-20 (IEEE, 2008).

[39] Hu, C. et al. ,"Prospect of tunneling green transistor for 0.1 V CMOS.", IEEE Int. Electron Devices Meet. 16.1.1-16.1.4 (IEEE, 2010).

[40] Boucart, K., Ionescu, A. M. & Riess, W., "Asymmetrically strained all-silicon tunnel FETs featuring 1V operation.", Proc. Eur. Solid State Device Res. Conf. 452-456 (IEEE, 2009).

[41] Boucart, K., Riess, W. & Ionescu, A. M. ,"Lateral strain profile as key technology booster for all-silicon tunnel FETs.", IEEE Electron Device Lett. 30, 656-658 (2009).

[42] Mookerjea, S., D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer et al. "Experimental demonstration of 100nm channel length In 0.53 Ga 0.47 As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications." In Electron Devices Meeting (IEDM), 2009 IEEE International, pp. 1-3. IEEE, 2009.

[43] Zhao, H. et al. "InGaAs tunneling field-effect transistors with atomic-layer-deposited gate oxides." IEEE Trans. Electron Devices 58, 2990-2995 (2011).

[44] Mookerjea, S., Mohata, D., Mayer, T., Narayanan V. & Datta, S. ,"Temperature-dependent characteristics of a vertical tunnel FET.", IEEE Electron Device Lett. 31, 564-566 (2010).

[45] Wang, L., Yu, E., Taur Y. & Asbeck, P. ," Design of tunneling field-effect transistors based on staggered heterojunctions for ultralow-power applications.", IEEE Electron Device Lett. 31, 431-433 (2010)

[46] Mohata, Dheeraj, Saurabh Mookerjea, Ashish Agrawal, Yuanyuan Li, Theresa Mayer, Vijaykrishnan Narayanan, Amy Liu, Dmitri Loubychev, Joel Fastenau, and Suman Datta. "Experimental staggered-source and N+ pocket-doped channel III-V tunnel field-effect transistors and their scalabilities." Applied physics express 4, no. 2 (2011): 024105.

[47] Tomioka, K., Motohisa, J., Hara S. & Fukui, T. ,"Control of InAs nanowire growth directions on Si.", Nano Lett. 8, 3475-3480 (2008).

[48] Lu, Y., Seabaugh, A., Fay, P., Koester, S. J., Laux, S. E., Haensch, W., & Koswatta, S. O. ,"Geometry dependent tunnel FET performance-dilemma of electrostatics vs. quantum confinement.", In Device Research Conference (DRC), 2010 (pp. 17-18). IEEE.

[49] Schmid, H., Moselund, K. E., Bjork, M. T., Richter, M., Ghoneim, H., Bessire, C. D., & Riel, H. ,"Fabrication of vertical InAs-Si heterojunction tunnel field effect transistors.", In Device Research Conference (DRC), 2011 69th Annual (pp. 181-182). IEEE, (2011, June).

[50] Ionescu, A. M., Lattanzio, L., Salvatore, G. A., De Michielis, L., Boucart, K., & Bouvet, D. , "The Hysteretic Ferroelectric Tunnel FET ",IEEE Transactions on Electron Devices, 57(12), 3518-3524.(2010)

[51] Nadim Chowdhury, S. M. Farhaduzzaman Azad and Quazi D. M. Khosru,"Negative Capacitance Tunnel Field Effect Transistor: A Novel Device with Low Subthreshold Swing and High on Current", ECS Trans. 2014 58(16): 1-8.

[52] Saurabh, S., & Kumar, M., " Novel attributes of a dual material gate nanoscale tunnel field-effect transistor ", Electron Devices, IEEE Transactions on, 58(2), 404-410.(2011)

[53] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken,"Tunnel field-effect transistor without gate-drain overlap," Appl. Phys. Lett., vol. 91, no. 5, pp. 053 102-1-053 102-3, Jul. 2007.

[54] F. Mayer, C. L. Royer, J. F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, $Si_{1-x}Ge_xOI$ and GeOI substrates on CMOS compatible Tunnel FET performance," in IEDM Tech. Dig., 2008, pp. 1-5.

[55] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and <60 mV/dec subthreshold slope," in IEDM Tech. Dig., Dec. 2008, pp. 1-3.

[56] Appenzeller, J., Lin, Y.-M., Knoch J. & Avouris, P. "Band-to-band tunneling in carbon nanotube field-effect transistors.", Phys. Rev. Lett. 93, 196805 (2004).

[57] Poli, S., Reggiani, S., Gnudi, A., Gnani, E., & Baccarani, G. "Computational study of the ultimate scaling limits of CNT tunneling devices", IEEE Transactions on Electron Devices,, 55(1), 313-321 (2008).

[58] Koswatta, S. O., Lundstrom, M. S. & Nikonov, D. E. ,"Band-to-band tunneling in a carbon nanotube metal-oxide-semiconductor field-effect transistor is dominated by phonon-assisted tunneling.", Nano Lett. 7, 1160-1164 (2007).

[59] Appenzeller, J., Lin, Y.-M., Knoch, J., Chen, Z. & Avouris, P. ,"Comparing carbon nanotube transistors-the ideal choice: a novel tunneling device design.", IEEE Trans. Electron Devices 52, 2568-2576 (2005).

[60] Zhang, Y. et al. "Giant phonon-induced conductance in scanning tunneling spectroscopy of gate-tunable graphene.", Nature Phys. 4, 627-630 (2008).

[61] Luisier, M. & Klimeck, G. ,"Performance limitations of graphene nano ribbon tunneling FETS due to line edge roughness.", IEEE Device Res. Conf. 201-202 (IEEE, 2009).

[62] Fiori, G. & Iannaccone, G., "Ultralow-voltage bilayer graphene tunnel FET.", IEEE Electron Device Lett. 30, 1096-1098 (2009)

[63] Woo, J. C., Terrill, K. W., and Vasudev, P. K., "Two-dimensional analytic modeling of very thin SOI MOSFETs", IEEE Transactions on Electron Devices, 37(9), 1999-2006.(1990)

[64] Liang, X., and Taur, Y.,"A 2-D analytical solution for SCEs in DG MOSFETs", IEEE Transactions on Electron Devices,51(9), 1385-1391.(2004)

[65] Atlas User's Manual, Silvaco Int, Santa Clara, CA, April 20, 2010

[66] www.comsol.com

[67] L. D. Landau and I. M. Khalatnikov, "On the anomalous absorption of sound near a second order phase transition point", Dok. Akad. Nauk, SSSR, vol. 96, pp. 469-472, Jun, (1954).

[68] Shen, C., Ong, S. L., Heng, C. H., Samudra, G., & Yeo, Y. C.," A variational approach to the two-dimensional nonlinear Poisson's equation for the modeling of tunneling transistors", Electron Device Letters, IEEE, 29(11), 1252-1255.(2008)

[69] Rajamohanan, B., Mohata, D., Ali, A., & Datta, S., "Insight into the output characteristics of III-V tunneling field effect transistors", Applied Physics Letters, 102, 092105.(2013)

[70] Liu, L., Mohata, D., & Datta, S."Scaling length theory of double-gate interband tunnel field-effect transistors" Electron Devices, IEEE Transactions on, 59(4), 902-908.(2012)

[71] Bhushan, B., Nayak, K., & Rao, V.,"DC Compact Model for SOI Tunnel Field-Effect Transistors",IEEE Transactions on Electron Devices,59(10), 2635-2644.(2012)