International Islamic University Chittagong
Department of Electrical and Electronic Engineering

Final Examination Spring-2019
Course Code: EEE-2407
Time: 2 hours 30 minutes

Program: B.Sc. Engg. (EEE)
Course Title: Digital Electronics
Full Marks: 50

Part A

[Answer any ***two*** questions from the followings;figures in the right margin indicate full marks.]

1(a). What are the differences between combinational circuit and sequential circuit? What are the procedures to design a combinational circuit? **3**

1(b). Design a 4 bit magnitude comparator. **5**

1(c). Construct a BCD to Excess-3 code converter. **2**

2(a). Design a 1x4 de-multiplexer using basic logic gates only. **3**

2(b). Implement a full adder with a decoder and two or gates **3**

2(c) Implement the following circuit with multiplexer **4**
$F(A,B,C,D)= \sum(0, 1, 3,4,8,9,15)$.

3(a). Design a binary to octal decoder. **4**

3(b). Design a 4 bit binary parallel adder and also explain a technique for reducing carry propagation time. **4**

3(c). Design the following function with a 4x16 decoder IC: **2**
$F(A,B,C,D) = \sum (1,3,4,5,6,7,8,12,15)$

Part B

[Answer any ***three*** questions from the followings; figures in the right margin indicate full marks.]

4(a). Design the sequential circuit for the following state diagram with J-K flip-flops. **8**

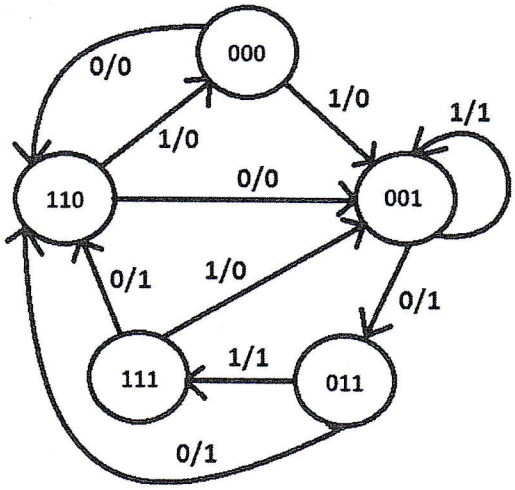

Fig:1

4(b). Determine the flip-flop inputs of a 3-bit counter if it is to be designed with a 'T' flip-flop. **2**

5(a). Design a decade counter. **4**

5(b). Following is an Asynchronous counter. What is its MOD number? Prove that it is a Up counter from its timing diagram. **5**

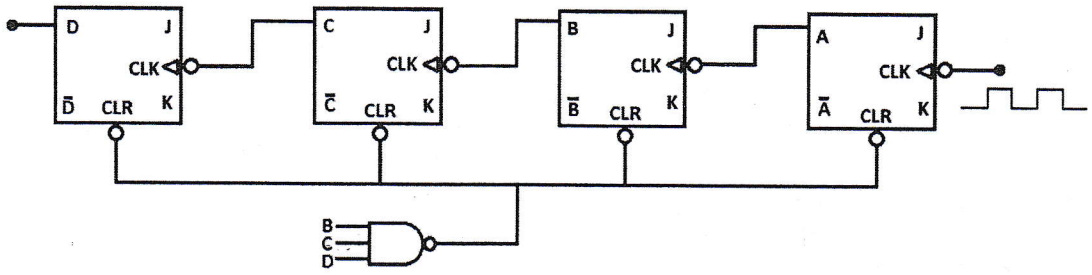

Fig:2

5(c). What is propagation delay? **1**

6(a). Design a 10 bit ring counter and also draw sequence table. **4**

6(b). Design a 4 bit bidirectional shift register and explain its operation. **6**

7(a). Derive the state table and state diagram of the sequential circuit in fig.3 **3**

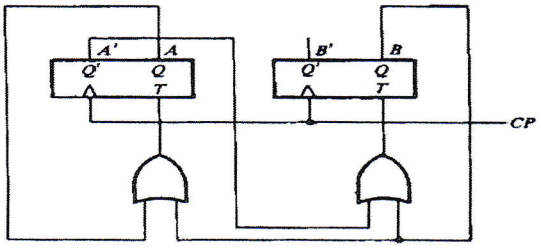

Fig.3

7(b). Reduce the state of the following state table and draw the reduced state table and state diagram. **4**

Present State	Next state		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

7(c). Design a 3 bit parallel in serial out shift register. **3**