" STUDY OF SOME COMMERCIALLY FABRICATED SEMICONDUCTOR P-N JUNCTION CHARACTERISTICS AND CHARACTERIZATION OF IMPURITY LEVELS PRESENT THEREIN "

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ABSTRACT

The object of present work has been to study junction properties of some commercially available diodes and transistors. We studied over fifty samples out of which twenty were analyzed in details and are reported here. To study the property of depletion layer of p-n junction we carried out a detail C-V measurement. From this study junction capacitance, depletion width, contact potential etc. have been evaluated. From I-V studies (for forward bias and reverse bias conditions) efficiency factor η has been estimated for large numbers of diodes. These studies indicate the presence of deep impurity centers in most of the samples.

To confirm this we carried out detail investigation to detect defect states, if any, and characterized the defect states whenever found. We have observed the presence many and varied deep states both in Si and Ge. The methods used for characterizing the states are TSCAP and TSC.

In carrying out the investigation we have to construct fixed and variable temperature system, a constant temperature bath and many electronic circuitry needed for our experiments.

INTRODUCTION

The work reported here constitutes an investigation of some commercially fabricated p-n junctions made of widely used semiconductors like Si, Ge and GaAs. Most of the devices are in the form of diodes although some are transistors. The samples are commercially available. Some are obtained particularly, GaAs ones, through the courtesy of a University professor working in an American University, and two samples of GaAs were fabricated in a Swedish laboratory. The purpose of the study is to look into the electrical behavior of these devices critically and to examine how the behaviour of the devices compare with the expected behavior predicted by the ideal diode law. As we know the ideal law is given by the Shockley equation[6] i.e. the current density follows an exponential law when a diode is operated under an external voltage V

$$J = J_s\left[e^{qv/kT} - 1\right].$$

This elegant but simple law is however, not adequate to explain the behavior of a practical diode. The departures from the ideal behavior, as we understand, are mainly due to series resistance effect, presence of surface states, generation and recombination of carriers in the depletion region. Apart from the above stated factors, the behavior of a diode may also be affected by the tunneling of carriers between states in the band gap -

which in some cases (eg. in GaAs) may cause a tunneling current component.[37]

However, most important factor that modifies the electrical, optical and, in some cases, magnetic properties of a semiconductor is the presence of impurity centers and defect states lying within the forbidden energy gap. The presence of the impurity centers not only changes the physical properties of the bulk material, its presence generally influences the junction behavior of the devices made of such semiconductor materials. The impurities in some case may be added intentionally for some specific purpose. However, in the commercially fabricated diodes the impurities get in via the very fabrication method.

As we know the fabrication technology i.e. junction fabrication method mainly are of three types: (i) the so called alloy method, (ii) the solid state diffusion method and (iii) epitaxial. The solid state diffusion gives a better control over impurity concentration whereas the epitaxial method reduces considerably the series resistance effect. But the very growth of single crystal may introduce impurities and defect states. As for example, oxygen gets in a quartz-crucible grown silicon, and if this material is heated to a higher temperature (> 400°C) the resistivity changes because donor centers are formed. Iron is another example which may be present in commercially prepared 'Si-single' crystal. Iron is a fast diffusing element in silicon.

In order to prevent contamination with iron, a very clean production process is necessary and successive heat treatment may be effective. But in spite of such precaution Si-devices may contain some iron impurities. The metallic impurities not only influence the electrical property of the material or the devices made out of it, but another disadvantage is that their precipitates act as a dislocation sources if stresses are present in the substrate. Another most common metallic impurity is Cu. Ge is another widely used semiconductor in device technology. Most of the monovalent metals create impurity centres in Ge. Cu introduces 3 acceptor levels (0.04 ev, 0.33 ev both above Ev, and 0.26 ev below Ec). When Fe is present as impurity it creates two acceptor levels 0.25 ev above Ev and 0.30 ev below Ec. Presence of oxygen introduces donor levels 0.04 ev and 0.20 ev below Ec. S and Se create donor levels near the conduction band, 0.18 ev and 0.14 ev below Ec respectively.

The technique of preparation of crystals of GaAs and some other III-V compound semiconductors have been greatly improved recently. Most of the impurities used to create energy levels deep in the energy gap. In some instants impurity pairing, or interaction with native defects, occurs and produces unexpected additions to the energy level structure.

Epitaxial growth processes with GaAs are becoming increasingly important for creating device structures that can not be achieved by conventional diffusion and alloying process. Some

of these processes involve the possibility of undesirable doping by deep impurities or cause levels associated with native defects. As for example, two unknown but commonly occurring defects in GaAs are found when it is grown by liquid phase epitaxy (LPE) and are popularly known as A and B centres. GaAs structures and devices after fabrication usually show trapping effects, caused by the deep levels and defect levels. The most common deep centres attributed to Cu are 0.14 ev (acceptor level), 0.44 ev, 0.24 ev above E_v. Another level 0.6 ev below E_c is also attributed to Cu. Oxygen is a deep donor 0.75 ev below E_c. It is assumed that Fe is responsible for the presence of a level 0.37 ev and 0.52 ev acceptor levels.

In order to see the behavior of practical p-n junction diodes, we studied a large number diodes made of Si, Ge and GaAs. The I-V (both forward and reverse bias) and C-V characteristics have been thoroughly investigated. From I-V measurement we calculated η-factor that is usually assigned in the modified Shockley equation to describe diode current, cutin voltage (V_γ), and forward resistance (R_f). From C-V measurement we estimated contact potential (V_o), intrinsic depletion capacitance (C_o), and doping concentration (N_B).

From the above discussion it appears that study of presence of impurity in commercial diodes needs no elucidation. In order to detect deep impurity in such diodes we followed two methods --

both of which is based on the transient response phenomenon. The first one is the so called "Thermally Stimulated Capacitance technique" wherein the change of depletion capacitance is monitored against a steady rise of temperature, and capacitance steps are obtained because of the presence of deep states. From the observed TSCAP curve. we can estimate ionization energy, trap concentration of the impurity level. In the second method, where in the reverse-saturation current is monitored against the temperature rise under a constant bias, current peaks due to the presence of impurity centers are recorded. The technique is called "Thermally Stimulated Current" measurement. From the TSC curve the same parameters can be evaluated. By using both methods we made an attempt to detect the deep impurity centres present in such devices and their energy levels have been characterized.

The work described here constitutes following main sections:

(i) theoretical discussion and necessary formulation

(ii) Experimental development

(iii) Result of our survey.

In performing the experiments we have to develop some electronics such as dc-power supply units, dc-amplifier, and differential amplifier, constant temperature bath. A fixed low temperature as well as variable temperature cryostatic system has been designed and constructed.

The detail description and analysis of our study follow in the subsequent chapters.

CHAPTER ONE

SEMICONDUCTOR JUNCTION AND ITS PROPERTIES

1.1 P-N JUNCTION:

Allmost all semiconductor devices are comprised of a single-crystal semiconductor incorporating two or more semiconducting regions of different impurity density. The metallurgical boundary between a *p* - region and an *n* - region is called a *p* - *n* junction. The junction is an inherent part of the molecular structure.

The junction formation requires that the material be started as one type and the impurity changed to the other type, forming a molecular transition from *n* to *p* (*p* to *n*). When the junction is formed, a diffusion current immediately flows from one type material to the other - creating an electrostatic potential difference across the junction and this area is termed as transition region. Since the junction region is almost totally devoid of carriers it is also called the depletion region.

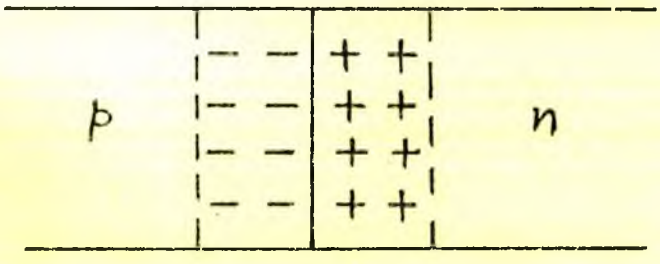


Fig. (1). a p-n junction

1.2. FORMATION OF DEPLETION LAYER AND BARRIER POTENTIAL:

When a single piece of semiconductor material is formed with both types of extrinsic materials, at absolute zero, no current can flow through the material. As the temperature is increased the diffusion phenomenon between the *n* and *p* materials comes to play. Since *p* - side is dominated by holes and *n* - side by electrons there exists a density gredient, holes in *p* - side will diffuse into the *n* side, whereas electrons in *n* -side will diffuse into the *p* - side. An electric field is established by the uncompensated donor and acceptor ions left behind and its presence gradually reduces the diffusion current, until an equilibrium condition is reached.

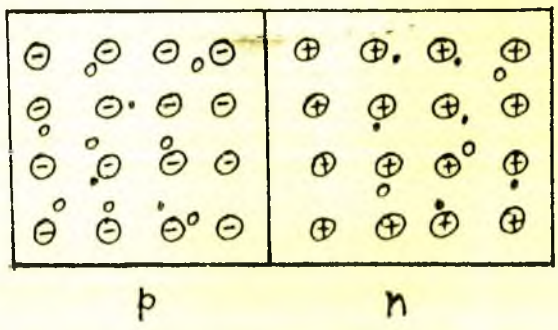


Fig. (2). Depletion layer formation

The junction contact potential or barrier potential[1] can be expressed by Fermi level conception. The Fermi level E_F is closer to conduction band edge E_{cn} in the *n* region and closer to valence

band edge E_{vp} in the p - region. When the contact is made, there would be a transfer of electrons and energy to line up the Fermi - level in two sides. The energy band diagram for a p -n junction therefore should look some-what like as pictured in fig. (3).

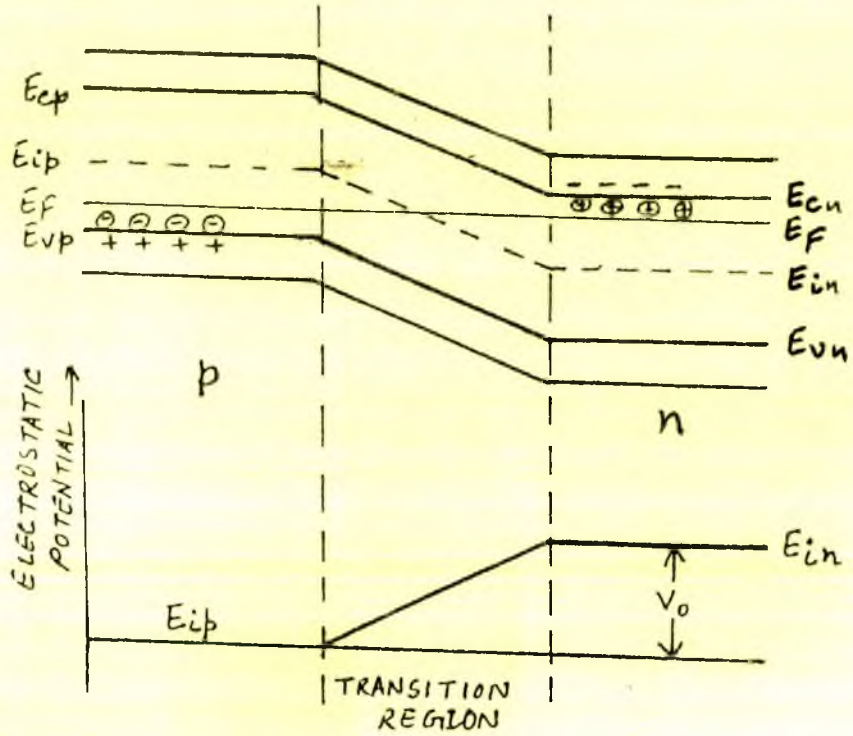


Fig. (3). Band diagram of a p-n junction

Under thermal equilibrium, the electron current density J_n, through the junction is [2]

$$J_n = 0 = q\,\mu_n \left[nE + \frac{KT}{q}\frac{\partial n}{\partial x}\right] \quad \ldots \quad (1.1)$$

We further know that at thermal equilibrium,

$$E_F - E_i = KT \ln \frac{n}{n_i} \quad \ldots \quad (1.2)$$

There are similar equations for holes also. Using all these equations we obtain,the barrier potential energy,

$$E_o = KT \ln \frac{N_a N_d}{n_i^2} \qquad \ldots \qquad (1.3)$$

As $n_n \approx N_d$ and $p_p \approx N_a$ and $n_n p_n = n_p p_p = n_i^2$ equation (1.3) can be written in the form,

$$E_o = KT \ln \frac{p_{po}}{p_{no}} = KT \ln \frac{n_{no}}{n_{po}} \qquad \ldots \qquad (1.4)$$

Here, the subscript 'O ' refers to the condition of thermal equilibrium.

From equation (1.4) we get the contact potential, V_o.

$$E_o = qV_o$$

$$\text{or } V_o = \left(\frac{KT}{q}\right) \ln \frac{N_a N_d}{n_i^2} = \frac{KT}{q} \frac{p_{po}}{p_{no}} = \frac{KT}{q} \ln \frac{n_{no}}{n_{po}} \qquad (1.5)$$

(i) ABRUPT OR STEP JUNCTION.

The abrupt junction assumes an abrupt transition between the *p* - type and *n* - type regions. The junction has uniform *p* - doping on one side of the sharp junction and uniform *n* - doping on the other side. A convenient technique for making abrupt *p*–*n* junctions

is the alloying of a metal containing doping atoms on a semiconductor with the opposite type of dopant. Junctions formed by epitaxial deposition also have an abrupt change in impurity density.[3]

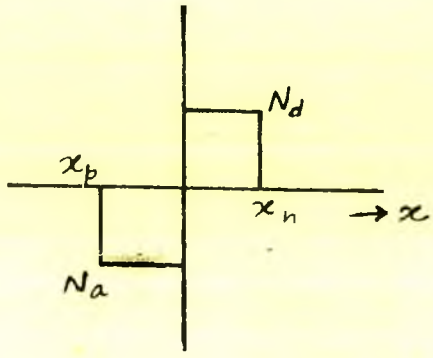


Fig. (4): An abrupt p-n junction

If the acceptor impurities (N_a) is greater than donor impurities (N_d) $\left[N_a >> N_d\right]$ the one sided abrupt junction is written as p^+n and if $N_d >> N_a$, one obtains a pn^+ junction. We consider here a p^+n junction as an example. Since at equilibrium deep inside the semiconductor on both sides of the junction, the charge neutrality is maintained, the total positive charge in the n - side is equal to the total negative charge in p - side. i.e.

$$qN_a x_p = qN_d x_n \qquad \ldots \qquad (1.6)$$

Fig (5) shows the charge density ρ, electric field E and contact potential V of the junction as a function of x.

The relationship between potential V(x) and charge density $\rho(x)$ is given by Poisson's equation,

$$\frac{d^2V(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_s} = -\frac{qN_d}{\epsilon_s} \quad \ldots \quad (1.7)$$

for $0 < x \leq x_n$

For boundary condition at x = 0, electric field

$$E(0) = E_m \text{ (maxm electric field)}$$

$$= \left[\frac{qN_d x_n}{\epsilon_s}\right] \quad \ldots \quad (1.8)$$

$$V(0) = 0$$

and at $x = x_n = W_n = W$, $V = V_o$, the contact potential barrier, solution of the Poisson's equation (1.7) gives

$$V_o = \frac{1}{2} E_m W$$

$$= \frac{qn_d}{2\epsilon_s} W^2 \quad \ldots \quad (1.9)$$

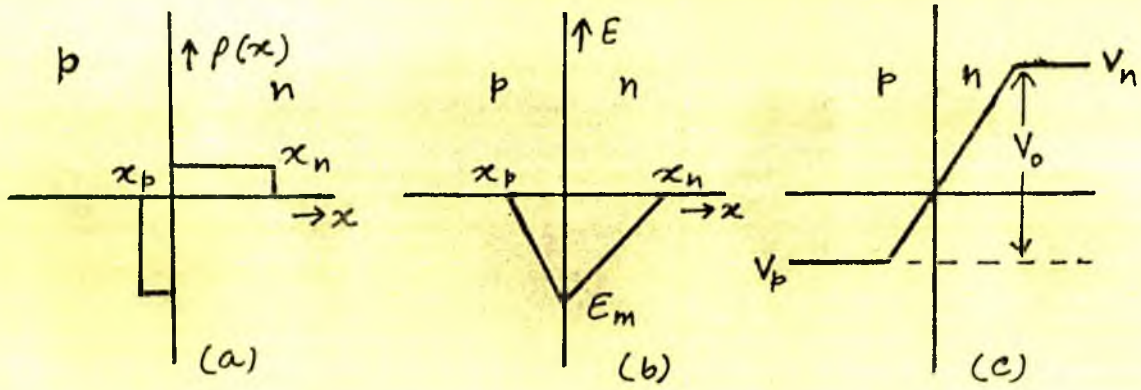


Fig. (5): charge density p, electric field E and contact potential of p^+n junction.

Thus for one sided abrupt junction p^+n, width of the depletion layer can be approximated as

$$W \simeq x_n = \left[\frac{2\epsilon_s}{qN_B} V_o\right]^{1/2} \quad \ldots \quad (1.10)$$

Where $N_B = N_d$ for $N_a >> N_d$. If however $N_a << N_d$, $N_B = N_a$ i.e. N_B represents the impurity concentration on the lightly doped side of the abrupt junction.

If however, abrupt junction is symmetric i.e. both sides have same doping concentration ($N_d = N_a$), the width of the depletion layer is given by

$$W = x_n + x_p = \left[\frac{2\epsilon_s}{qN_dN_a}\left(N_a + N_d\right)V_o\right]^{1/2}$$

$$= \left[\frac{2\epsilon_s}{qN_B} V_o\right] \quad (1.11)$$

$$\text{with} \quad \frac{1}{N_B} = \frac{1}{N_a} + \frac{1}{N_d}$$

The width of the transition region W is in the order of .0005 mm. The potential profile for a typical junction is shown in fig. (5c). Typically its value is $\sim$ 0.41V for Ge and 0.71 for Si. This potential difference may be represented as a battery internally connected across the junction. We may think of it as a potential hill or barrier that can be decreased or increassed by the

application of external voltage: $V_B = V_o \mp V$, where V is the external voltage applied (- sign for +V and vice versa).

(ii) GRADED OR GROWN JUNCTION:

The graded junctions are diffused junctions. The technique for forming graded *p-n* junction is the impurty diffusion process. The impurity concentration in a linearly graded junction, varies gradually from one region to the other and is a linear function of the distance parameter. The significant effects of the junction generally occur entirely within the linear slope region. Such a junction is usually obtained by drowing a single crystal from a melt of semiconductor whose type is changed during the drowing process by adding first *p* -type and then *n* -type impurities.

The charge distribution, electric field and potential difference of a graded junction are shown in figure (6).

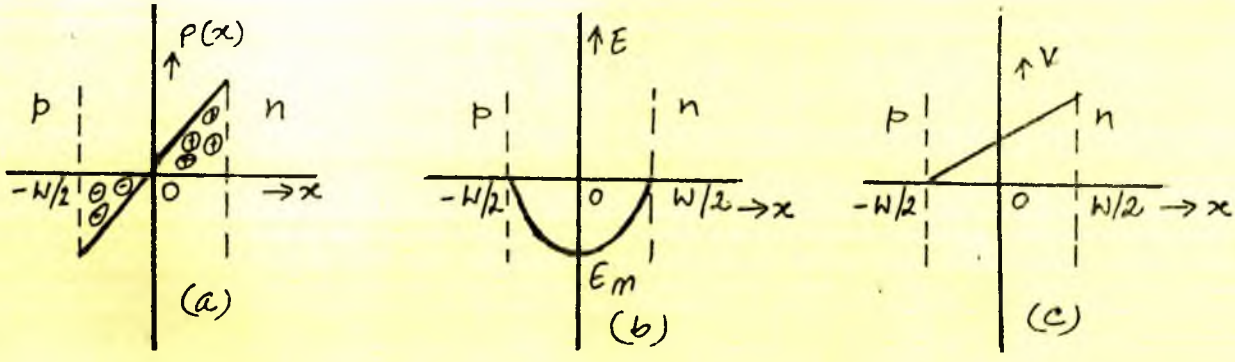


Fig.(6): charge distribution *p*, electirc field E, contact potential *V* of a graded junction.

Let N(x) be the impurity concentration at x distance from the junction, then we can write

$$N(x) = ax \qquad \ldots \qquad (1.12)$$

Here 'a' is called impurity gradient, expressed as $\left(\text{atoms/cm}^3\right)\text{cm}^{-1}$ i.e. atoms cm^{-4}.

From the fig. 6, we can write down Poisson's equation for the region $\frac{-W}{2} \leq x \leq \frac{W}{2}$

$$\frac{d^2V}{dx^2} = -\frac{-\rho(x)}{\epsilon_s} = -\frac{-qax}{\epsilon_s}, \quad -\frac{W}{2} \leq x \leq \frac{W}{2} \qquad (1.13)$$

From the boundary condition

at $x = o, E = -\frac{dV}{dx} = E_m = -qaW^2/8\epsilon_s$ and

at $x = \pm \frac{W}{2}$, $E = 0$, the solution of Eq (1.13) yeilds

V_p = potential at $x = -W/2$

$$= \frac{-qa}{6\epsilon_s}\left(-\frac{W}{2}\right)^3 + \frac{qaW^2}{8\epsilon_s}\left(-\frac{W}{2}\right) + K_1 \qquad (1.14)$$

and V_n = potential at $x = \frac{W}{2}$

$$= -\frac{qa}{6\epsilon_s}\left(\frac{W}{2}\right)^3 + \frac{qaW^2}{8\epsilon_s}\left(\frac{W}{2}\right) + K_1 \qquad (1.15)$$

Hence the contact potential barrier V_o across the junction[4], in the abscence of any external voltage may be expressed as

$$V_o = V_n - V_p = \frac{qaW^2}{12\epsilon_s} \quad \ldots \quad (1.16)$$

and W = width of the depletion region

$$= \left[\frac{12\epsilon_s}{qa} V_o\right]^{1/3} \quad \ldots \quad (1.17)$$

1.3 P-N JUNCTION AS A DIODE:

The *p-n* junction is refered to as junction diode, because the junction is a two terminal device. Basically all junction diodes act as rectifiers i.e. it permits the easy flow of electricity in one direction then oppositely. This is the desired property of a diode rectifier. In general, all diodes have similar characteristics, volt-ampere curve, the reverse breakdown phenomenon, certain maximum current and voltage values, temperature characteristic and frequency limitation.[5]

(i) FORWARD BIAS:

If a positive voltage *V* is applied to the *p* side with respect to the *n* side, we call the junction is forward biased. When the

diode is operated in this way the barrier potential will be decreased by an amount of the applied voltage V . The reduced potential barrier height ($V_B = V_o - V$) gives a low resistance path and allows majority carriers to diffuse through the junction. So that a large current is realized. The application of +V destroys the equilibrium that exists between the forces tending to cause diffusion of majority carriers and the restraining effect of the potential energy barrier. As a result the holes cross the junction from the *p* -side into the *n* -side constituting an injected minority current. Simultaneously, the electrons cross the junction from *n* -region to *p* -region constituting the injected minority current. The flow of holes from *p*- to *n*- and electrons from *n*- to *p*- regions constitute conventional currents in the same direction namely from *p*-region to *n*- region, the total current being the summation of these two components. The hole flow are approximately equal. In addition to this large current due to majority carries

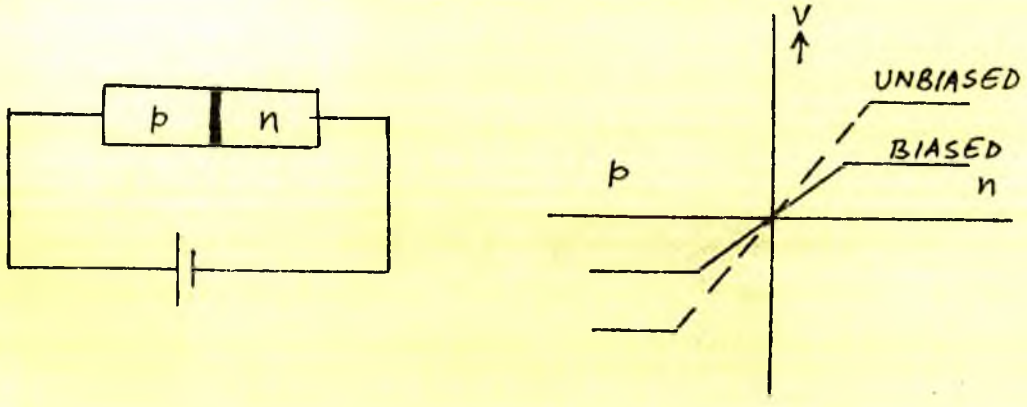


Fig.(7): Forward biased p-n diode

there is a small current due to the minority carriers but it is almost negligible. It has been found that the current increases exponentially with the applied voltage.

(ii) REVERSE BIAS:

When a negative voltage $-V_R$ is applied to the *p* - side with respect to the *n* - side, Fig.(8), the potential barrier height is increased to $V_o + V_R$ and the depletion region widens due to the positive terminal of the battery drawing electrons from the *n* - type and the negative terminal attracting holes from the *p* - type. The increased potential barrier prevents carrier transport through the junction. Only the minority carriers can cross the junction, as a result a small reverse current, usually in the micro ampere region, flow from *n*- side to *p*- side. The small current results from the small number of hole-electron pairs continuously generated throughout the device because of the thermal energy. The holes so generated in the *n*- region (electrons in the *p*- region) cross the junction and enter *p*- region (electrons - *n* region). This total small current, as caused by both holes and electrons, is termed as diode reverse saturation current I_o. Since the density of the minority carrirs (see Eq. 1.18 below) depends upon the amount of thermal energy, the reverse current is very temperature dependent - increasingwith the increase of temperature. Hence the back resistance of a semiconductor diode decrease as the temperature increases. For the same reason the

forwarcurrent is also temperature dependent, but to a much smaller degree.

$$\eta_i^2 \simeq A_o\, T^3\, e^{-E_o/kT} \qquad \ldots \qquad (1.18)$$

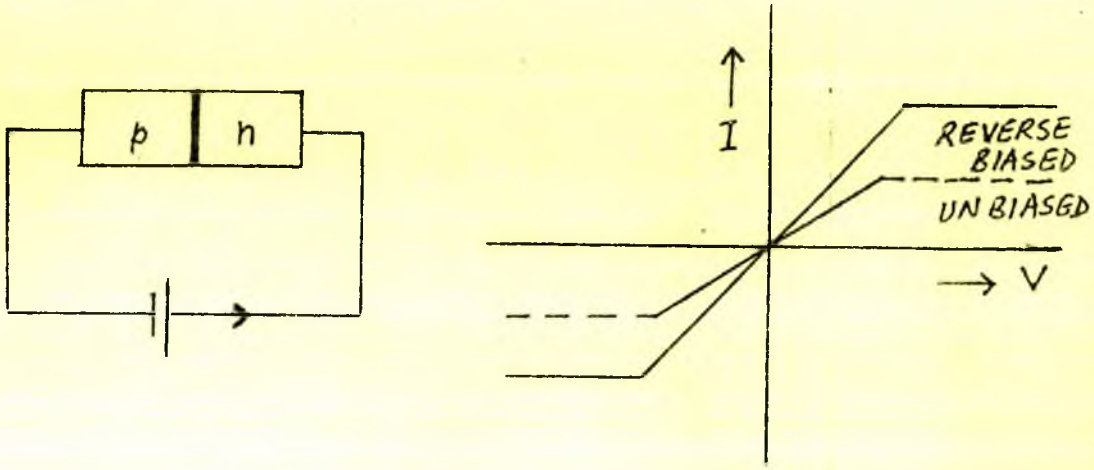


Fig. (8): p-n junction under reverse bias condition.

1.4 CURRENT IN P-N JUNCTION:

If the diode is forword biased, holes are injected into the *n*- side and electrons into the *p*- side. The number of these injected minority carriers falls off exponentially with distance from the junction (Eq. 1.19).

$$P_n(x) = p_n - p_{no} = P_n(o)e^{-x/L_p} \qquad (1.19)$$

Where $P_n(x)$ = injected concentration of holes

p_n = hole concentration

p_{no} = thermal equilibrium concentration of holes before the applicantion of the forward bias

$P_n(0) = p_n(0) - p_{no}$ = excess holes at $x = 0$.

$p_n(0)$ = hole concentration at $x = 0$

L_p = diffusion length which represents the distance into the semiconductor at which the injected concentration falls to $\frac{1}{e}$ th of its value at $x=0$.

Similar equation exists for electorns in *p* -side. Since the diffusion current of minority carriers is proportional to the concentration gradient, this current must also vary with distance from the junction on both sides.

Thus according to diffusion equation, the minority carrier hole diffusion current at x = 0 and entering the *n*- region is given by

$$I_{pn}(0) = -AqD_p \left.\frac{dp_n}{dx}\right|_{x=0} \quad \ldots \quad (1.20)$$

and similar equation for minority carrier electron diffusion current that enters the *p*- region $\left[I_{np}(0)\right]$. The total current I at x = o is then

$$I = I_{pn}(0) + I_{np}(0) \quad \ldots \quad (1.21)$$

which remains same throughout the circuit.

Under forward bias, we note from Eq.(1.19) that the concentration of holes p_n in the *n* - region is increased above its thermal equlibrium value p_{no} i.e

$$p_n(x) = p_{no} + P_n(o)e^{-x/L_p} \quad \ldots \quad (1.22)$$

Therefore hole diffusion current at a distance x in the *n* - region can be expressed as

$$I_{pn}(x) = -AqD_p \frac{dp_n}{dx}$$

$$= \frac{AqD_p P_n(o)}{L_p} e^{-x/L_p} \quad \ldots \quad (1.23)$$

The above equation proves the statement that hole current decreases exponentially with distance. Similar equation for electrons in *p* - side exists.

We noted earlier that a forward bias lowers the barrier height and permits more charge carrier to cross the junction. $p_n(o)$, and hence $P_n(o)$, the injected concentration of holes must be a function of the applied forward bias V. It has been shown theoretically that holes arriving at the junction x=o, $p_n(o)$ obeys the relation.

$$p_n(o) = p_{no} e^{V/V_T} \quad \ldots \quad (1.24)$$

$$\text{Where,} \quad V_T = \frac{KT}{q} = \frac{T}{11,600} \quad \ldots \quad (1.25)$$

and is defined as volt equivalent of temperature, k is Boltzmann constant expressed in joules / deg. K .

From Eq.(1.22) and (1.24) we get an expression for $P_n(o)$

$$P_n(o) = p_{no} e^{(V/V_T - 1)} \quad \ldots \quad (1.26)$$

The boundary condition given by Eq (1.24) or Eq (1.26) is called the law of the junction. Similar equation with p and n interchanged gives the electron concentration and injected electrons at the edge of the p – region.

$$n_p(o) = n_{po} e^{V/V_T} \quad (1.27)$$

and $$N_p(o) = n_{po} \exp\left[V/V_T - 1\right] \quad \ldots \quad (1.28)$$

Using Eqs (1.26), (1.23) we get expression for $I_{pn}(o)$ and $I_{np}(o)$ and using them in (1.21) we obtain the expression for total diode current under forward bias V i.e.

$$I = I_o \left[e^{V/V_T} - 1\right] \quad \ldots \quad (1.29)$$

With $$I_o = \frac{AqD_p p_{no}}{L_p} + \frac{AqD_n n_{po}}{L_n} \quad \ldots \quad (1.30)$$

Let us consider the *n*– region Since at any x, the total current must remain same, the majority (electron) current I_{nn} must vary with x such that total current I at any position is constant. Hence we may write

$$I_{nn}(x) = I - I_{pn}(x) \quad (1.31a)$$

and for *p* – region similarly we have

$$I_{pp}(x) = I - I_{np}(x) \quad (1.31b)$$

The behaviour of these current components are shown in Fig. (9)

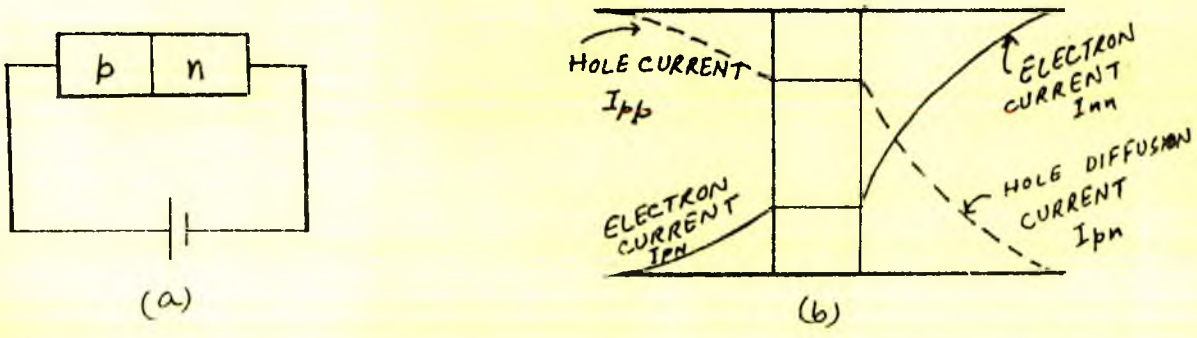


Fig.(9) The minority carrier current (solid) and the majority carrier current (dashed) as a function of *x* in a p-n diode ($N_a >> N_d$).

We further note that in the *p* - region far away from the junction, the current is a drift current I_{pp} of holes as covered by a small electric field in the semiconductor. However,as the holes approach the junction, a few of the holes recombine with electrons which got injected into the *p* - region from the *n*-side. This recombination process reduces I_{pp} as it approaches the junction. The rate of reduction must be such that the total current remains same. This reduced hole current I_{pp} at the junction enters the *n*-side and becomes the hole diffusion current I_{pn}. Similar remarks may be made for I_{nn} in *n*-region.

Thus it is seen that the current in a p-n diode is bipolar in nature since this current is due to flow of positive and negative charge carriers.

Eqn. (1.29) is the celebrated Schockley equation which is the ideal diode law. The ideal current -voltage relation is shown in Fig. (10) below:

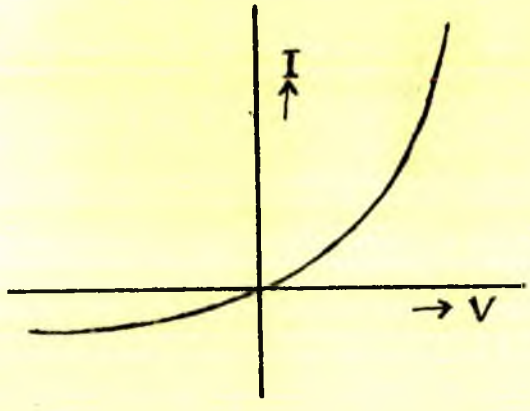


Fig (10): I-v curve for an ideal diode (linear plot)

It may be mentioned here that Schockley equation for ideal diode has been derived on the assumptions that (i) the abrupt depletion layer remains valid, (ii) Boltzmann approximation is applicable throughout the depletion layer, (iii) injection level is very low, (iv) the most important one being – no generation current exists in the depletion layer and the electron and hole currents are constant through the depletion layer.[6]

15 REVERSE SATURATION CURRENT

Schockley Equation (see Eq 1.29) is equally valid for reverse bias i.e. for negative values of V. We note that in reverse direction the current saturates at $-I_o$. Accordingly this current I_o is called reverse saturation current. From Eq. (1.30), we get

$$I_o \equiv Ag \left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n} \right]$$

For *n* – type and *p* – type we may write,

$$p_{no} = \frac{n_i^2}{n_{no}} = \frac{n_i^2}{N_d} \quad \ldots \quad (1.32a)$$

and

$$n_{po} = \frac{n_i^2}{p_{po}} = \frac{n_i^2}{N_a} \quad \ldots \quad (1.32b)$$

Using these expressions in equation for I_o, we have

$$I_o = Aq \left[\frac{D_p}{L_p N_d} + \frac{D_n}{L_n N_a} \right] n_i^2 \qquad \ldots \qquad (1.33)$$

Where n_i^2 is given by Eqn.(1.18).

In Eq. (1.33) D_p, L_p $\left[\equiv \sqrt{D_p \tau_p} \right]$, D_n, L_n $\left[\equiv \sqrt{D_n \tau_n} \right]$, are all temperature dependent. If D_p/τ_p and D_n/τ_n are proportional to T^γ, where γ is a constant, then

$$\begin{aligned} I_o &\approx kT^{(3+\gamma/2)} \; e^{-E_g/kT} \\ &= kT^{(3+\gamma/2)} \; e^{-v_g/v_T} \\ &= K \, T^m \, e^{-v_g/v_T} \end{aligned} \qquad \ldots \qquad (1.34)$$

Where K is a constant, independent of temperature.

1.6 TRANSITION REGION:

In the above discussion we have not taken into account of effect of carrier generation and recombination. For Ge device this ommission is not serious but not for other devices like Si or GaAs. In such devices transition layer charge generation current may be comparable to diffusion current. Schockley equation for ideal diodes can give only qualitative agreement. The deviation from the ideal are mainly due to : (1) Surface effect, (2) the generation and recombination of carriers in the depletion layer,

(3) the high injection condition which may occur even at relativly small forward bias, (4) the series resistance effect, (5) the tunneling of carriers between states in the band gap (particularly for GaAs).

The surface effect on *p–n* junction are mainly due to the ionic charges on or outside the semiconductor surface which induce image charges in the semiconductor and thus cause the formation of the soclled surface channels or surface depletion layer regions. This effect gives rise to surface leakage current. For Si planar *p–n* junctions the surface current is in general much smaller than the generation current in the depletion region. (Ref. 2)

Under reverse bias condition, as there is reduction of carrier concentration ($pn << n_i^2$), the dominant recombination generation processes are those of emission. With $p < n_i$ aswell as $n < n_i$, the rate of generation of electron – hole pair may be expressed as

$$g = -\left[\frac{\sigma_p \sigma_n \nu_{th} N_t}{\sigma_n \exp\left(\frac{E_t - E_i}{KT}\right) + \sigma_p \exp\left(\frac{E_i - E_t}{KT}\right)}\right] n_i$$

$$= -\frac{n_i}{\tau_e} \qquad (1.35)$$

Where τ_e = effective life time and is the reciprocal of the expression in the square braket.

Thus current due to the generation in the depletion region can be estimated as

$$I_g = \left[\frac{qn_i}{\tau_e} W\right] A \qquad \ldots \qquad (1.36)$$

Where W is the depletion layer width and A is the diode cross sectional area. Thus the generation current will there have the same temperature dependence as n_i. At a given temperature I_g is proportional to the depletion layer width. Which in turn is dependent of the reverse bias. We therefore explain

$$I_g \alpha \left[V_o + V\right]^{1/2} \text{ for abrupt junction,}$$

and

$$I_g \alpha \left[V_o + V\right]^{1/3} \text{ for linearly graded junction.}$$

The total reverse saturation current I_s can be approximated as the sum of the diffusion component in the neutral region and the generation current in the depletion layer for a p^+n diode:

$$I_s = q \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_d} + \frac{qn_i}{\tau_e} W \qquad (1.37)$$

The first part of the above equation is the diffusion current component and second part is the generation current.

For semiconductor with large n_i (e.g. Ge) the diffusion component predominates and I_s follows the Shockley equation. However for small value of n_i(e.g. Si) the generation current may dominate.[6]

Let us consider the case when diode is forward biased. In this case, the major recombination -generation processes in the depletion region are the capture processes and we will have a recombination current component I_r together with the diffusion component. For simplicity if we make the following assumption $E_i = E_t$ and $\sigma_n = \sigma_p = \sigma$, the recombination rate γ may written as

$$\gamma \simeq \frac{1}{2} \sigma \nu_{th} N_t n_i \exp\left[\frac{qV}{2kT}\right] \quad (\text{for } V > kT/q) \qquad (1.38)$$

and the recombination current,

$$I_\gamma \simeq \frac{qW}{2} \sigma \nu_{th} N_t n_i \exp\left[\frac{qV}{2kT}\right] \qquad (1.39)$$

We note that similar to the generation current in reverse bias, the recombination current in forward bias is also proportional to n_i. Thus the total forward current for a p^+n junction, is approximately given as the sum of diffusion component and recombination component[7].

$$I_F = q \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_d} \exp\left[\frac{qV}{kT}\right] + \frac{qW}{2} \sigma \nu_{th} N_t n_i \exp\left[\frac{qV}{2kT}\right] \qquad (1.40)$$

It may be mentioned here that above expression for generation and recombination current are derived on the assumption that there exists a single-level generation recombination centres that are uniformly distributed and have energy E_t very near to the intrinsic Fermi-level E_i and N_t is the concentration.

Usually the forward current can be expressed, taking into account of the effect of transition region, by an empirical relation given as

$$I_f \sim \exp\left(\frac{qV}{\eta kT}\right) \qquad (1.41)$$

1.7 CALCULATION OF η :

From the above discussion it is thus evident that in general the volt-ampere characteristic may be reprsented by

$$I = I_o\left(e^{qv/\eta kT}-1\right)$$

$$= I_o\left(e^{V/\eta V_T}-1\right) \qquad \ldots \qquad (1.42)$$

Here I_o is the reverse saturation current and V_T is the volt equivalent of the temperature T given by Eq. (1.25) η is very nearly equal to 2 for rated current in Si and $\eta \simeq 1$ for Ge. At room temperature ($T \simeq 300^oK$)

$$V_T \simeq 0.026V = 26\ mV$$

From Eq. (1.42), assuing that V is very large compared to V_T, so that we may drop the unity, we have

$$\ln I = \ln I_o + \frac{V}{\eta V_T}$$

$$\log I = \log I_o + \frac{0.434}{\eta V_T} \quad \ldots \quad (1.43)$$

We therefore, expect that at small current the plot of logI against V will be a straight line and from the slope we can evaluate η and from the intercept the value of I_o at temperature of ovservation T.

At high current however, an increment of voltage does not yeild as large an increase of currents as at low currents. The reason is the ohmic resistance of the diode comes into effect. At low current the ohmic drop is negligible and the applied external voltage simply decreases the potential barrier of the junction. At high currents the external voltage acts upon principally to establish an electric field to overcome the ohmic resistance of the semiconductor material. Therefore the diode behaves more like a resistor than a diode and current tend to increase linearly rather than exponentially.

(i) CUT-IN VOLTAGE V_γ AND PIECEWISE LINEAR DIODE CHARACTERISTICS:

If we look I-V characteritic of a *p-n* junction we note that there exists a cutin, offset, breakpoint, or threshold voltage V_γ, below which the current is very very small. Beyond this voltage V_γ, the current rises very rapidly. The cutin voltage of *p-n* diode

differs for different semiconductor material and for different methods of fabrication. For Ge this Value is ~ 0.2v and for Si this is 0.6.

This difference results partly due to higher reverse saturation current in a Ge- diode than in Si-diode. The other reason for the delay in the rise of forward current in Si-diode is that the current increases as $e^{V/2V_T}$ in small current range with V being a few tenths of a volt but increase as e^{V/V_T} only at higher voltages.

A large signal approximation often used with sufficient accuracy is the piecewise linear representation. Fig. (11) below shows a piecewise linear approximation for a *p-n* junction diode.

The breakdown voltage V_γ also called offset voltage is not at the origin . Accordingly for $V < V_\gamma$, the diode acts as an open circuit, while for $V > V_\gamma$, the diode has a constant incremental resistance $\gamma = \frac{dV}{dI}$. The resistance defined as such is called forward resistance and refered as R_f.

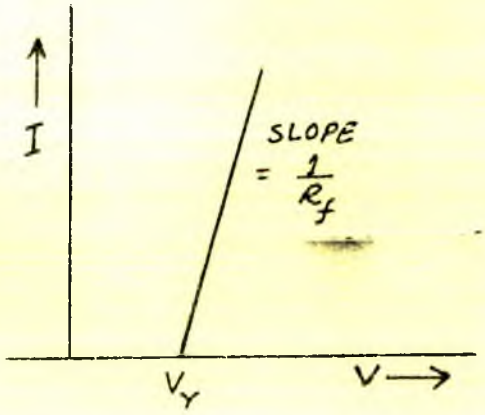


Fig. (11)

(ii) REVERSE SATURATION CURRENT I_o AND FORBIDDEN ENERGY GAP:

From our earlier discussion it follows that in geleral. The reverse saturation current I_o may be expressed as (see Eq.1.34)

$$I_o = KT^m e^{-V_g/\eta V_T}$$

$$= KT^m e^{-qV_g/\eta KT}$$

Where k is a constant and V_g is the forbidden energy gap expressed in volt. The constant m depends on the semiconding material of the diode. Thus for

Ge: $m \simeq 2 \qquad \eta = 1$

Si: $m \simeq \frac{3}{2} \qquad \eta = 2$

We note that reverse saturation current depends on the semiconductor energy gap E_g or V_g. From the above Eq. we have

$$\ln I_o = \ln k + m \ln T - \frac{V_g}{\eta V_T}$$

$$= \ln k + m \ln T - \frac{V_g}{\eta T} \times (11600) \qquad (1.44)$$

The temperature dependence term T^m is not very important in comparison with exponential term. The slope plot of $\ln I_o$ against $\frac{1}{T}$ is determied by the energy gap E_g. From the slope we may estimate η or V_g. It is thus expected that in the reverse direction the

current I_o will increase approximately as $e^{-E_g/KT}$ with temperature; and in the forward direction the current I will increase approximately as $e^{-(E_g-qV)/KT}$.

1.8 DIODE REVERSE RECOVERY TIME:

A p-n junction diode, on being switched from forward bias to reverse bias condition, or vice versa, has a response time accompanied by a transient. Thus, on being switched, diode response reaches the steady state after an interval of time, This interval of time is called the recovery time. The forward recovery time defined as (when switched from reverse bias to forward bias) time interval between the instant of 10% diode voltage to the instant this voltage reaches within 10% of its final value. In a similar way reverse recovery time is defined. Forward recovery time posses no serious problem. We would therefore only discuss briefly reverse recovery time.

From our earlier discussion we note that when a p-n junction is forward biased, the minority carrier density, under steady state condition both side of the junction falls off exponentially with distance x . The minority carrier holes in the *n*-region have been supplied from the other side where these holes are in plentiful supply. Similarly minority carrier electrons in the *p* - region have been supplied from the *n* - region where they are in large number.

Now let the diode, carrying a current in the forward direction under an external voltage V, be reversed suddenly. The diode current then does not instantaneously fall to its steady state reverse voltage. This steady state value of current in reverse voltage condition is reached only when the minority carrier distribution reduces from its initinal distribution to the new distribution i.e. when the injected or excess minority carrier density ($p_n - p_{no}$) or ($n_p - n_{po}$) has dropped nominally to zero.[4]

CHAPTER TWO

DEPLETION CHPACITANCE

2.1 JUNCTION CAPACITANCE:

The uncompensated acceptor ions on the P - side provide a negative charge and an equal positive charge results from the ionized donores on the *n* - side of the transition region. These opposite charges in the depletion region are analogous to charges on the opposite plates of a capacitor. Hence with no bias applied to the junction there is a fixed space - charge capacitance associated with the junction, which is called junction capacitance.

Capacitance is defined as differential flow of charge into a plate or terminal with respect to a change of voltage. When the voltage across a *p-n* junction is changed, there is a change in the width of the depletion region, which requires a flow of charge. Also the number of minority carriers on either side of the junction changes, with the change in depletion region. The contribution to capacitance of the change in depletion width is called depletion - layer capacitance, where as the contribution of the changes in minority carrier density is called diffusion capacitance. Depletion layer capacitance is dominant under reverse bias conditions and diffusion capacitance is dominant when it is forward biased.

As the capacitance is inversely proportional to width of the dielectric medium between the plates, applying a reverse bias to the junction, decreases the junction capacitance. The junction capacitance increases with increasing forward bias voltage.

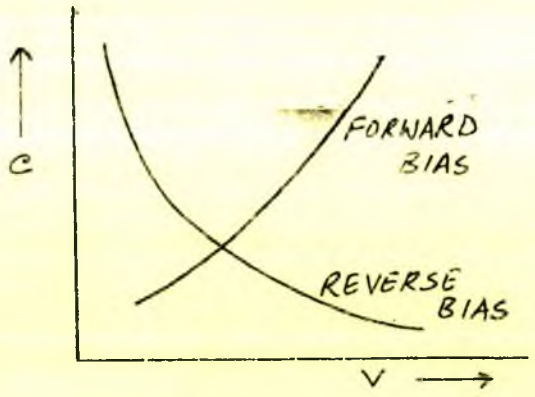


Fig. (12): Bias effect on junction capacitance

2.2 DEPLETION CAPACITANCE IN ABRUPT JUNCTION:

Let us consider a *p–n* junction with arbitrary distribution of impurities and contact potential V_o. If a reverse bias is applied to the diode, the total magnitude of potential is the sum of contact potential V_o and applied potential V_R. Capacitance is obtained as the differential rate of change of charge with respect to voltage:

$$C = \frac{dQ}{dV} \qquad \ldots \qquad (2.1)$$

Where dQ is the increase in charge per unit area caused by a change dV in voltage.

The value of Q can be written in terms of doping concentration and transition region width on each side of the

junction,

$$|Q| = qAx_n N_d = qAx_p N_a \quad \ldots \quad (2.2)$$

As, widths x_n and x_p are,

$$x_n = \frac{N_a}{N_a+N_d} W \text{ and } x_p = \frac{N_d}{N_a+N_d} W$$

equation (2.2) becomes,

$$|Q| = qA \frac{N_a N_d}{N_d+N_a} W \quad \ldots \quad (2.3)$$

Where $$W = \left[\frac{2\epsilon_s}{q} \left(\frac{N_a+N_d}{N_a N_d} \right) \left(V_o \pm V \right) \right]^{1/2}$$

$$= \left[\frac{2\epsilon_s}{qN} V_B \right]^{1/2} \quad (2.4)$$

$$\left[\text{As, } V_B = V_o + V \text{ \& } \frac{1}{N_B} = \frac{1}{N_a} + \frac{1}{N_d} \right]$$

From equation (2.3) we get,

$$C = \left| \frac{dQ}{d(V_o - V)} \right| = \frac{A}{2} \left[\frac{2q\epsilon_s}{(V_o - V)} \frac{N_a N_d}{N_a+N_d} \right]^{1/2}$$

$$= \frac{A}{2} \left[\frac{2q\epsilon_s}{V_B} \frac{N_a N_d}{N_a+N_d} \right]^{1/2}$$

$$= \frac{A\epsilon_s}{W} \quad \ldots \quad (2.5)$$

If V=0, $V_i = V_o$, the intrinsic potential barrier, then

$$W = W_o = \left[\frac{2\epsilon_s}{qN_B} V_o\right]^{1/2} \quad \ldots \quad (2.6)$$

C_o = intrinsic capacitance of the junction

$$= \frac{A\epsilon_s}{W_o} \quad \ldots \quad (2.7)$$

For a one sided abrupt junction p^+n, $N_a >> N_d$ and $x_n \simeq W$, while x_p is negligible. The capacitance is then,

$$C = \frac{A}{2}\left[\frac{2q\epsilon_s}{V_o - V} N_d\right]^{1/2} \quad \ldots \quad (2.8)$$

Equation (2.8) is the so called *C* square-root *V* law for capacitance of a step junction.

If *V* is sufficiently greater than V_o, it is a good approximation that $CV^{1/2}$ is constant.

For a p^+n junction,

$$\frac{1}{C^2} = \frac{2V_o}{A^2\epsilon_s qN_B} + \frac{2V}{A^2\epsilon_s qN_B} \quad \ldots \quad (2.9)$$

Therefore, from the slope of the plot $1/C^2$ Vs V, we can get N_B if area of the junction, *A* is known and hence, W_o from Eq. (2.7). V_o, the intrinsic contact potential is obtained from the intercept on

the V-axis and hence C_o, the intrinsic capacitance may be obtain straightway.

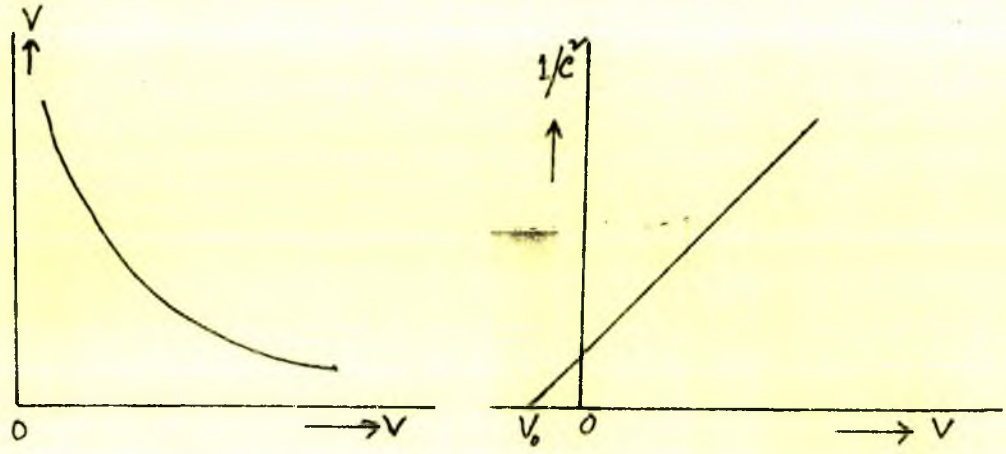


Fig. 13

2.3 GRADED JUNCTION CAPACITANCE:

In a graded junction the total charge distribution is given by

$$\rho(x) = q\left[p(x) - n(x) + N(x)\right]$$
$$\simeq qax \qquad -W/2 \leq x \leq W/2 \qquad (2.10)$$

The solution of Poisson's equation (see Eq.1.13)

$$V_o = \frac{qaW^3}{12\epsilon_s}$$

or
$$W = \left[\frac{12\epsilon_s V_o}{qa}\right]^{1/3} \qquad \ldots \qquad (2.11)$$

Now, if the junction is externally biased, as before, the width W then expressed as,

$$W = \left[\frac{12\epsilon_s}{qa}(V_o \pm V)\right]^{1/3} = \left[\frac{12\epsilon_s}{qa} V_B\right]^{1/3}$$

The junction capacitance is then given by [4]

$$C = \frac{\epsilon_s A}{W} = A \left[\frac{qa\epsilon_s^2}{12V_B}\right]^{1/3} \quad \ldots \quad (2.12)$$

The variation of capacitance in equation (2.12) is called cube-root variation and a cube root variation proves the junction to be a linear gradient.

Under reverse bias condition we may write, equation (2.12) as

$$\frac{1}{C^3} = \frac{1}{A^3}\left[\frac{12}{qa\epsilon_s^2} V_o + \frac{12}{qa\epsilon_s^2} V\right] \quad \ldots \quad (2.13)$$

Then plot of $^1/C^3$ Vs V, the applied reverse voltage will yield a straight line with the slope.

$$\frac{d(^1/C^3)}{dV} = \frac{12}{qa\epsilon_s^2}\left[\frac{1}{A^3}\right] \quad \ldots \quad (2.14)$$

from which 'a' can be estimated if, the area of the junction A is known. From the intercept of V with $^1/C^3 = 0$, we can find the contact potential barrier V_o and hence C_o, is the intrinsic capacitance of the junction.

2.4 TEMPERATURE DEPENDENCE OF DEPLETION CAPACITANCE:

We know the intrinsic or contact potential barrier V_o (Eq.1.5) is related to intrinsic carrier concentration n_i and temperature T, as:

$$qV_o = KT \ln \left[N_a N_d / n_i^2\right] \quad \ldots \quad (2.15)$$

It reveals that the contact potential V_o is a function of T. We further know that n_i^2 decreases with the decrease of temperature through the relation

$$n_i^2 = A_o T^3 \exp\left(-E_{go} / KT\right) \quad \ldots \quad (2.16)$$

where A_o = constant.

This means in effect V_o in Eq. (2.15) increases with decrease of temperature and increase of V_o results in the increase of width of the depletion layer (W). As a result lowering of temperature in general should decrease the depletion capacitance. Combining equation (2.15) and (2.16) we get,

$$qV_o = KT \left[\ln (N_a N_d) - \ln n_i^2\right]$$

$$\simeq E_{go} + KT \ln \left[\left(\frac{N_a N_d}{A_o}\right)\left(\frac{1}{T^3}\right)\right] \quad (2.17)$$

Equation (2.15), shows that at higher temperature V_o decreases which results in the decrease of the depletion layer width W. This

ultimately, affects the capacitance of the junction i.e. increase of temperature causes the increase of capacitance. We however note that initially at low temperature capacitance may rise and then falls with the temperature. The temperature at which capacitance result maximum may be found from Eq. (2.15) as

$$T_m = \frac{1}{e}\left(\frac{N_a N_d}{A_o}\right)^{1/3} \quad \ldots \quad (2.18)$$

2.5 SCHOTTKEY DEVICES:

Schottkey diodes are devices made of metal semiconductor junction. One may use wide variety of metals like Au, Ag, Al, Pt etc in contact with n- or p- type semiconductor like Ge, Si, GaAs etc.

The minimum energy required for an electron to escape from the metal surface is termed as work function ϕ, measured from the fermi level to the valence level. The ϕ is very sensitive to the surface contaminator. We also know application of an external field, causes the potential energy barrier corresponding to ϕ is lowered due to the so called Schottkey effect. The lowering of the barrier $\Delta\phi$ and where it occurs are given by two equations

$$\Delta\phi = \sqrt{\frac{qE_a}{4\pi\epsilon_o}} \quad (2.19)$$

and

$$x_m = \sqrt{\frac{q}{16\pi\epsilon_o E_a}} \quad (2.20)$$

where E_a = applied electric field

Thus at very high field, the lowering of potential barrier may cause field emission from the metal.

The emission of electron from the conduction to the vacuum level in a semiconductor, say n-type material is governed by an analogous parameter ϕ_s, measured from the Fermi level to the vacuum level. It is related to the conduction band level (E_c), the fermi level and the electron affinity χ measured from the bottom of the conduction band to the vacuum level.

$$\phi_s = E_c + \chi - E_F \qquad (2.21)$$

If now a metal surface is in intimate contact with say, an n-type semiconductor and $\phi_s \neq \phi_m$, then an inequilibrium states exists. So to achieve equilibrium the fermi levels in both materials must be coincident. As $\phi_m > \phi_s$, the electron from the semiconductors will flow into the metal, resulting metal surface negatively charged. The semiconductor will acquire positive charge. This process will continue still an equilibrium is reached i.e. an electric field is established between the metal-semiconductor junction which opposes further flow of electron from n-type to the metal. As density of donors is relatively low the donors will become ionized over a region which extends into the n-material i.e. a space charge region is formed, similar to p^+n junction. Thus a contact potential barrier will be created which will oppose the flow of electrons from semiconductor to metal and +ve charges from metal to semiconductor.

If we now apply an external electric field across the junction the potential barrier will change and so also the width of the depletion layer. If the semiconductor end is made +ve with respect to the metal the barrier height increases and vice versa. It is thus clear from the above discussion that if a metal is in intimate contact with a semiconductor the conduction band and valence bands of the semiconductor are brought into a definite energy relationship with the fermi level in the metal. This relationship imposes the boundary condition under which Poission's equation is to be solved.

Under the abrupt approximation that charge density,

$$\rho = qN_d \qquad \text{for} \qquad x < W$$

and $$\rho = 0 \; ; \; \frac{dV}{dx} = -E = 0 \qquad \text{for} \qquad x > W$$

the solution of Poisson's equation

$$\frac{d^2V}{dx^2} = \frac{\rho}{\epsilon_s} = \frac{qN_d}{\epsilon_s} \qquad (2.22)$$

$$x < W$$

yields the results identical to those of the one-sided abrupt p-n junction and we have

$$W = \text{width of the depletion layer}$$

$$= \frac{2\epsilon_s}{qN_d}\left(V_{ib} - V - \frac{KT}{q}\right) = \frac{2\epsilon_s}{qN_d}\left(V_{ib} - V - V_T\right) \qquad (2.23)$$

and $|E(x)|$ = electric field intensity

$$= \frac{qN_d}{\epsilon_s}(W - x) = E_m - \frac{qN_d}{\epsilon_s}x \qquad (2.24)$$

$$V(x) = \frac{qN_d}{\epsilon_s}\left(Wx - \frac{1}{2}x^2\right) - (V_m - V_x)$$

$$= \frac{qN_d}{\epsilon_s}\left(Wx - \frac{1}{2}x^2\right) - V_n \qquad (2.25)$$

The term $\left(\frac{KT}{q} = V_T\right)$ arises from the contribution of the mobile carriers to the electric field and E_m is the maximum electric field strength occurring at x = 0. V_N is the voltage equivalent and V_n volt - equivalent of the limiting value of the barrier height $(\phi_m - N)$.

For V = 0 and neglecting the effect of KT/q, we have the contact potential V_i, intrinsic width W_o identical to p^+n junction. In a similar way, the depletion layer capacitance may be obtained i.e.

$$C = \frac{\epsilon_s A}{W} = A\left[\frac{q\epsilon_s N_d}{2(V_{ib} - V - \frac{KT}{q})}\right]^{1/2} \qquad (2.26)$$

If N_d is constant throughout the depletion region, we would get a straight line when $\frac{1}{C^2}$ vs V is plotted. Thus once again from the x-axis intercept we estimate V_i and obtain C_o from the intercept on $\frac{1}{C^2}$ axis, and then if area of the junction is known N_d, concentration of the n-type material may be obtained.

2.6 EFFECT OF SURFACE STATES:

So far we have assumed that both the metal and semiconductor surfaces are clean i.e. free of any contamination and lattice defect. It is well known that the barrier heights of metal-semiconductor system are determined by both the metal work function and the surface states. The physical origin of the surface states lies in (1) imperfection of real surface (2) impurity atoms absorbed on the surface.

It is evident that at the surface of a semiconductor i.e. boundary of the periodic lattice the situation may be complex. The sequence of the allowed and forbidden zone breaks down at the surface and energy states may be occupied there which would be forbidden within the crystal. Occupancy of these states at the surface leads to a layer of surface charge which intern creates a layer of space charge in the crystal beneath of the surface and thus a potential energy barrier is created.

Whatever may the cause of the presence of surface states on the semiconductor surface a general expression of the barrier height of metal-semiconductor contact is obtained on the basis of the assumptions : (1) with intimate contact between the metal and the semiconductor and with an interfacial layer of atomic dimensions, this layer will be transparent to electrons and can withstand potential across it and (2) the surface states per unit area per eV at the interface are a property of the semiconductor surface and are independent of the metal.

As an example, if we consider a metal n-type semiconductor with surface states, the surface state charge density on the semiconductor may be expressed as

$$q_{ss} = -qN_s \left[E_g - \phi_o - \phi_n - \Delta\phi\right] \qquad (2.27)$$

where,

N_s = number of surface states / cm^2/eV

ϕ_o = Energy difference between the fermi level and the valence - band edge

ϕ_n = barrier height of the metal-semiconductor barrier

$\Delta\phi$ = Schottkey barrier lowering

The space charge distribution which form in the depletion layer of the semiconductor at thermal equilibrium is very similar to p^+n abrupt junction.

$$q_{sc} = 2q\epsilon_s N_d \left[V_{ib} - \frac{KT}{q}\right] \qquad (2.28)$$

$$V_i = V_n - V_{FC} + \frac{1}{q}(\Delta\phi - kT)$$

It has been shown that barrier height of metal semiconductor for such a system is

$$V_n = \frac{\phi_n}{q} = \frac{1}{q}\left[C_2(\phi_n - \chi) + (1-C_2)(E_g - \phi_o) - \Delta\phi\right] \qquad (2.29)$$

$$\equiv \frac{1}{q}\left[C_2\phi_m\right] + C_3$$

If C_2 and C_3 are determined experimentally and N is known, then

$$\phi_o = E_g - \frac{C_2 N + C_3 + \Delta\phi}{1 - C_2} \qquad (2.30)$$

The values of ϕ_o for Si GaAs and GaP are very closed to one third of the band gap (Si = 0.3 eV, GaAs = 0.53 eV, GaP = 0.66 eV).

The current transport in metal-semiconductor barrier is mainly due to majority carriers and usually three approaches are used (1) isothermal thermoionic emission (2)isothermal diffusion theory and general theory which incorporates both.[8]

The complete expression of I-V characteristics may be written in the form

$$J = J_s \left[e^{qV/KT} - 1 \right] \qquad (2.31)$$

with

$$J_s = A\, T^2 \exp\left[-\frac{\phi_n}{kT} \right] \qquad (2.32)$$

2.7 SCHOTTKEY BARRIER HEIGHT MEASUREMENT:

Several experimental technique may be used to measure experimentally the barrier height parameter ϕ_n (V_n). Among them most important are

(1) Current-voltage measurement

(2) Capacitance-voltage measurement

(3) Photoelectric merriment

We briefly discuss the underlying principle of those technique.

(i) CURRENT-VOLTAGE MEASUREMENT:

A. Forward characteristics: If the Schottkey diode is forward biased, the current density, as discussed earlier can be given by

$$J = A\,T^2\,Exp\left(-\frac{\phi_o}{KT}\right)\exp\left(\frac{\Delta\phi + qV}{KT}\right) \qquad (2.33)$$

ϕ_o = zero-field asymptotic barrier height

A = effective Richardson constant

$\Delta\phi$ = Schottkey barrier lowering

As both A & $\Delta\phi$ are functions of applied voltage V, the I-V characteristics (for $V > 3KT/q$) is not represented by $\left(\sim\exp(qV/KT)\right)$ but rather by an empirical relation

$$J \sim \exp(qV/\eta KT) \qquad (2.34)$$

$$\text{Where } n = \frac{q}{KT}\frac{\partial}{\partial(\ln J)}V$$

$$= \left[1 + \frac{\partial\Delta\phi}{\partial V} + \frac{KT}{q}\frac{\partial}{\partial V}(\ln A)\right]^{-1} \qquad (2.35)$$

For W-Si and W-GaAs diodes n have been formed to be 1.02 and 1.04 respectively. Plot of log I vs V, should yield a straight iine, the intercept on the y-axis will give the value saturation current J_s and the barrier height can be obtained from the relation

$$\phi_n = kT\ln\left(\frac{AT^2}{J_s}\right) \qquad (2.36)$$

(ii) **CAPACITANCE - VOLTAGE MEASUREMENT:**

The relationship between C and V is given by Eq (2.26). So a plot of $\frac{1}{C^2}$ vs applied reverse voltage would yield straight line. The intercept on the voltage axis will give the net contact potential barrier at V = 0 volt. This intercept V_i will contain the term barrier height, lowering of Schottkey barrier, Volt-equivalent of temperature (V_T) and another rm V_{FC} (depth of the fermi level below conduction band) i.e.

$$V_{ib} = V_n - V_{Fc} + \frac{\Delta\phi}{q} - V_T$$

$$V_n = \frac{\phi_n}{q} = V_{ib} + V_{Fc} + V_T - \frac{\Delta\phi}{q} \qquad (2.37)$$

From where we may calculate V_n or ϕ_n, the barrier height. From the slope one can determine the carrier density. For Au- n-Si system a typical value obtained such materials may be in the range of 0.80 volt.

Since we have not made any photoelectric measurement, we refrain from its discussion.

CHAPTER THREE

IMPURITIES IN SEMICONDUCTOR

IMPURITIES IN SEMICONDUCTOR

We know that presence of impurities in semiconductor material greatly affect the electrical and optical properties of the materials and the device made out of it. Some of the impurities may act as recombination center via which recombination of electron and holes takes place. These impurity centers contribute electronic states in the energy gap of the semiconductor. These states may also be associated with imperfections in crystals. As for example gold is extensively used as recombination agent by semiconductor device manufactures.[9,10] In brief the impurity states generally affect the life time of the free carriers.

Impurity induced photoconductors are fairly wide applicants in various fields including detection of radiation, in the wave length from 10-100 μm at low temperature. Thus impurity or defects having energy levels deep in the semiconductor band gap may create desirable effect in electronic devices.

3.1 IMPURITY AND DEFECT CENTERS

Generation recombination centers in pn junctions play an important role in determining the current - voltage and capacitance characteristics of junctions. In general, these centers are most effective when located in energy somewhere near the center of the band gap because then communication between the

conduction and valence bands through the centers tends to be greatest. The generation-recombination centers may be impurity atoms located interstitially or substitutionally in the lattice or crystal lattice defects or surface effects.

The simple energy band structure of a semiconductor consists of two allowed energy bands, which are separated by the forbidden energy gap, with infinite dimension. Any disturbance of the crystal order by crystal defects or impurity atoms introduces additional energy levels either within the energy gap or within the bands. These energy levels are localized at the imperfection centers and have a significant effect on the crystal properties if they occur within the forbidden energy gap. The states in the gap between conduction and valence bands are placed in two categories: Shallow states and deep states.

3.2 SHALLOW STATES:

Shallow states are located near their related band edges (valence band for acceptors and conduction bands for donors). These states typically relate to substitutional impurities which possess a single excess (donor) or deficit (acceptors) valence electron structure relative to the atom replace in the host material. The ionization energy associated with shallow states can be approximately described by a modified hydrogenic model.

For example, the group (V) element As substituting in group (IV) host Si, is a shallow donors since As has one more valence electron than Si. The strength of the binding energy of the excess electron can be estimated in a model where the electron is acted only by singly charged nucleus. Because this hydrogen like structure is in a crystalline host rather than freespace, a modification by the reduced mass of electron and dielectric screening is included. The modified binding energy of a donor is[11]

$$E_D = \frac{1}{n^2 \epsilon^2} \left(\frac{m^*}{m_o}\right) 13.3 \text{ eV} \qquad (3.1)$$

where, m^* = carrier effective mass

m = free electron mass

ϵ = ratio of the dielectric constant of the host to that of free space.

n = an integer

It may be interesting to estimate the extent of the spread of the wave function of electrons or holes bound to such an impurity center. The Bohr's radius of our hydrogenic system can be expressed as

$$a_n = (m_o/m^*) \epsilon_s a_o n^2 \qquad (3.2)$$

where a_o is the Bohrh's first orbit radius in hydrogen atom. For As in Ge $a_1 \simeq 80\ a_o$ whereas in Si this is $30a_o$. We thus see the wave function is spread over many lattice spacings.

According to this formula shallow donor impurity possess localized energy levels E_D, lying within a few times the thermal energy kT of the conduction band at room temperature T = 300°K. Similarly group (III) element, Ga substituting in Si acts as an acceptor and the binding energy of the localized state associated with the impurity atom Ga lies in the forbidden band has the similar distance ($E_A \approx E_D$) from the valence band edge. At room temperature most of the impurity atoms (donors and acceptors) become ionized and the excess electrons or holes are no longer localized at the discrete impurity centers, but are promoted respectively to the conduction and valence bands of the host crystal, where they may contributed in conduction.

In standard nomenclature donor states are defined as those states which become more positively charged when ionized and acceptor states as those which become more negatively charged when ionized.

Energy level of some shallow impurity states are given below (with their ionization energy).

TABLE -1

Ionization Energies of Shallow Impurities in Silicon and Germanium

Impurity Element		E_i (eV)	
		Thermal	Optical
In silicon	Donors		
	Li	0.033	
	P	0.044	0.045
	As	0.049	0.053
	Sb	0.039	0.043
	Bi	0.069	
	Acceptors		
	B	0.045	0.046
	Al	0.057	0.067
	Ga	0.065	0.071
	In	0.16	0.154
In germanium	Donors		
	P	0.0120	
	As	0.0127	
	Sb	0.0096	
	B	0.0104	
	Acceptors		
	Al	0.0102	
	Ga	0.0108	
	In	0.0112	

3.3 DEEP LEVELS IN SEMICONDUCTOR AND ITS EFFECT ON SEMICONDUCTING MATERIALS AND THEIR DEVICES:

Deep states are most simply classified as those which are position deeper than corresponding hydrogenic states in the band gap. This definition includes donors which are near the valence band and acceptors which are near the conduction band. The large ionization of these states implies a strong potential acts to localize the carrier wave function near the site of imperfection or impurity center. The deepest states near center gap have generally the most localized electronic wave functions while shallow states have wave function extending over many lattice constant. Due to localization the deeper-laying impurity states act more often as electron or hole traps or recombination centers than as means to supply carrier to conduction or valence bands.

For example, let us take valence - six element substituting in Si. There are two electrons surplus over those needed to form the co-valent bonds of the host lattice. Both of these electrons can be donated to the conduction band. Because the nuclear charge is effectively +2e, the first ionization energy is generally higher than for a simple donor. The second donor electron is even more tightly bound. Similarly, valence two double acceptors have states correspond to single and double ionization. These states with large ionization energy controls the probability of trapping or recombination for an electron or hole normally come very close to them.

When the imperfection density is low, then they are far apart from one another and all states associated with particular electrons of a particular imperfection will have the same energy. When the density becomes so high that their localized wave functions appreciably overlap one another and the imperfection state energies will spread to form a band of imperfection states. This band would have a regularity like those of the host crystal itself and the imperfection states also permits the possibility of electron exchange between the states, even though the host crystal itself may be an insulator.

The energy levels associated with the impurities that produce deep energy levels may be associated with impurity complexes or impurity vacancy complexes and that the impurity may interstitial rather than substitutional. Even if attention is confined to substitutional type impurity there are considerable difficulties in applying the effective mass theory successfully. A direct approach at calculating deep impurity levels has been made by Glodeanu.[12,13] He considers bi-valent substitutional impurities that generate two localized energy levels in the forbidden band and uses a helium like model in a single-band approximation and calculates the deep donor and acceptor levels of impurities in semiconducting materials.

According to his theory, two ionization energies are

$$E_1 = a\left[Z_{eff} - \frac{5}{4} Z_{eff} + \frac{25}{128}\right] \qquad (3.3)$$

$$E_2 = a\, Z_{eff}$$

where $a \approx m^*/\epsilon_s$

$Z_{eff} \approx$ is a parameter fitted to the experimental result in such a way that standard error becomes minimum.

The determined values for Z_{eff} lie in a reasonable range, $2 \leq Z_{eff} \leq 3$.

The calculated and experimental ionization energies are given in Table-2. The depth of the donor levels is counted from the conduction band and that for the acceptor levels from the valence band.

Deep impurities may create desirable effects in devices. the use of gold gives fast recombination in Si junctions that require nanosecond switching tiqes. Impurity photoconductivity is a further important application of deep impurity effects in semiconductor. Semiconductors containing deep impurities are also of use as temperature sensors in thermistor type applications. Deep impurities also creates undesired trapping, oscillation and negative resistance effects in large band gap compound semiconductors and that can be source of considerable frustration to the would be user of these materials.

TABLE-2

Calculated and Observed Values of the Ionization Energy for Deep Impurities in GaAs, Si, and Ge

Crystal	Impurity	Type[b]	Z_{eff}	E_1(eV)		E_2(eV)	
				Calculated	Observed	Calculated	Observed
GaAs	Cu	A	2	0.171	0.15	0.407	0.47
Si	S	D	2.145	0.206	0.18	0.447	0.52
	Ni	A	2.380	0.280	0.23	0.550	0.70
	Co	A	2.515	0.328	0.35	0.614	0.58
	Zn	A	2.428	0.297	0.31	0.537	0.55
Ge	Se	D	2.275	0.138	0.14	0.285	0.28
	Te	D	2.195	0.124	0.11	0.262	0.30
	Mn	A	2.475	0.177	0.16	0.322	0.37
	Co	A	2.815	0.249	0.25	0.431	0.43
	Fe	A	3.060	0.312	0.34	0.509	0.47
	Ni	A	2.753	0.234	0.22	0.413	0.44
	Cr	A	2.580	0.068	0.07	0.123	0.12
	Cd	A	2.735	0.079	0.06	0.138	0.20
	Zn	A	2.050	0.034	0.03	0.078	0.09

b. A is acceptor; D is donor[19].

3.4 DEFECT STATES:

In a broad sense, a defect state may be defined as an electronic state introduced into the forbidden gap of a semiconductor as a result of a perturbation of the bonding structure of the host material by the presence of a lattice defect or impurity. Most crystalline materials far from perfect, even synthetically produced single crystals. Imperfections fall into two categories: those in which atoms are merely disarranged and those involving additional or missing atoms.

The electronic states associated with defects (lattice defect, point defect) and dislocations may be located in either allowed or forbidden bands of the host crystal. The depth of the state inside the forbidden band determines the nature of the imperfection centers. Dislocations are more effective as traps than are point defects.

There are essentially four process by which crystal defects can be formed: (1) as the result of thermal dissociation and disorder, when the material is heated to a high temperature (2) by exposing the material to an excess pressure of one of its constituents, usually at an elevated temperature ; (3) by incorporating impurities which require the simultaneous formation of crystal defects to permit their incorporation and (4) by bombarding with X rays or nuclear particles.

3.5 Trap:

A deeper lying imperfection center which is capable of trapping free-charge-carrier (electrons and holes) and keeping it for a mean life time and then ejects the carrier to the band from which it came is termed as trap. Traps interact mainly with one band - the conduction band or the valence band.A deep defect centre in a semiconductor may act either as a trap or as a recombination center, depending on the impurity, on the temperature and on the other doping conditions. Which role a center will play depends on the concentration of majority carriers and on the relative cross-section for capture of minority and majority carriers.

Imperfection centers are doubly charged and attractive to minority carriers are likely to act as traps. They will possess a large cross-section for the minority carrier but after capture will be repulsive to the majority carrier. This repulsion reduces the cross-section and causes the ejection of trapped minority carrier. Traps are two types: fast traps and slow traps. Fast traps return the carriers to the band in a short time (often as little as 10^{-7} sec) while slow traps may retain the carriers for seconds or even hours.

In terms of carriers capture or emission rate traps are classified as electron traps, hole traps, majority carrier traps and minority carrier traps. For a electron trap, electron capture

rate c_n or electron emission rate e_n is much larger than hole capture rate c_p or hole emission rate e_p. Similarly c_p and e_p are larger then c_n and e_n respectively for a hole trap.

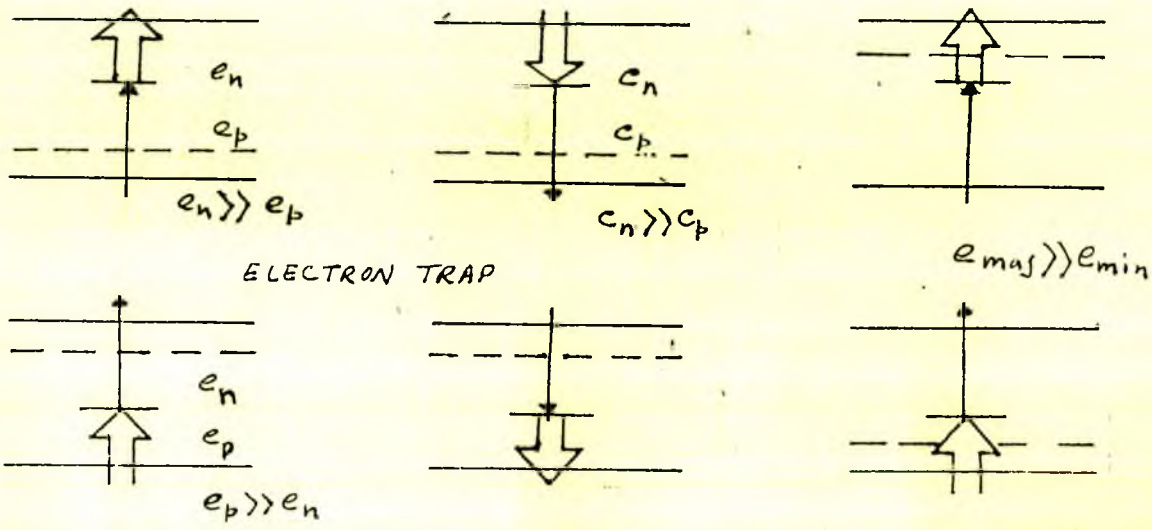


Fig. (14). Electron trap, Hole trap, Majority carrier trap and minority carrier trap.

3.6 CAPTURE RATE AND EMISSION RATE

(i) Capture Rate:

The capture rate c (cm^3 see^{-1}) of electrons (or holes) that is usually determined in an experiment is defined as follows. For electrons captured from the conduction band is written as

$$\frac{dn}{dt} = -cn\ N_T \qquad (3.4)$$

(here n = density of conduction electrons, N_T density of empty defect states that can capture an electron).

In Δt time, the number of electrons captured by N_T traps

$$\Delta n = n\sigma v_o \Delta t N \tag{3.5}$$

where σ is capture cross section for electrons, v_o velocity of electrons and E_o is the energy of electrons $\left[v_o = (2E_o/m^*)^{1/2}\right]$. Then for such a simple model, comparing Eq. (3.5) with (3.4), we get

$$\boxed{c = \sigma v_o} \tag{3.6}$$

More usually this is written as

$$\sigma = \frac{c}{v_{th}} \tag{3.7}$$

where v_{th} is the thermal velocity of free electrons and at temperature between $77^o$to 300^ok typically the value ranges from 10^6 to 10^7 cm/sec

The cross-section that we found experimentally fall in three categories: (i) the giant trapping cross-sections usually in the range $10^{-15}$to 10^{-12} cm^2 and associated with attractive centers, (ii) medium ranges cross-sections of 10^{-17} to 10^{-15} cm^2 associated with neutral centers and (iii) tiny cross-section 10^{-22} cm^2 are associated with repulsive centers. How giant cross-section are possible for attractive and neutral centers could not be explained readily. Lax's cascade theory of capture partially proved to be successful.[14,15] Lax's cascade model assumes that large cross-section are made possible by capture into excited states possessing large orbits. The large energy loss is possible by a cascade process involving the successive emission of single

phonons as the electron plummets down the excited states. Such excited states of large orbit are available to a coulomb attractive center and permit large cross-section that depend on the charge of the center. On the other hand, for neutral centers a moderately long range inverse-fourth power potential is available because of the interaction between the charge carrier and the polarizibility of the center. Since polarizibility of an atom varies inversely a$_o$ the square of the ionization energy and ionization energies of centers in solids are an order of magnitude lower than free atom ionization energy, large polarizibility results. These polarizibilities may be large enough to permit a ladder of excited states sufficient to allow a cascade process.

We must remember, however that for electron capture to be effective it must lose enough energy in a collision to go into a bound orbit. The energy can be taken away by (1) a photon (2)another electron hole (3) optical phonons (4) accoustical phonons. However neither the radiative capture nor Auger process (2) can explain the observed large cross-section. On the other hand optical phonons (3) make a significant contribution to the room temperature capture cross-section in Si and Ge. At low temperatures, at large distances from the trap, electrons will only have enough energy to emit accoustical phonons. The enormous cross-section in low temperature must then be associated with accoustical phonons(4).

From the foregoing discussion, we may say capture rate is the probability per unit time for a neutral defect to trap a free electron and for a negatively charged defect to trap a free hole. The electron and hole capture rates may be written as

$$\left.\begin{aligned} C_n &= c_n n = \sigma_n \langle v_n \rangle n \\ C_p &= c_p p = \sigma_p \langle v_p \rangle p \end{aligned}\right] \qquad (3.8)$$

Here, n and p are the concentration of electrons and holes. v_n is the average thermal velocity of electrons (v_p is of holes) and approximately given by

$$v_n \simeq \sqrt{\left[v_n^2\right]} = \sqrt{\frac{3KT}{m_e^*}} \qquad (3.9)$$

σ_n and σ_p are the capture cross-section of defect center for capturing electrons and holes.

The capture cross-section represents a geometrical area determined by the radius such that the probability of escaping from the center is equal to that of being finally captured. The capture cross-section of a center is determined by the potential variation in the neighbourhood of the center. The largest cross sections occur for charged centers which exert a coulomb attraction on free carriers. A simple estimate of σ can be made by

the formula,[16]

$$\frac{e^2}{r\epsilon_s} = KT$$

or at room temperature,

$$\sigma = \pi r^2 = \frac{10^{-10}}{\epsilon_s^2} \text{ cm}^2 \qquad (3.10)$$

The life time of a free carrier can be calculated from equation (3.8). The life time is the time that an excited electrons spends in the conduction band or the time an excited hole spends in the valence band.

$$\tau_n = \frac{1}{C_n} \qquad \left(\tau_p = \frac{1}{C_p}\right)$$

$$= \frac{1}{\sigma_n \langle v_n \rangle n} \qquad (3.11)$$

The life time of a free carrier can vary from 10^{-14} to 10^{3} sec.[16]

(ii) EMISSION RATE:

Emission rate is probability per unit time for an electron to go from trap level to the conduction band and a hole to valence band.

Thermal emission rates are proportional to a Boltzmann factor exp $(-\Delta E/KT)$, where ΔE is the depth of the trap (free energy) from band edge to which the carrier is emitted. Electron emission rate is

$$e_n = A_n \exp(-\Delta E/KT) \qquad (3.12)$$

where $\Delta E = E_c - E_T$ the thermal activation energy relative to band edge. A_n is a property of the particular defect and is given by

$$A_n = \frac{\sigma_n \langle v_n \rangle N_c}{g} \qquad (3.13)$$

Here, g is the generacy of the level and N_c is the effective density of the state at the conduction band edge. Generally, A_n[17] lies in the range 10^{11} - 10^{13}/sec.

The similar equation for hole emission rate is

$$e_p = A_p \exp(\Delta E/KT) \qquad (3.14)$$

here $\Delta E = E_T - E_v$

3.7 DECAY AND GROWTH EQUATION:

We noted earlier that an electron (or holes) may be emitted to the conduction band (valence band) emission rates are given by Eq.(3.12) and (3.14). This emission are thermal emission. However we may induce optical emission of carriers if the material is illuminated with light.

Let e_n° and e_p° are optical electron and optical hole emission rates. N_T and N are total concentration of defect states and states filled with electron. Then N_T - N are empty states (of electron).

Therefore, the net rate of increase of states filled with electrons can be immediately written as

$$\frac{dN}{dt} = \left(c_n + e_p + e_p^o\right)(N_T - N) - \left(c_p + e_n + e_n^o\right)N \qquad (3.15)$$

The first terms gives the no. of states filled with electron being increased in unit time and the second term gives the no. of states filled with electron being disappeared in unit time.

If we write

$$a = c_n + e_p + e_p^o \text{ and } b = c_p + e_n + e_n^o$$

the above equn. becomes

$$\frac{dN}{dt} = a\left(N_T - N\right) + bN \qquad (3.16)$$

We may solve the above equation under two boundary condition:

Case (a): at t=0 the traps are filled. For any other time t>0, we may try for a solution i.e.

$$N(t) = \left(\frac{a}{a+b}\right) N_T + \left(\frac{b}{a+b}\right) N_T e^{-(a+b)t} \qquad (3.17)$$

Case (b): at t=0, the traps are empty, then solution of Eq.(3.16) is find to be

$$N(t) = \left(\frac{a}{a+b}\right) N_T \left(1 - e^{-(a+b)t}\right) \qquad (3.18)$$

For thermal emission and capture process only we may neglect the effect of optical emission $e_n^o = e_p^o = 0$. In equations a and b will

involve only c_n, e_p and c_p, e_n. Usually in thermal process one of remaining four rates dominate. Thus for electron capture process into an initially empty electron trap follows for Eq. (3.17) ($a = c_n$, $b = 0$), we have

$$N(t) = N_T\left(1 - e^{-c_n t}\right) \tag{3.19}$$

and for subsequent emission process for this electron ($b = e_n$, $a = 0$)

$$N(t) = N_T e^{-e_n t} \tag{3.20}$$

The capture and the emission process by a single trap level is shown in fig.(15)

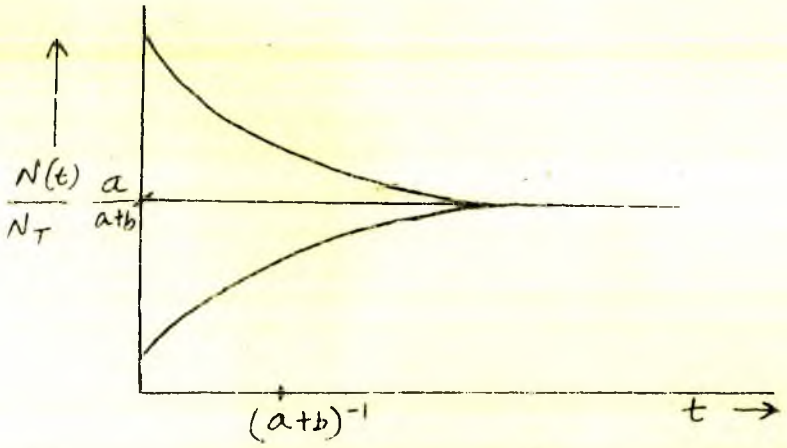


Fig.(15) Capture and emission processes.

3.8 RECOMBINATION CENTER:

A defect capable of trapping an electron and subsequently a hole or vice-versa, the result being the recombination of a pair of free carriers, is termed recombination center. To provide a recombination center for an electron hole pair the defect should effectively interact with both bands.

Imperfection centers that are singly charged and attractive to minority carriers are likely to act as recombination centers. Since the cross-section for the subsequent neutral capture of a majority carrier may only be one order of magnitude lower than the minority carrier-cross-section, and the number of majority carriers may be sufficiently large that recombination will occur before ejection. For a recombination center both the electron and hole capture rates are large.

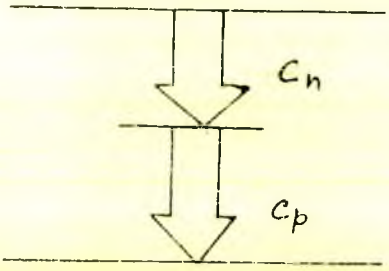


Fig. (16) Recombination at a defect center.

If the semiconductor contains a concentration N_T of defects whose energy level E_T be inside the forbidden band and are not occupied by electrons (are occupied by holes), then several process illustrated in Fig.(17) below are possible:

(a) a free electron is trapped by a neutral defect

(b) a free electron after spending sometime trapped on the defect level, again becomes free

(c) a free hole is trapped by a neutral defect

(d) a trapped hole becomes free

(e) an electron is trapped from the conduction band and the neutral defect becomes negatively charged and then traps a

free hole. The result is a recombination process of a electron-hole pair.

(f) By trapping a free hole a neutral defect becomes positively charged and traps a free electron i.e. a recombination process.

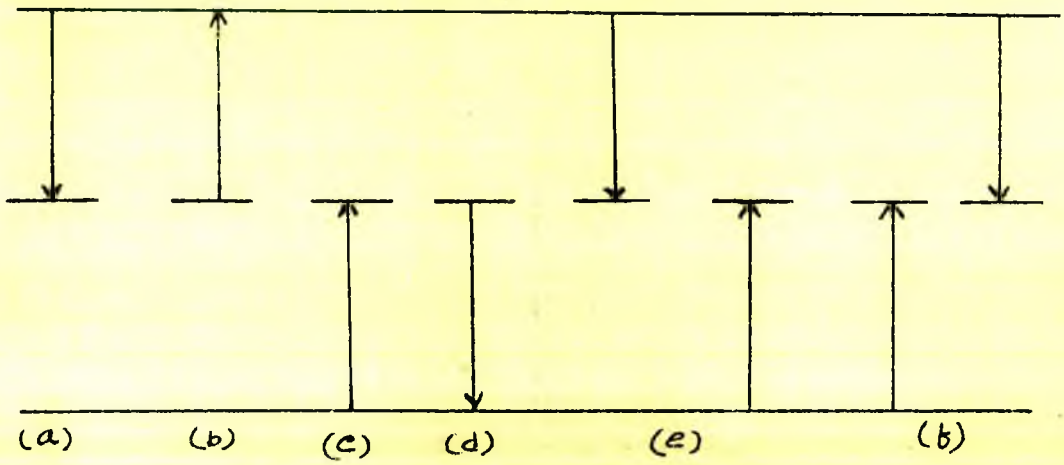


Fig. (17) Process of trapping and recombination at a defect level.

3.9 LIFE TIME OF CARRIERS AND RECOMBINATION PROCESS:

If the thermodynamic equilibrium of a semiconducting material is disturbed, non-equilibrium charge carrier are created and after surviving for a time they are annihilated by recombination processes. The energy released by the recombination is emitted as a photon or phonons. When a photon is emitted, the process is called radiative recombination. Nonradiative recombination emits phonons to the lattice in the form of heat dissipation. The most important recombination processes are the direct and indirect recombination.

An electron in the conduction band may make a transition directly to the valence band to recombine with a hole. This process is called the direct or band-to-band recombination. Direct recombination plays the leading role in solids of narrow forbidden band width of the order of 0.2 - 0.3 eV.[18] The carrier life time τ depends on thermal equilibrium carrier densities n_o, p_o and the probability co-efficient of recombination τ represents the average time a carrier remains free before it recombines.

In a semiconductor with a direct energy band structure such as GaAs, the band to band recombination is the dominant mechanism. The energy released by the recombination is emitted in the form of photons and for this reason, GaAs is used to fabricate light emitting devices.

In indirect band structure materials recombination occurs via an intermediate states. This type of recombination is termed as indirect recombination. For forbidden band width in excess of 0.5 eV indirect recombination occurs.

Let us consider a material with traps concentration N_T and of energy levels E_T. The number of occupied centers is therefore $N_T f_T$ and the number of empty centers is $N_T (1-f_T)$. Here, f_T is the electron distribution function of defect level E_T. The capture rate of an electron by an empty center is

$$R_1 = c_n n N_T (1-f_T) \qquad (3.21)$$

Where n is the electron density in the conduction band and c_n is the electron capture probability.

The emission rate of an electron to the conduction band from an occupied centers may be written as

$$R_2 = e_n N_T f_T \qquad (3.22)$$

[e_n is the emission probability]

The emission and capture rates of holes by the centers are,

$$R_3 = c_p N_T f_T \qquad (3.23)$$

and $$R_4 = c_p N_T (1-f_T) \qquad (3.24)$$

Under steady-state condition,

$$R_1 - R_2 = R_3 - R_4 \qquad (3.25)$$

Using all the above equations. We get,

$$f_T = \frac{n + n_i \exp\left[(E_i - E_T) \,/\, KT\right]}{n + p + 2n_i \cosh\left[(E_T - E_i)/kT\right]} \qquad (3.26)$$

[By assuming $c_n = c_p = c$]

Therefore, the net recombination rate is

$$U \equiv R_1 - R_2 = \frac{cN_T\,(pn - n_i^2)}{n + p + 2n_i \cosh\left[(E_T - E_i)/KT\right]} \qquad (3.27)$$

From equation (3.27), we find that at equilibrium, that is, $pn = n_i^2$, the net recombination rate is zero. It is also

interesting to note that the maximum recombination rate occurs when $E_T = E_i$ i,e. when the centers are located at or near the center of the forbidden gap. Away from the level E_i, the centers would be less effective because it is more probable to capture the other type.

For an n-type silicon with a center located at E_i, the net recombination rate for low-level injection ($n_n \approx n_{no}$) is,

$$U = c_p N_T \left[p_n - p_{no}\right] \tag{3.28}$$

And the carrier life time, τ_p is

$$\tau_p = \frac{1}{c_p N_T} \tag{3.29}$$

The life time τ_p is independent of the capture of the majority carriers since they are abundant and the limitation of recombination rate is the capture of minority carriers. Therefore, τ_p is also called the minority carrier lifetime[19].

Similarly for a p-type semiconductor, the electron life time is

$$\tau_n = \frac{1}{c_n N_T} \tag{3.30}$$

In the following section we give a brief resume of some important deep impurity centers dopped in Si and Ge.

3.10 DEEP IMPURITIES IN Si & Ge:

The energy levels of impurities depend on how well these

impurities fit the electronic and geometric periodic pattern of the host lattice and are thus determined by the

(i) lattice position

(ii) lattice size

(iii) electronic shell structure of the impurities

(iv) solid solubility

We should also note that, the tendency to form or precipitates upon cooling, or the presence of the same impurity in different lattice sites may result in varying proportion of electrically active and inactive species.

1) **Si: Impurities of gr. I, II, & III :**

The number and type of impurity energy levels follow a few simple rules.

i) Substitutional impurities of group II and III tend to complete the tetrahedral bonding, need electron to do so and therefore act as acceptor.

The depth of the acceptor level appears to increase within group III as the row number increases.

group III	(eV)	
B	0.045 (v)	acceptors
Al	0.057 (v)	
Ga	0.065 (v)	
In	0.16 (v)	deep acceptor levels.
Tl	0.26 (v)	

This may be due to repulsion between the electronic making it less favourable for electrons to complete the tetrahedral bonding.

group II

Zn	0.55 (c, a)
	0.31 (v, a)
Hg	0.31 (c, a)
	0.36 (c, a)
	0.33 (v, d)
	0.25 (v, d)
Mg	0.11 (c, a)
	0.25 (c, a)
Cd	0.45 (c, a)
	0.55 (v, a)

Here the letters c, v indicates whether the energy has been given with respect to the conduction band or valence band edges and the letters a, d for acceptors and donors.

group I :

	eV
Ag	0.32 (v, d)
	0.22 (c, a)

Au Gold is the impurity that has been the subject of most study in silicon because it has considerable technological importance as a life time control impurity. It has two important

levels (1) 0.35 eV (v,d) and (2) 0.54 eV (c,a). Gold diffuses somewhat faster than does silver in silicon. The electrically active solubility is limited to about 10^{17} cm^{-9}. Although the tetrahedral radii of Cu, Ag and Au (1.35, 1.53 and 1.50Å) do not follow their position in the periodic table the energy levels of these substitutional impurities obey a reasonable sequence namely,

Cu	0.52 (v, a)
	0.37 (v, a)
	0.24 (v, a)
Au	0.54 (c, a)
	0.35 (v, d)
Ag	0.29 (c, a)
	0.32 (v, d)

Table-3, shows some of reported energy levels in Silicon.

2) **Ge : group I, II, III impurities:**

The group III elements B, Al, Ga, In are shallow impurities in germanium. The levels are in the range 0.0096 to 0.013 eV and are considerably shallower than the levels of the same impurities in silicon. The solid solubilities tend to be less in germanium than in silicon, both for shallow and deep impurities. Most of the deep impurities are faster diffusers then the shallow impurities by many orders of magnitude. However it seen that both Au and Zn

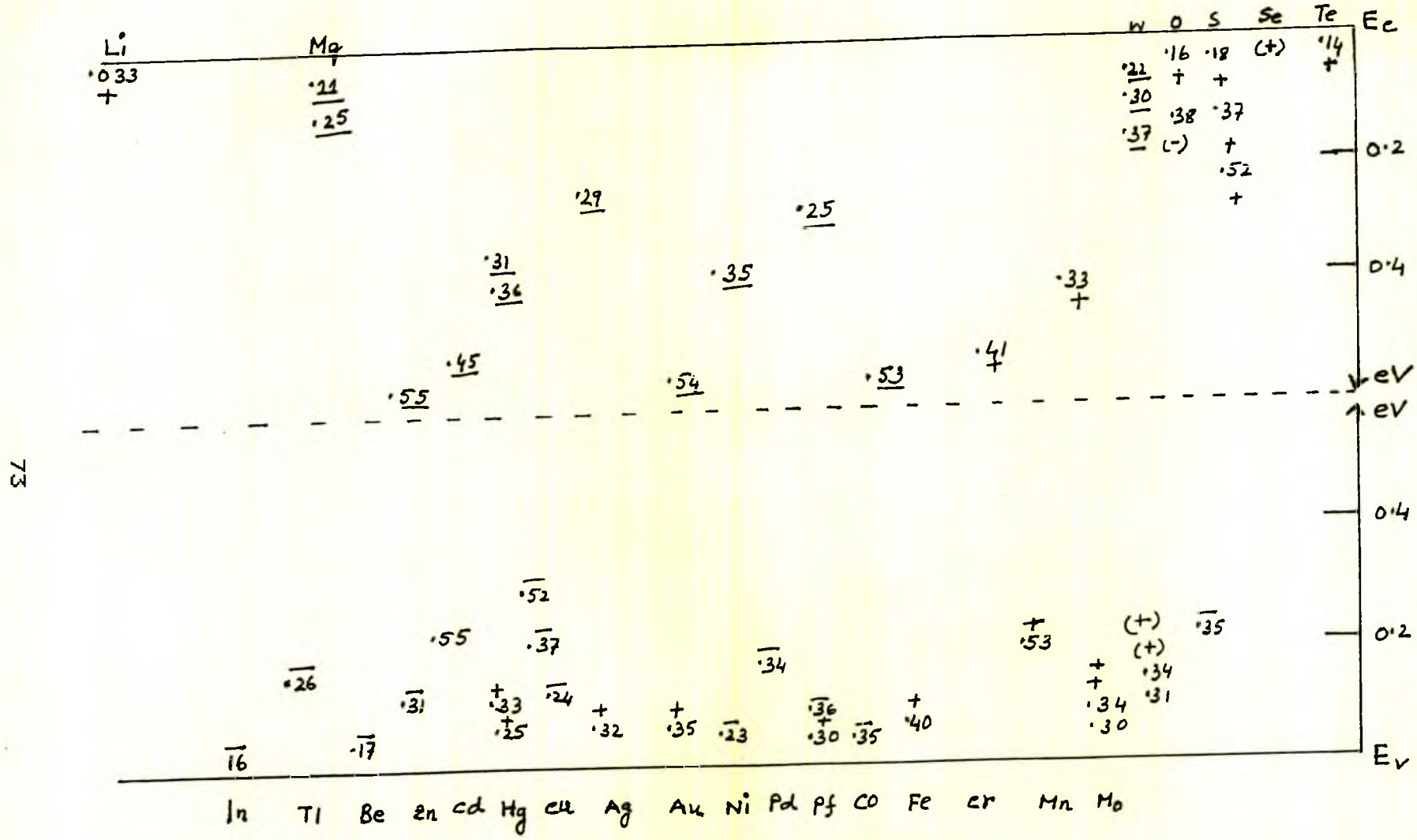


Table:3 Deep energy levels in silicon.

are much slower diffusers in germanium than in silicon because substituted action is present in germanium to a greater extent than in silicon

gr II elements

Be	0.02 (v, a)
	0.06 (v, a)
Zn	0.095 (v, a)
	0.035 (v, a)
Cd	0.05 (v, a)
	0.16 (v, a)
Hg	0.23 (v, a)
	0.087 (v, a)

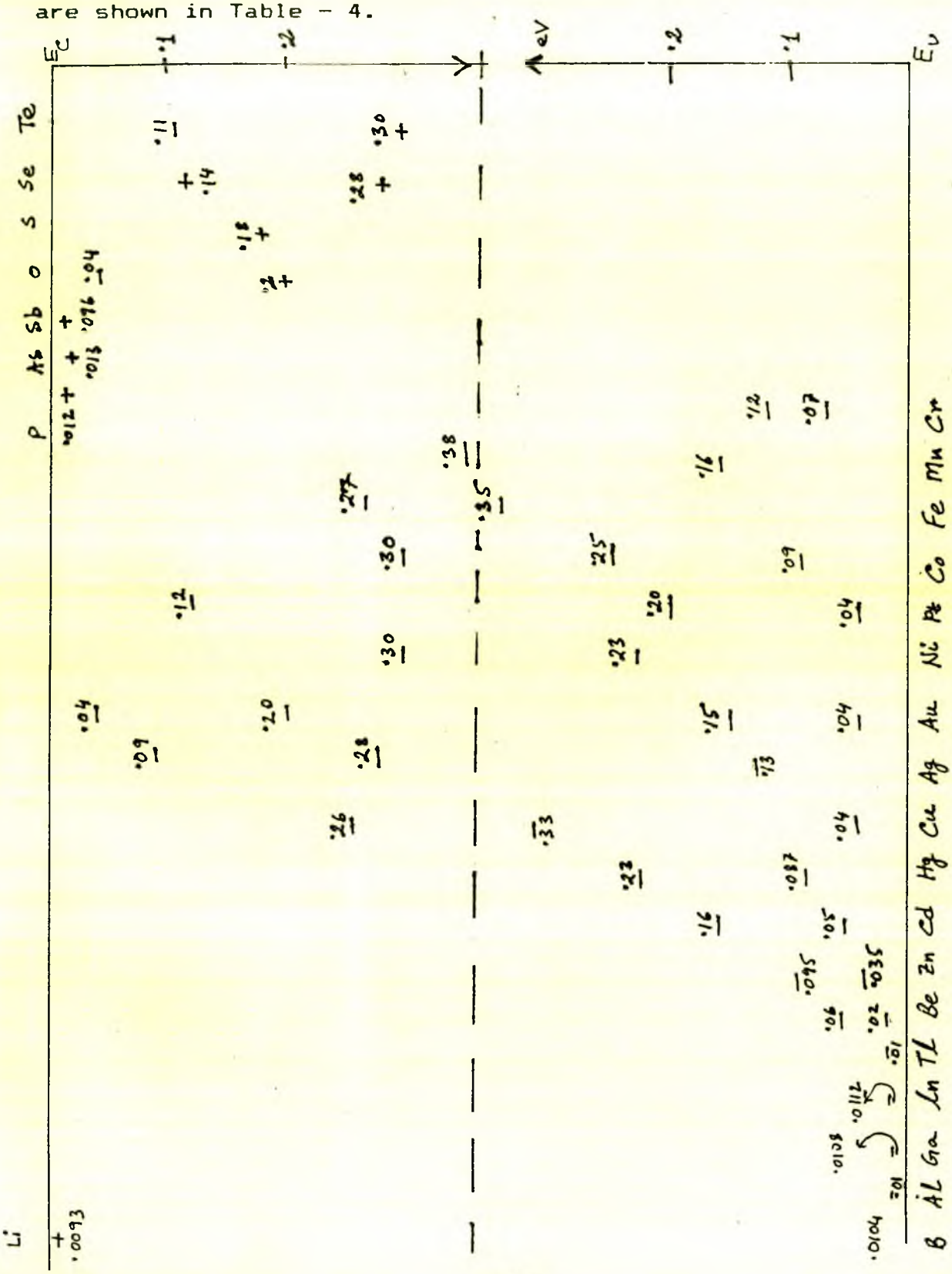
group I Water absorbed on the surface of germanium produces recombination centers. The presence of atomic hydrogen germanium surfaces results in fast recombination surfaces states, even though hydrogen in the bulk germanium is not active.

Interstitial Li is a shallow donor in germanium (0.00093 eV). Silver in germanium is a triple acceptor with levels at 0.13 eV (v, a), 0.28 eV (c, a) and 0.09 eV (c, a).

Gold in germanium has a very deep donor level and three acceptor levels

Au	0.04 (c, a)
	0.20 (c, a)
	0.15 (v, a)
	0.04 (v, d)

The energy levels of shallow and deep impurities in germanium are shown in Table – 4.



3.11 DEEP STATES IN SPACE-CHARGE REGION:

For simplicity we will limit our discussion to one-sided step junction or Schottky barrier structure. As reverse bias is applied, a region depleted of mobile free carriers is created predominantly on the lightly doped side of the junction. The depleted region is characterised by a space charge of ionized dopant.

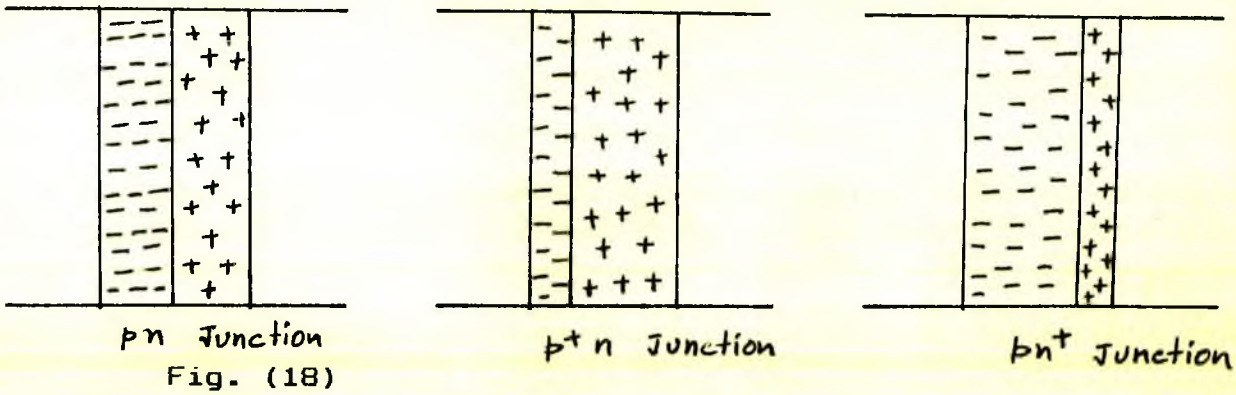


Fig. (18)

Thus for an abrupt p^+n junction ($N_A >> N_D$) a predominantly positive space charge region exists (Fig b). Following fig. gives an elaborate picture when we apply an external reverse bias voltage V.

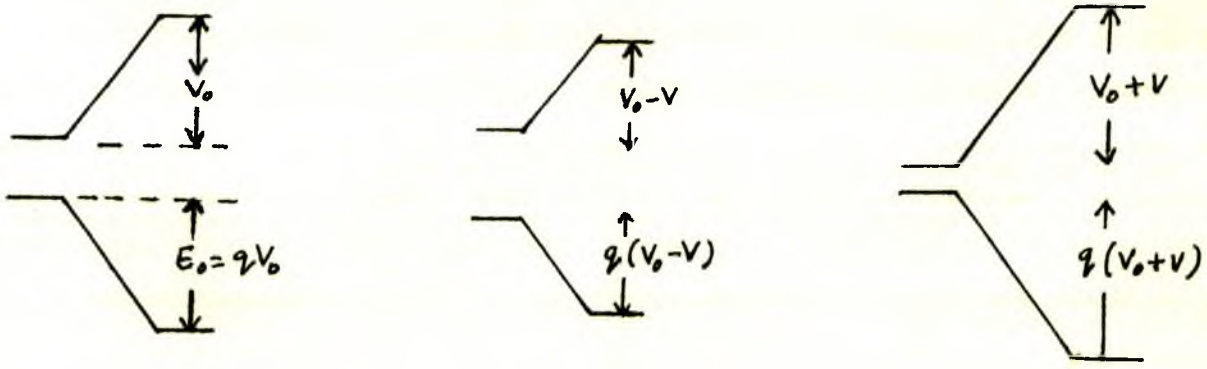


Fig. (19)

V_o in the above picture denote the intrinsic contact potential. Let us now consider such a junction p^+n with a deep level E_T. (donor and acceptor state). We depict the picture of the electronic structure below.

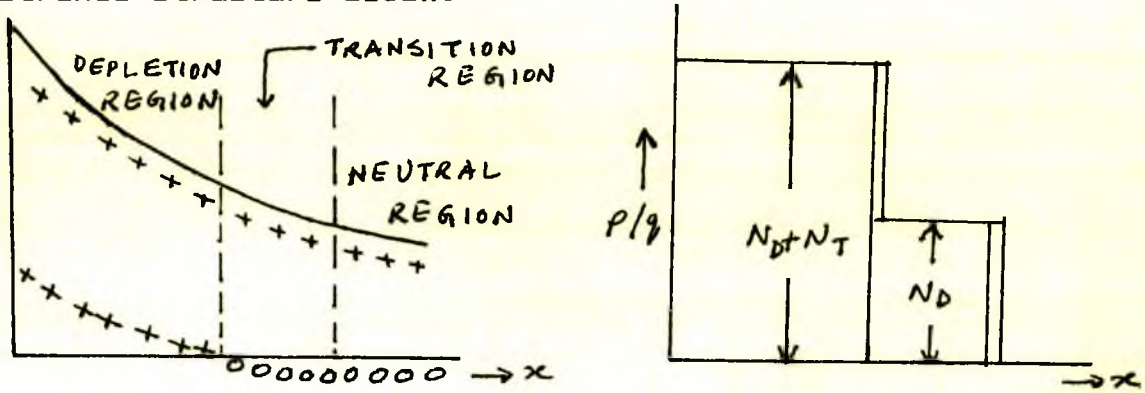


Fig. (20) (a) (b)

Fig. (20). Deep donor traps in a p^+n junction.

The unique feature of a structure with deep state is the transition region $y < x < w$. Transition region is the boundary layer between the neutral and depletion regions, it is usually smaller than depletion region. In this region, generation, recombination processes are both active in determining the equilibrium occupation of defect states. The more general case is the region $o< x <y$, which is totally depleted of mobile carriers and in which defect state occupation is controlled only through emission process, since capture rate is zero. The region $x > w$ is neutral material and away from the junction in which the space charge of ionized dopant is exactly canceled by the presence of mobile carriers. The space-charge non-uniformity may be

represented to a first order by step functions as shown in fig (20) b.

The leading edge of the depletion region is not abrupt by is marked by the spill-over of electrons from the neutral region, which is truncated with the characteristic Debye screening length,

$$L_D = \left[\frac{kT\epsilon_s}{q^2 n}\right]^{1/2} \qquad (3.31)$$

[L_D is the measure of the sharpness of the depletion edge]

The physical basis for this spillover concentration is a balance of the diffusion of free carriers from the neutral region against the retarding potential of the depletion region. When deep states are present this distribution of carriers defines a steady state occupation within the depletion region.

The frequency and transient response of a junction structure are directly related to the two depleted regions : transition region and space charge region.

3.12 EFFECT OF DEEP IMPURITIES ON JUNCTION CAPACITANCE:

We mentioned earlier that the reverse-biased capacitance of an abrupt p^+n junction depends on the depletion width W which infect resides in the lightly doped side of the junction. If this is determined by the shallow donors N_d only, then the capacitance of the junction is given by

$$C = \frac{\epsilon_s}{W} A = A \left[\frac{q\epsilon_s N_d}{2(V_i + V)} \right]^{1/2}$$

$$= A \left[\frac{q\epsilon_s N_d}{2V_B} \right]^{1/2} \qquad (3.32)$$

with $V_B = V_i + V$, (V = applied reverse bias and V_i is the intrinsic barrier).

Usually depletion capacitance is measured at some fixed voltage by superimposing a small oscillating voltage (ΔVosc) and making a bridge measurement. The above equation is valid only if the edge of the depletion region follows the frequency of the superimposed a.c. voltage. If amplitude of the a.c. voltage is small, depletion width W remains same approximately. If there are deep impurities as shown in fig. (20), the oscillating voltage will uncover charge at both W and y. At W free carriers are swept away and at y, electrons are emitted the conduction band (and swept away) from traps at E_T. If the frequency of oscillation is slow, then the traps N_T, at y can follow the voltage variations by emission and capture processes. In the case of acceptors, for example, both charge $N_d - N_T$ (at W) and N_d (at y) contribute so the measured capacitance depends primarily on N_d. the condition may be shown as:

(i) $e_n > \omega$; ω is the oscillating voltage frequency and e_n is the emission rate of electrons from the trap E_T. (see Eq.3.12).

However if oscillation frequency is significantly high i.e.

(ii) $e_n < \omega$,only the untrapped charge at W can respond and the capacitance depends on $N_d - N_T$. Thus if the trap level is an acceptor level the capacitance at low frequency is greater than that measured with high frequency. Similar effect should also be observed for electrons trap E_T. This frequency effect on junction capacitance then can be employed to detect states by observing capacitance steps in capacitance frequency behaviour or a peak in the admittance Vs frequency[20,21]. The effect of frequency response has been studied for a Au-dopped Si-p^+n junction between frequency range 10Hz-30MHz at room temperature.

Dopping of gold as an impurity in p^+n system creates two levels in the forbidden gap E^-_{Au}, the acceptor level and a donor level E^+_{Au}. Energy and charge diagram for the junction with impurity levels are shown in fig. (21).

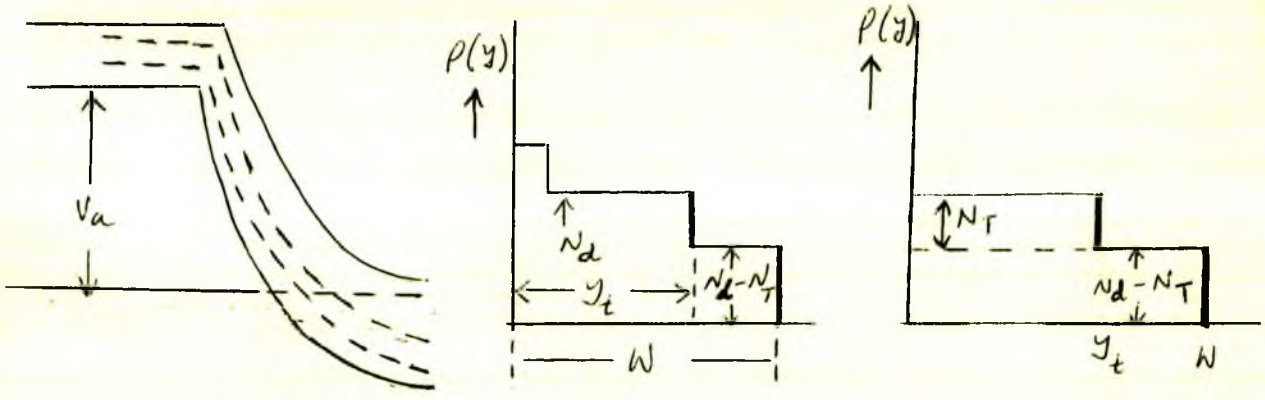


Fig. (21)

For very low frequency or dc junction capacitance

$$C_{dc} = \frac{C_o}{\left[1-(N_T/N_d)(\phi_t/q)/(V_i+V)\right]^{1/2}} \qquad (3.34)$$

with

$$\phi_t = \left(E_F - E_{Au}^-\right);\ C_o = \left[\frac{q\epsilon_s N_d}{2(V_i+V)}\right]^{1/2} \text{ i.e.} \qquad (3.35)$$

the capacitance without the impurity states. The corresponding depletion width is found to be

$$W = y_t + \left[\frac{2\epsilon_s \phi_t}{q^2(N_d-N_T)}\right]^{1/2} \qquad (3.36)$$

The frequency range for which the gold acceptor centers in the region near y_t can not respond is of interest. In this case time constant is long (~0.005 sec). At the depletion edge region (y=W), however, the free carriers present allow charging and discharging time constants of the order of 10^{-6} - 10^{-10} sec. Therefore there is a hf range for which the gold does not charge and discharge at y_t, but does follow at the depletion edge W. The capacitance in this frequency range is given by

$$C_{ac} = \frac{dQ}{dV(W)} = A\frac{\epsilon_s}{W} \qquad (3.37)$$

The expression for depletion width W is

$$W = \frac{N_T}{N_d}\left[\frac{2\epsilon_s \phi_t}{q^2(N_d-N_T)}\right]^{1/2} + \left[\frac{2\epsilon_s (V_i+V-\phi_t(N_T/N_d)}{q^2 N_d}\right]^{1/2} \qquad (3.38)$$

The capacitance C_{ac} then can be written as,

$$C_{ac} = \frac{C_o}{\left(N_T/N_d\right)\left\{\left[N_d/(N_d-N_T)\right]\left[\frac{\phi_i}{q(V_i+V)}\right]\right\}^{1/2} + \left[1-\left(N_T/N_d\right)\frac{\phi_i}{q} / \left(V_i + V\right)\right]^{1/2}} \qquad (3.39)$$

Sah and Reddi's model as described here is found to agree with experimental result. The bias dependence expected from the theory is given by

$$\left(\frac{C_{as}}{C_{dc} - C_{ac}}\right)^2 = \frac{N_d}{N_T}\left(\frac{N_d}{N_T} - 1\right)\left(\frac{V_i+V}{\phi_i/q} - \frac{N_T}{N_d}\right) \qquad (3.40)$$

This predict a linear dependence of $\left[C_{ac} / \left(C_{dc} - C_{ac}\right)\right]^2$ on (V_i+V). Thus experiment with variable frequency may be employed to study to presence of deep level defects in semiconductor.

However as the capture rate state are temperature dependent variation of the junction temperature which monitoring the depletion capacitance at a fixed frequency, can often give the same information as frequency response. The method employed is called the space charge spectroscopy and is described in the following chapter.

CHAPTER FOUR

THERMALLY STIMULATED RELAXATION

4.1 Introduction:

In investigating defect states in the forbidden gap, the carrier populations of such states can intentionally be altered thermally, optically or electrically. The resulting physical effects can be monitored in a variety of ways using suitable experimental technique. Whenever the thermal equilibrium of a physical system is disturbed, there are processes by means of which the system tends to revert to equilibrium and the return proceeds with a characteristic time constant τ, termed relaxation time.

For the occurrence of thermally stimulated relaxation process two basic conditions have to be fulfilled.

(i) The system must be removed from statistical thermodynamic equilibrium and exists in a state which requires the reactants to surmount a free-energy barrier in order to move toward the re establishment of equilibrium

(ii) The system must be in contact with a temperature reservoir that provides the thermal energy necessary to activate the relaxation process.

In thermally stimulated relaxation process, the sample is excited by illumination, current or voltage transient. The temperature at which this step takes place must be low enough, so that equilibrium is reestablished very slowly. The sample is then heated at a linear rate and the variation in capacitance, conductivity or the emitted light, resulting from return to

equilibrium, is monitored against temperature. Comparison of this measurement with one done without the initial excitation, shows the presence of current, capacitance or glow peaks associated with the emptying of traps within the semiconductor. It is then possible to determine the position of these trap levels within the energy gap. From the experiment the density of the traps or their capture cross-sections may sometimes be determined, although not usually with great accuracy.

4.2 SPACE-CHARGE SPECTROSCOPY:

A space-charge layer is depleted of mobile carriers and hence is very much like the bulk insulator. The existence of a space-charge layer at a p-n junction or Schottky barrier is a general characteristics of semiconductors. Such a layer is necessary to create the electrostatic potential variation needed to counteract the diffusion process of the carriers across the junction and maintain thermal equilibrium. We may think of a semiconductor "space-charge layer" as somewhat like a variable width insulator, typical thickness being in the range of about[22] 0.1 to 10μm. With reverse bias voltages of 1-100V the maximum electric field F_m in the layer is of order 10^4 - 10^5 V/cm.

We however note that there are two principal differences between space-charge layers and bulk insulators.

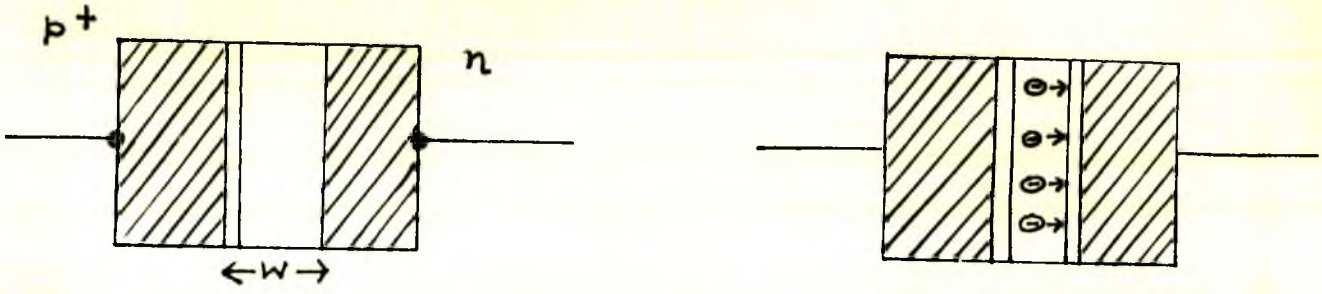
(i) The width of the layer can be readily adjusted by varying the bias voltage according to equation (2.8 & 2.21).

$$C = \frac{\epsilon_s A}{W} \qquad (4.1)$$

(ii) A large spatially varying electric field exists in the space-charge layer even at zero applied bias. The large electric field means that carriers thermally emitted from traps in the space-charge layer are swept out of the layer in a very short time, typically[22] 10^{-10} to 10^{-12} sec . Therefore, retrapping effects can be neglected and the analysis of thermal emission transients is considerably simplified as compared to bulk phenomena.

4.2.1 Capacitance and Current Detection of Trap Levels:

Trap levels in space-charge layer may be detected either by their effect on the junction current or on capacitance (Fig.22).



(a): Capacitance measurement

(b): Capacitance discharge (current) measurement.

Fig. (22)

For simplicity we take an asymmetric p^+n junction as an example. The current detection case is almost exactly analogous to the thermally stimulated trap-emission current which would be seen in a very thin bulk insulator in the absence of retrapping. The capacitance-detection case, yields the same basic physical information about traps, and is unique to space-charge layers and has no analogy in the bulk insulator case. The space-charge-layer capacitance is a direct measure of the total charge in this layer, because a change in charge density in the space-charge layer induces a corresponding change in width and capacitance of the layer.

In thermally stimulated conductivity one measures the free carrier concentration and infers from this the properties of traps and recombination centers. In junction capacitance measurements on the other hand one directly measures the trapped carrier concentration. The trap signals are more-or-less independent from each other and the analysis is considerably simplified. When trap induced capacitance charge ΔC is much less than total junction capacitance C ($\Delta C \ll C$), the thermal emission capacitance transients are simple exponent decays.

4.3 TRANSIENT CAPACITANCE PHENOMENON:

4.3.1 Measurement of Junction Capacitance:

In actual measurement junction capacitance is measured by superimposing a small alternating voltage ΔV_{osc} on the reverse

bias battery level of voltage (V_R) and making a bridge measurement. The depletion width remains constant and the junction capacitance

$$C = \frac{\Delta Q}{\Delta V} \qquad (4.2)$$

is determined by measuring the current induced by oscillating voltage; Eq.(2.8)

$$C = A \left[\frac{q\epsilon_s}{2V_B} N_B \right]^{1/2}$$

is valid if the edge of the depletion region follows the frequency of the applied ac voltage.

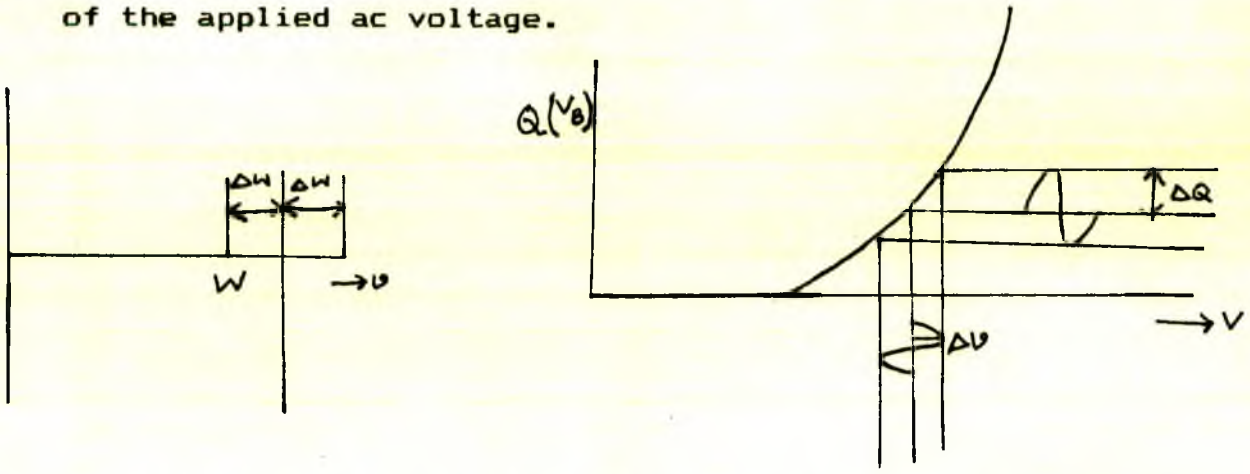


Fig.(23): Oscillating voltage applied on a junction

As discussed earlier, we note that when deep levels are present ΔV_{osc} will uncover charges at both W and y. At W free carriers are swept away and at y, electrons are emitted to the conduction band from traps E_T. If the voltage oscillations are slow $\left[\omega(\Delta V_{osc}) < e_n\right]$, then the traps N_T at y can follow the voltage

variations by emission and capture processes. In the case of acceptor both charge at W, $(N_D - N_T)$ and y, N_D contribute so that the measured capacitance depends primarily on N_D.

At sufficiently high frequencies $\left[\omega(\Delta V_{osc}) > e_n\right]$ only the untrapped charge at W can respond and the capacitance depends on $N_D - N_T$. Hence, the measurement frequency should be high enough (typically 1 MHz) so that the oscillating voltage applied to the junction by the capacitance bridge is unable to induce charges in the occupancy of the deep levels.

As discussed in the preceding chapter, the frequency effect can be used to detect defect states by observing steps in capacitance vs frequency behavior or a peak in the admittance Vs frequency characteristic. Because the rates of defect state capture and emission processes are temperature dependent, variation of the junction temperature, while monitoring the junction capacitance at constant frequency, can often give the same information as frequency response. However temperature variation also effects the equilibrium Fermi level according to the relation,

$$E_F = kT \ln (n/N_c) \qquad (4.3)$$

As temperature is increased, E_F may cross a defect state. Under the condition $\omega(\Delta V_{osc}) > e_n$, a capacitance step will be observed due to an increase in the free carrier density rather than a phase lag in the charging and discharging of defect states.

Fig (24) summarises the capacitance vs temperature behaviour of a junction containing a deep defect state.

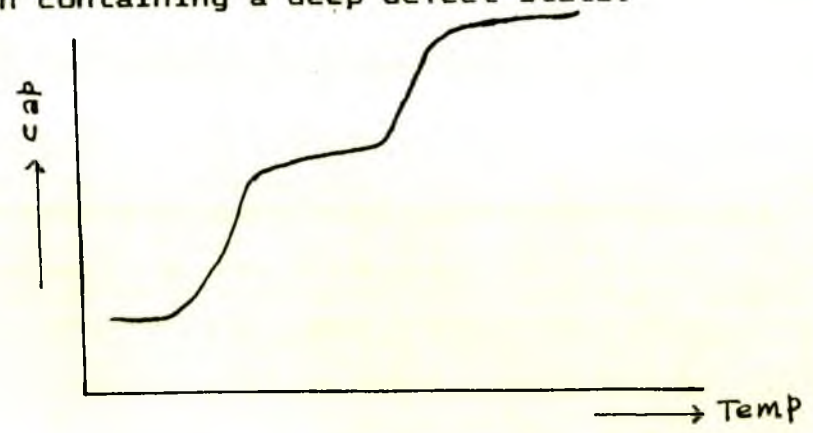


Fig. (24): Capacitance Vs temperature curve of a junction.

The basis of the technique to measure the free carrier distributions by junction capacitance measurements is the measurement of junction capacitance C and the slope $\Delta C/\Delta V$ as the reverse bias V_R is increased. In the most usual form of measurement ΔC and ΔV are derived from a point by point measurement of C versus V_R curve.

Alternative profiling technique have been reported in which ΔV_R is varied at rates 300 Hz and 5 MHz. The junction structure responds to the variation in bias voltage in the same manner as for the small ΔV_{osc}. In all measuring systems the range of frequencies employed such that,

$$0 < \omega \left[\Delta V_R\right] \leq \omega \left[\Delta V_{osc}\right]$$

where, $\omega \left[\Delta V_R\right]$ => frequency at which reverse bias varied

$\omega \left[\Delta V_{osc}\right]$ => oscillating frequency of the measuring-capacitance bridge.

4.3.2. Transient Response:

The depletion region of p-n junction is almost devoid of mobile carriers. In this region defect states occupation is controlled only through emission processes, since the capture rate is zero. All defects are traps in a truly depleted layer, as recombination cannot occur. Under conditions where the volume of the space charge region being much greater than the volume of the transition region, the junction response may be interpreted in terms of emission rates (see Eq.3.12). Emission processes can only be observed following the forced introduction of carriers which are to be captured. This preparation of defect charge states is most conveniently accomplished by pulsing the junction bias.

Let us take an abrupt p^+n junction, with a deep state E_T of concentration N_T. The depletion layer under reverse bias condition is entirely space-charge region and lies almost in the lightly doped semiconductor side.

Under such circumstances, the electronic structure is shown in Fig.(20).

On the n-side (neutral region) of the junction the trap level E_T lies much below the Fermi level E_F and the defect centers in this region facilitates the recombination of the injected holes with electrons

In the junction region, we get a transition region where the Fermi level is closed to E_T. On the left, E_T will be empty of electrons and on the right E_T's are filled. Usually the transition

region (W-y) is small and can be neglected in comparison to space charge region (y). If E_T is a donor state the impurity atoms in space charge region will be completely ionized, whereas in the transition region and neutral region these are neutral occupied by electrons. On the other hand if the E_T is an acceptor state, in the space-charge region they are neutral whereas they are negatively charged in transition and neutral region of n-type material.

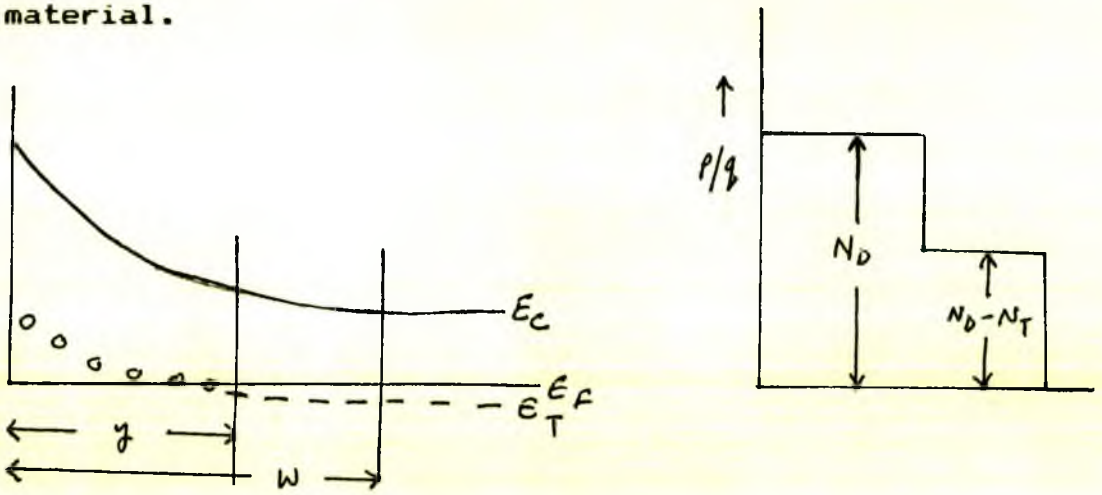


Fig.(25): p^+n junction with deep acceptor traps.

Thus we see that the depletion region have charge distribution (N_D+N_T) for donor state and N_D for acceptor state in space charge region and N_D (donor state), (N_D-N_T) (for acceptor state) in the transition region.

Now, let us see the effect due to pulsing junction bias. The depletion region here is in the n-type material and we have electrons as the majority carriers.

Step 1: Initially the junction is under reverse bias (V_R) , to establish space-charge dominant conditions. States in this region are empty because no mobile carrier are available for capture. The capacitance of the junction now is given by,

$$C_R = \frac{\epsilon_s A}{W_R} \qquad (4.4)$$

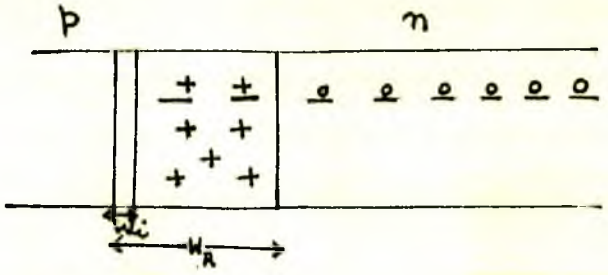


Fig. (26a)

Step 2: Now a positive bias pulse will momentarily collapse (toward the junction) the space charge region, making majority carriers available for capture. The capacitance increases rapidly as depletion width reduces to W_i from W_R. Here, $C_i = \frac{\epsilon_s A}{W_i}$;and

$C_i >> C_R$, $V_B = V_i + V_R - V_{inj}$

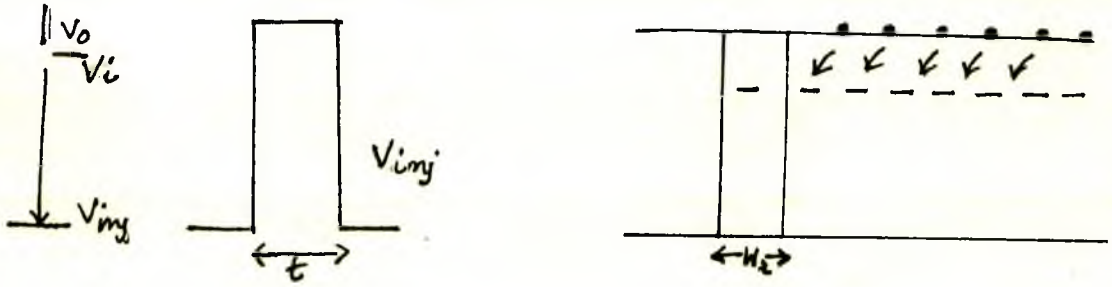


Fig (26b)

Step 3: The pulse is turned off and thus V_R is re-established. But now defect states within depletion region are filled resulting the over all decrease of space-charge density $\left[\sim (N_D+N_T) - N_T\right]$, although V_R is reestablished.

Hence capacitance will be slightly less than the C_R i.e. $C_R > C_{RT}$ (i.e. capacitance when traps are filled)

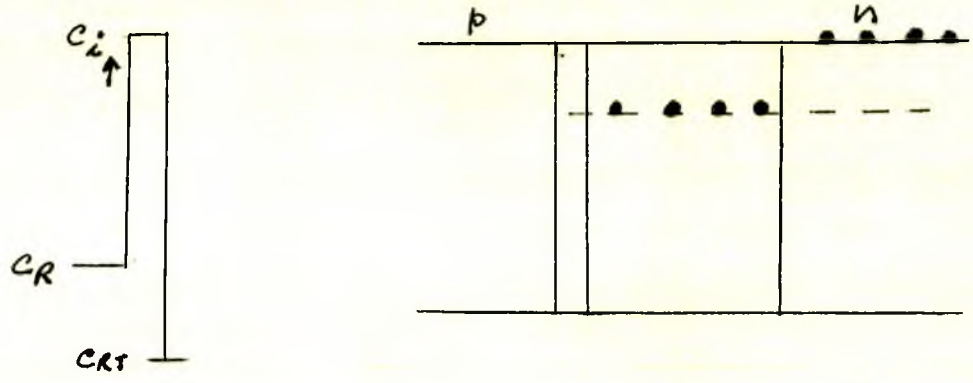


Fig. (26c)

Step 4: But this is an inequilibrium situation. The trapped electrons are then gradually emitted to the conduction band and swept away from the depletion region, thus restoring to the equilibrium condition.

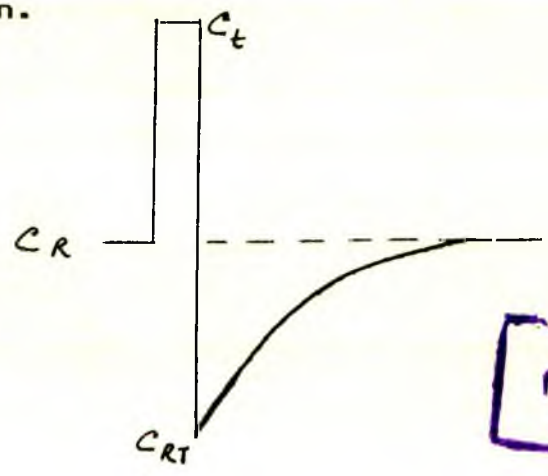
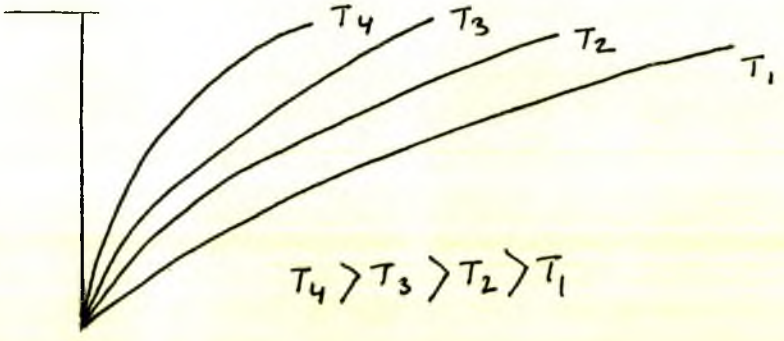


Fig. (26d)

The change in capacitance will appear as transient capacitance change. Emptying of the traps is governed by the Eq.(3.20) i.e.

$$n_T(t) = N_T e^{-e_n t} = N_T \exp(-t / \tau_{en}) \qquad (4.5)$$

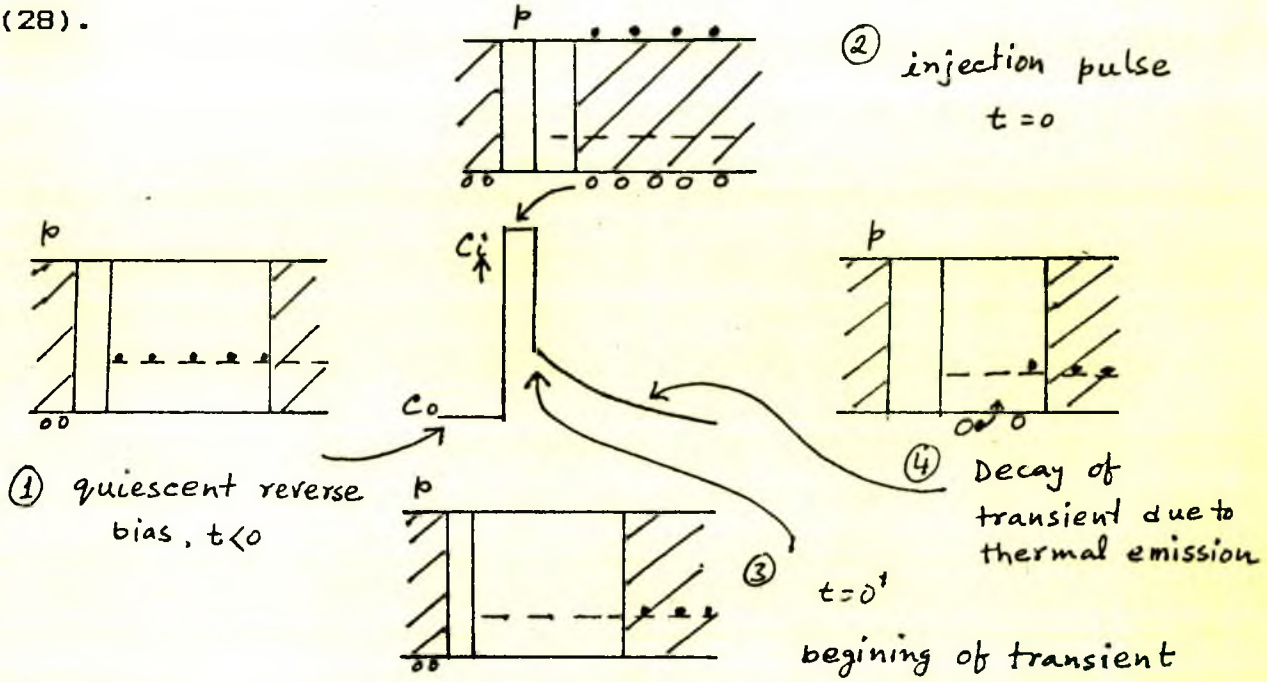
Since e_n increases with temperature, higher the temperature, greater is the emission rate, quicker is the emptying process of traps i.e. quicker is the time constant τ_{en}. The effect of temperature is shown below.



Fig(27): Transient Capacitance at different temperature.

So far we have assumed, the trap level is a donor type. If it is an acceptor type the depletion layer charge density is due to mainly N_D in the transition region (under quiescent reverse bias). In condition (3) the charge density is therefore $(N_D - N_T)$. Therefore once again capacitance under condition (3) when traps are filled will be less than quiescent capacitance C_R ($C_{RT} < C_R$). The traps are now majority carrier traps.

The minority carrier trapping sequences are shown in fig. (28).



Fig(28): Capacitance transient due to a minority carrier trap (in a p^+n junction)

4.4 THERMALLY STIMULATED CAPACITANCE TECHNIQUE:

Thermally stimulated capacitance (TSCAP) is a single shot method. When a system, in equilibrium, is perturbed and then allowed to relax back to original condition, its relaxation exposes properties of the physical systems. When such an experiment is carried out just once or is repeated a few times to improve its accuracy, it can be classed as a single shot measurement. TSCAP is a useful technique for investigating energy levels in p-n junctions. For simplicity, it is described in terms of a single electron trapping level, distance ΔE below the

conduction band edge, in a p^+n junction.

If the junction is reverse biased with a fixed voltage, there results a depletion layer of width W and a corresponding capacitance C. The device is then cooled to a sufficiently low temperature such that thermal emission rate e_n for electrons on the traps is negligible. the bias is then reduced to a substantially lower value for a short period, during which the traps in corresponding region of the depletion layer rapidly fill, with a time constant $\tau_n = 1/c_n = 1/\sigma_n < v_n > n$. Following this the bias is returned to its original value; thereby leaving electrons trapped in the depletion layer. The width of the depletion layer is now somewhat greater than it would have been without the trap-loading process since some of the positive charge of the bound ionized donors is now canceled by the negative charge of the trapped electrons. As a result the junction capacitance has been decreased.

On slowly warming the sample up with a linear ramp of temperature, while continuously monitoring the depletion layer capacitance, a temperature is reached at which the thermal emission rate e_n is no longer negligible. At this time electrons are rapidly promoted thermally to the conduction band whereupon they are immediately swept out of the depletion layer by the electric field, resulting in a corresponding increase in the junction capacitance. This process continues until those traps in the depletion layer that were loaded at the low temperature have

been emptied. The thermal release of the trapped carriers effects a change of the space-charge density in junction transition region and hence a change of the transition region width and junction capacitance.

For simplicity, the situation is described in an asymmetric diode. In the highly asymmetric junction, the depletion region is in low-doped material and consequently one is much more sensitive to traps only on that side of the junction. In more symmetric junctions the main difference is that traps on both sides will give comparable signals.

The process is summarized below:

In an actual experiment following steps are performed:

We describe the method with reference to a p^+n junction having a deep electronic trap level.

(1) The junction is reverse biased with a voltage V called quiescent bias. The shallow levels and the trap levels will be ionized.

(2) The junction is then cooled to a suitable temperature, say $77^{o}k$. The capacitance is lowered slightly because of the temperature effect.

(3) The reverse bias V then suddenly is brought to zero level, that is equivalent to an injection of a positive pulse to bring into majority carriers into the space-charge region. The free carriers, in this case electrons, will be captured by the E_T

levels determined.

(4) The quiescent bias is then restored. Space charge density is now $N_d q$ instead of $(N_d+N_T)q$, resulting increase of depletion width. This will decrease the capacitance.

(5) The temperature now is slowly allowed to raise to room temperature with a constant rate. The occupied traps start emitting free carriers that are immediately swept away by the space-charge field. As a result the depletion zone is modified and we would observe a capacitance step. As the temperature reaches a critical temperature T_m that corresponds to the ionization energy of the deep state maximum numbers of electrons are thermally excited and we get a point of inflexion. So the $\left(\frac{dC}{dt}\right)_m$ gives the ionization temperature T_m and the area under the curve will be proportional to concentration of the deep states.

Let

C_o = Capacitance of the junction when all the trap levels in the depletion region under quiescent bias are empty ($n_T=0$), at low temperature (condition 2); charge being $(N_d+N_T)q$.

C(o) = Capacitance of the junction when traps are completely filled with free carriers (electrons) by collapsing the V=0) (condition 3-4).

C(t) = Capacitance after time t from the time t=0

The hf capacitance of the junction for these conditions may be written as:

$$C_o = A \left[\frac{q\epsilon_s (N_d+N_T)}{2(V_i+V)}\right]^{1}/2 \qquad (4.6a)$$

$$C(o) = A \left[\frac{q\epsilon_s \left[N_d+(N_T-n_T(0)\right]}{2(V_i+V)}\right]^{1}/2$$

$$= A \left[\frac{q\epsilon_s N_d}{2(V_i+V_B}\right]^{1}/2 \qquad (4.6b)$$

and $$C(t) = A \left[\frac{q\epsilon_s \left[N_d+(N_T-n_T(t)\right]}{2(V_i+V)}\right]^{1}/2 \qquad (4.6c)$$

$n_T(o) = N_T$, when all traps are filled at t = 0

$n_T(t)$ = no of traps filled with carriers at time t.

Since filled traps will start emptying, at any time $tn_T(t) < n_T(0)$ and hence $C_o > C(t) > C(o)$. From Eqs.(4.6) we have:

$$\frac{C^2(t)-C^2(o)}{C^2(o)} = \frac{(N_T-n_T(t)}{N_d} \qquad (4.7)$$

and $$\frac{C_o^2 - C^2(o)}{C^2(o)} = \frac{N_T}{N_d} \qquad (4.8)$$

Combining the two equations we get,

$$\frac{C^2(t)-C^2(o)}{C^2(o)} = \frac{C_o^2 - C^2(o)}{C^2(o)} \times \frac{\left[N_T - n_T(t)\right]}{N_d} \qquad (4.9)$$

Since N_T = Trap level concentration, then

$N_T - n_T(t)$ = no of empty traps at time 't'

The rate equation then can be written as;

$$\frac{dn_T(t)}{dt} = (N_T - n_T)\, e_p - n_T e_n \qquad (4.10)$$

where e_p and e_n are hole and electron emission rate respectively and we neglected the capture of electrons or holes .

For initial condition i.e. t=0, we assume all the traps in the depletion region are filled with electrons,

$n_T(o) = N_T$, then solution of Eq.(4.10) is

$$n_T(t) = \frac{e_p}{e_n + e_p} N_T + \left[\frac{e_n}{e_n + e_p}\right] N_T\, e^{-(e_n + e_p)t} \qquad (4.11)$$

If we assume $e_n >> e_p$ for traps filled with electrons, then

$$n_T(t) \simeq N_T\, e^{-(e_n)t} \qquad (4.12)$$

Thus the trapped electrons emptied themselves exponentially with the characteristic time that is inverse of the emission rate of the trap.

$$\tau_n = \frac{1}{e_n}$$

Using Eq.(4.12), in Eq.(4.9) we get

$$\frac{C^2(t) - C^2(o)}{C_o^2(o)} = \frac{C_o^2 - C^2(o)}{C^2(o)} \left[1 - e^{-e_n t}\right] \qquad (4.13)$$

or $$\Delta C^2(t) = \Delta C_m^2 \left[1-e^{-e_n t}\right] \qquad (4.14)$$

where $$\Delta C^2(t) = C^2(t) - C^2(o) \qquad (4.15a)$$

$$\Delta C_m^2 = C_o^2 - C^2(o) \qquad (4.15b)$$

Thus we see that ΔC^2 reaches the maximum value ΔC_m^2 exponentially with characteristic time $\frac{1}{e_n}$, where e_n is given by the Eqn. (3.12) $C^2(t)$ value reaches its maximum value C_o^2 as $t \longrightarrow \infty$ i.e. when all the filled traps $n_T(o)$ $(=N_T) \longrightarrow 0$. Again from Eq. (4.6a,b,c), we may write,

$$\frac{C_o^2 - C^2(t)}{C_o^2} = \frac{n_T(t)}{N_d+N_T} = \frac{N_T\, e^{-e_n t}}{N_d+N_T} \qquad (4.16)$$

Here $C_o^2 - C^2(t)$ = difference between square of depletion capacitance without filling the traps and at any other time after the traps are filled at t = 0.

Initially i.e. as we start emptying the traps i.e. t=0, Eq (4.16) has the form.

$$\frac{C_o^2 - C^2(o)}{C_o^2} = \frac{n_T(o)}{N_d+N_T} = \left[\frac{N_T}{N_d+N_T}\right] \qquad (4.17a)$$

or $$N_T = \frac{C_o^2 - C^2(o)}{C^2(o)}\, N_d \qquad (4.17b)$$

Thus using formula (4.17), we can estimate the trap concentration N_T if the shallow donor concentration N_d is known or N_T/N_d ratio may be obtained. Combining Eq. (4.17a) with (4.16), we fined

$$\frac{C_o^2 - C^2(t)}{C_o^2} = \frac{C_o^2 - C^2(o)}{C_o^2} e^{-e_n t}$$

or $$C_o^2 - C^2(t) = \left[C_o^2 - C^2(o)\right] e^{-e_n t}$$

or $$\partial C^2(t) = \partial C^2(o)\, e^{-e_n t} \qquad (4.18a)$$

$$\partial C^2(t) = C_o^2 - C^2(t); \quad \partial C^2(o) = C_o^2 - C^2(o) \qquad (4.18b)$$

However for a first order approximation, from Eq.(4.6-4.8) we get

$$C_o - C(o) = A\left[\frac{q\epsilon_s (N_d+N_T)}{2V_B}\right]^{1/2} - A\left[\frac{q\epsilon_s N_d}{2V_B}\right]^{1/2} = \frac{1}{2}\frac{N_T}{N_d} C(o) \qquad (4.19)$$

$$\frac{C_o - C(o)}{C(o)} = \frac{1}{2}\frac{N_T}{N_d}$$

$$N_T = 2N_d \times \frac{C_o - C(o)}{C(o)} = \frac{(\Delta C)_o}{C(o)} 2N_d \qquad (4.19a)$$

or, we may write,

$$\frac{C_o - C(o)}{C_o} = \frac{1}{2}\frac{N_T}{(N_d+N_T)} \qquad (4.20)$$

Eq.(4.19) or (4.19a) may be used for approximate estimate of N_T

$(\Delta C)_o$ = difference of capacitance between the empty traps and initially completely filled traps.

$C(o)$ = Capacitance of the junction when traps are filled

C_o = Capacitance of the junction when traps are empty.

Starting from Eqs.(4.6) and using Eq.(4.20), for first approximation and proceed as before, we arrived at the following Eq.

$$\frac{C_o - C(t)}{C(o)} = \frac{C_o - C(o)}{C(o)} e^{-e_n t}$$

or $$C_o - C(t) = \left[C_o - C(o)\right] e^{-e_n t}$$

$$\partial C(t) = \partial C(o) e^{-e_n t} \qquad (4.21)$$

4.4.1 Estimation of Ionization Energy:

Either from Eq.(4.14) or Eq. (4.18a) we immediately obtain

$$e^{-e_n t} = \frac{C_o^2 - C^2(t)}{C_o^2 - C^2(o)} = \frac{\partial C^2(t)}{\partial C^2(o)}$$

$$-e_n t = \ln \left[\frac{\partial C^2(t)}{\partial C^2(o)}\right] \qquad (4.22)$$

If the sample is now warmed up with uniform rate β, from a starting temperature T_o (usually 77^ok), then

$$T = T_o + \beta t$$

where 't' is time after which observation is made as counted from T_o. Then Eq.(4.22) is written interms of temperature T, T_o and β

i.e.

$$e_n = -\frac{\beta}{(T-T_o)} \ln \frac{\partial C^2(t)}{\partial C^2(o)} = -\frac{\beta}{(T-T_o)} \ln \frac{C_o^2 - C^2(t)}{C_o^2 - C^2(o)}$$

$$= \left(\frac{\beta}{(T-T_o)}\right) \ln \frac{C_o^2 - C^2(o)}{C_o^2 - C^2(t)} \qquad (4.23)$$

Thus using Eq. (4.23) and observing C_o, C(o), C(t) we can estimate e_n for different time t i.e. at different temperature T. Since e_n is related to ionization energy ΔE $\left[= (E_c - E_T)\right]$, with E_c and E_T being the conduction band and defect state energies respectively, with temperature by (Eq.3.12)

$$e_n = A_n e^{-\Delta E_i / kT}$$

or $$\ln e_n = \ln A_n - \frac{\Delta E_i}{kT} \qquad (4.24)$$

$$= \ln A_n - \frac{V_i}{T} \times 11600 \qquad (4.24a)$$

From the slope of the curve we can estimate ΔE_i or V_i where V_i is the ionization potential corresponding to ΔE_i.

4.4.2 Approximation Method:

We can estimate the ionization energy of the defect state by using Eq. (4.21); from Eq. (4.21) we have

$$\left(C_o - C(t)\right) = \left(C_o - C(o)\right) e^{-e_n t}$$

i.e. $$-e_n t = \ln\left[\frac{C_o - C(o)}{C_o - C(t)}\right]$$

As before if the sample is scanned through temperature uniformly i.e.

$$T = T_o + \beta t$$

$$e_n = -\left(\frac{\beta}{(T-T_o)}\right) \ln \left[\frac{C_o - C(t)}{C_o - C(o)}\right]$$

$$= \frac{\beta}{(T-T_o)} \ln \left[\frac{C_o - C(o)}{C_o - C(t)}\right] \qquad (4.25)$$

Thus observing C_o, $C(t)$ at different temperature we obtain e_n for various temperature. Then plotting $\ln e_n$ against $1/T$ we can estimate the ionization energy ΔE of a deep state [Eq. (4.24).]

4.5 THERMALLY STIMULATED CURRENT STUDY (TSC)

At low temperature, deep impurity states may be studied, particularly in a high resistance semiconductor by the method of thermally stimulated current (TSC). This method first was employed in a bulk semiconductor, but later on has been extended to device study also.

In the case of a bulk material the usual technique followed is describe below. The bulk sample is mounted in vacuum cryostat and cooled. It is then excited by optical illumination to place the traps in non-equilibrium state. Excitation may be done also by electrical method such as employing current or voltage transient. The temperature must be very low so that equilibrium is re-established very slowly so that measurement is possible. The sample is then heated at a linear rate and the variation of conductivity (or the emitted light glow), resulting from return to

equilibrium, is monitored against the rise of temperature. Comparison of this experiment with one done without the initial excitation-illumination shows the presence of current (or glow) peaks associated with the emptying of traps within the semiconductor. Study of TSG (Thermally stimulated Glow) was first made on NaCl excited with X-rays. Analysis of thermally stimulated phenomenon may be approached by (i) quasi-equilibrium treatment (ii) fast and slow trapping technique. The quasi-equilibrium is based on a few assumptions like[16]:

(a) Recombination in the material involves retrapping of the emitted carrier by the level under consideration.

(b) the level is initially completely empty

(c) equilibrium is assumed between the conduction band and the trap, so that a Fermi level can be defined throughout the temperature rise.

(d) The peak current occurs when the Fermi-level crosses the trap level.

If the above assumptions are true or near true, the energy level of the trap may be obtained from the relation

$$\Delta E_T = kT_m \ln \left[\frac{N_c(T_m)}{n_T(T_m)} \right] \qquad (4.26)$$

ΔE_T = level of the trap below the conduction band edge of the trap state.

T_m = Temperature at which conductivity or current peak occurs.

N_c = density of states in the conduction band at T_m.

$n_T(T_m)$ = electrons concentration of the traps at T_m.

However assumption (b) is difficult to be fulfilled and it is not possible to be sure absolutely if a trap level is completely empty or not. This then affects n_T. Assuming no retrapping and with n_T computed from a temperature independent capture cross-section of 10^{-14} cm^2 for the traps of a typical semiconductor, Eq.(4.26) reduces to

$$\Delta E_T = 23k\ T_m \qquad (4.27)$$

Thus a thermally stimulated current peak occurring at 100^oK represents a trap-level of about 0.2 eV. Usually T_m is found to be increased with increase of heating rate (β), and this is an important way of determining trap depth. It must be emphasized however, that Eq.(4.27) is used only for very crude estimates of trap depths. The method of TSC as applied in bulk materials has been reviewed by many authors[19,29].

The more fundamental approach to the thermally stimulated current problem was made by Randall and Wilkines[24] and later, further developed by Saunders[25] and Jewitt and their treatment is based on the two equations:

$$\frac{dn_i(t)}{dt} = -n_i N_c \sigma_i v_{th} \exp\left(-\frac{\Delta E_i}{kT}\right) + n_c(N_i - n_i)\ \sigma_i v_{th} \qquad (4.28a)$$

$$\frac{dn_c}{dt} = -\frac{n_c}{\tau} - \sum_i \frac{dn_i}{dt} \qquad (4.28b)$$

N_i = density of the i-th impurity level

n_i = density of electrons in the i-th impurity level

n_c = density of electrons in the conduction band

v_{th} = thermal velocity of electron

σ_i = capture cross-section of the i-th level

τ = recombination time of electrons

In Eq.(4.28a), the left hand side gives the net rate of change of electrons in the i-th level. On the right hand side, first term gives the thermal release of the n_i trapped electrons. $N_c \simeq 2(2\pi m^* kT/h^3)^{3/2}$ and this $\left(N_c \sigma_i v_{th}\right)$ is the attempt-to-escape frequency A, and the exponential gives the probability of escape. In fact the entire term represents the emission rate e_n of n_i electrons. The 2nd term on the right hand side represents the retrapping of the conduction band electrons, n_c by the unoccupied traps $(N_i - n_i)$ which have a capture cross-section of σ_i. In fact $n\sigma_i v_{th}$ gives the capture rate C_n. Eq.(4.28b) involves the recombination of conduction electrons. The first term on the right side assumes that free electrons interact with a recombination center which is described by an effective life time τ. The second term is re-capture by the traps. If more than one trap is present, it is assumed that they are of significantly different energy so that they do not interact.

On the basis of first trapping analysis, i.e. only one

impurity level acts at a given time and the recombination time τ is long compared with the retrapping action,and assuming that peak current occurs at a temperature T_m when n is maximum, Eq.(4.28b) reduces to

$$\frac{dn}{dt} = -\frac{dn_i}{dt} \qquad (4.29)$$

(for single level & $\tau \longrightarrow$ very large)

and peak occurs at (T_m), $\frac{dn}{dt} = 0$ i.e. from (4.29) it implies

$$\frac{dn}{dt} = 0 \text{ for } T = T_m.$$

Then Eq. (4.28a) yields

$$\Delta E_i = kT_m \ln \left[\frac{N_c}{n_c} \times \frac{\eta}{\eta-1}\right]$$

where $\eta = \left[\frac{n_i}{N_i}\right]$. It is noted if $\eta = {}^1/_2$ we get Eq.4.26.

If we let

$$n_c = N_c \exp\left[-\frac{E_c - E_F}{kT}\right]$$

as is the case in thermal equilibrium, we can solve for $E_c - E_F$ as follows:

$$E_c - E_F = E_c - E_T - kT_m \ln \left[\frac{\eta}{1-\eta}\right] \qquad (4.30)$$

More rigorous and general analysis was offered by Saunders and Jewitt. Their basic assumptions are : (i) contribution of electrons from all but one trap may be neglected, (ii) the occupancy of all of the other traps remain sufficiently constant. Thus retrapping by these levels may be accounted for in the term

involving τ and be temperature independent.

Under these condition, the summation term in Eq.(4.28b) is dropped. Further, if it is assumed that

$$n_c \ll n_i$$

and $$n_i \ll N_i \tag{4.31}$$

Eqs.(4.28a and 4.28b) can be solved and the conductivity as defined by Eq.(4.32)

$$\sigma(T) = q\mu_n n \tag{4.32}$$

may be evaluated as

$$\sigma(t) = \frac{q\tau\mu_c N_c \sigma_i v_{th}}{1 + \tau N_c \sigma_i v_{th}} \hat{n}_i \exp\left[- \frac{\Delta E_i}{kT} - \frac{1}{\beta} \int_{T_o}^{T} \frac{N_c \sigma_i v_{th} \exp\left(-\frac{\Delta E_c}{kT}\right) dT}{1 + \tau N_i \sigma_i v_{th}} \right] \tag{4.33}$$

β is the rate at which temperature is being raised, such that

$$T = T_o + \beta t \tag{4.34}$$

$\hat{n}_i$ = initial occupancy of carriers (electrons) of the i-th impurity level (at t=0 and $T = T_o$).

Usually $N_c \propto T^{3/2}$, $v_{th} \propto T^{1/2}$, $\sigma_i \propto T^{-b}$, and τ = constant.

Then it has been shown that $\sigma(T)$ results maximum at $T = T_m$ such that,

$$\frac{\Delta E_i}{kT_m} = \ln\left(\frac{T_m^2}{\beta}\right) + \ln\left[\frac{N_c \sigma_i v_{th} k}{\Delta E_i}\right] - \ln\left[1 + \tau N_i \sigma_i v_{th}\right] \tag{4.35}$$

provided $\Delta E_i > kT_m$.

Case 1. If the process involved is such that retrapping is very slow, then

$\tau N_i \sigma_i v_{th} << 1$, and Eq.(4.35) assumes the form

$$\frac{\Delta E_i}{kT_m} = \ln\left(\frac{T_m^2}{\beta}\right) + \ln\left(\frac{N_c \sigma_i v_{th} k}{\Delta E_i}\right) \qquad (4.36)$$

Usually $\sigma_i \propto T^{-2}$, and $N_c \propto T^{3/2}$ and $v_{th} \propto T^{1/2}$, thus the second term in Eq.(4.36) is almost independent of temperature. Then a plot $\frac{1}{T_m}$ vs $\ln\left(\frac{T_m^2}{\beta}\right)$ for various heating rates should give a straight line with the slope $\frac{\Delta E_i}{k}$ and the intercept yields the capture cross-section. If however b ≠ 2, then Eq.(4.36) can be written in the form:

$$\frac{\Delta E_i}{kT_m} = \ln\left(\frac{T_m^{4-b}}{\beta}\right) + C \qquad (4.37)$$

Where C is independent of temperature. The value of 'b' must then be found by trial and error so that a straight line is obtained to determine ΔE_i and σ_i as above.

Case 2.

Fast trapping: Under this process, we may take $\tau N_i v_{th} \sigma_i >> 1$. Eq.(4.35) stands out

$$\frac{\Delta E_i}{kT_m} = \ln\left(\frac{T_m^{9.5}}{\beta}\right) + C' \qquad (4.38)$$

$$\text{where } C' = \ln\left(\frac{N_c}{\tau N_i}\right) - \frac{3}{2}\ln(T_m) - \ln\left(\frac{\Delta E_i}{k}\right) \qquad (4.39)$$

and is independent of temperature.

In this case it is not possible to estimate σ_i, but τN_i may be estimated.

The peak of TSC current may be determined by finding the maxima of Eq.(4.33) i.e. by setting $\frac{\partial \sigma}{\partial T}\Big|_{T=T_m} = 0$, we obtain as follows:

$$\exp\left(-\frac{\Delta E_i}{T_m}\right) = \left(\frac{1+N_c \sigma_i v_{th} \tau}{N_c \sigma_i v_{th} k T_m^2}\right)^{\Delta E_i \beta} \tag{4.40}$$

The above equation may be evaluated for various values of β under two limiting conditions (i) slow trapping, when $\tau N_c \sigma_i v_{th} << 1$ and (ii) fast retrapping i.e. when $\tau N_c \sigma_i v_{th} >> 1$. Under these limiting conditions Eq.(4.40) reduces to particularly convenient expression, since in the first case variations of $N_i \tau$ are not important, and in the second σ_i drops out,

There are various technique and approximation method of evaluating ΔE_i from the observed TSC peaks depending on the experimental condition and constrains. However most people start with Eqs.(4.28a,4.28b) and make other simplifying assumption to obtain an expression for ΔE_i as a function of T_m. We may use a simplified form assuming slow retrapping and expanding the integral in a series as have been used by many[2σ-2ρ], then we get

$$\Delta E_i = \left(\frac{1.51\ k T_m T_{1/2}}{T_m - T_{1/2}}\right) \tag{4.41}$$

where $T_{1/2}$ = Temperature at which half-maximum occurs on the

rising portion of the curve, where we have assumed $\sigma_i \propto T^{-2}$.

A number of other experimental techniques have been carried out by many authors to obtain TSC curves. These involve space-charge limited currents, capacitor and diode structures, polarization charge relaxation and ac field methods[30]. As for example, Devaux and Schott[91] obtained expressions for space charge limited peaks and trap exhaustion current peaks. In the former case,

$$\frac{\Delta E_i}{kT_m} = \ln \left[\frac{(2\alpha e\mu)\nu k T_m^2}{\beta \Delta E_i \left[1+\frac{2kT_m}{\Delta E_i} \right]} \right] \qquad (4.42)$$

where α = a constant related to dielectric constant

ν = thermal escape frequency,

whereas for the later case, we may write

$$\frac{\Delta E_i}{kT_m} = \ln \frac{A k T_m^2}{\beta(\Delta E_i)} \qquad (4.43)$$

where A is a constant proportional to the constant field in the device.

4.5.1 TSC IN JUNCTION DEPLETION REGION:

So far we have described the method of TSC as applied to bulk material. We noted that TSC measurements are difficult to make in a semiconductor that is only moderately high in resistance ($<10^5 \Omega$-cm) as then dark current becomes too large.

The difficulty may be, at least partially, overcome if we use a junction device made out of the semiconductor. If the junction is reverse biased, the dark current is considerably reduced and emission from traps in the depletion region can be studied. Many authors have made such measurements on p-n junction devices. There are two methods:in one technique, measurement is made at constant temperature with a step of applied voltage causing the transient condition[32]. In the second technique, the bias is held constant and temperature increased to provide the thermal stimulation current[33,34]. This technique is virtually indentical to TSCAP except that the device is connected to a suitable electrometer amplifier instead of a capacitance bridge.

Traps are filled by excitation at low temperature and then emptied by raising the temperature at a constant rate β. On reaching the temperature at a significant rate there results a temporary increase in current. A curve of thermally stimulated current for a single trap depth has the form of a somewhat asymmetric curve with a fairly sharp maximum at a temperature which is determined by the trap depth, the capture cross-section of the trap and the heating rate(Fig.29). By making measurements

at two or more heating rates, independent values of the trap depth and the capture cross section can be obtained. If more than one type of trap is present, curves obtained by thermal stimulation may be expected to show several maxima. Again let us consider an abrupt p^+n junction with an deep impurity state of concentration N_T and for simplicity of analysis, we assume that the level is an acceptor type. An acceptor is characterized as one which accepts an electrons when majority carriers are brought in by reducing the reverse bias at low temperature. When the impurities accept electrons they become negatively charged, whereas at higher temperature i.e when the traps are empty the states are electrically neutral. In the analysis followed, we must keep those facts in mind.

As mentioned before, in any junction measurement, the device is cooled to a low temperature where defect centers are filled in with majority carriers by applying a suitable bias, usually zero, which reduces the depletion width to W_i (intrinsic value). Then the

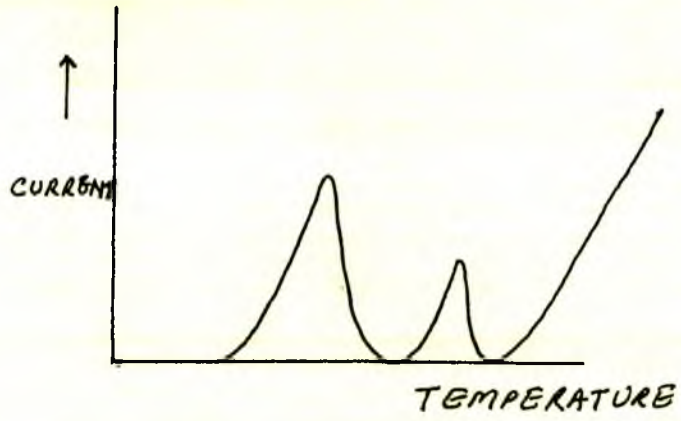


Fig.(29) TSC curve

reverse bias is restored to the original value, the depletion width increases to W

Let n_t = electron density at the defect centers i.e. no of electrons trapped by the center.

n_t^* = electron density at the defect center in the initially uncharged depletion region .

The thermally stimulated current is measured as the junction is heated. This heating effect generates current, due to the emission of electrons and holes from the acceptor defects in the depletion region. The TSC has two components, the conduction current associated with generation of carriers and the displacement current. The later current is due to the fact that junction may be treated as parallel-plate condensor and hence a displacement current as introduced by Maxwell must exists.

The electric field that exists across the junction is given by

$$E_o = -q\epsilon_s\left[\left(N_d - n_t\right)\left(W - W_i\right) + \left(N_d - n_t^*\right)W_i\right] \qquad (4.44)$$

and the total junction voltage including the applied voltage,

$$V_B = (-q/2\epsilon_s)\left[\left(N_d - n_t\right)\left(W^2 - W_i^2\right) + \left(N_d - n_t^*\right)W_i^2\right] \qquad (4.45)$$

As potential V_B is kept constant throughout the experiment, $\frac{\partial V_B}{\partial t} = 0$,

Differentiating Eq(4.45) and putting $\frac{\partial V_a}{\partial t} = 0$, we obtain an expression for $\frac{\partial W}{\partial t}$ needed for the evaluation of $\frac{\partial E_o}{\partial t}$ from Eq.(4.44):

$$\frac{\partial W}{\partial t} = \dot{W} = \left[\bar{n_t}\left(W^2 - W_i^2\right) + n_t^* W_i^2\right] \Big/ \left[2W\left(N_d - n_t\right)\right] \qquad (4.46)$$

The Maxwell displacement current for a parallel-plate capacitor system is given by

$$I_{dc} = A\epsilon_s \frac{\partial E_o}{\partial t} = A\epsilon_s \dot{E}_o \qquad (4.47)$$

Using Eq.(4.44) and then (4.46), we get from (4.47)

$$I_{dc} = \frac{qA}{2W}\left[\bar{n_t}\left(W - W_i\right)^2 + \bar{n_t^*}\left(2WW_i - W_i^2\right)\right] \qquad (4.48)$$

The conduction current due to the emission of holes from the trap center may be computed as

$$I_{co} = -qA \int_o^W \bar{p_t} dx \qquad (4.49)$$

where p_t = hole density at the defect centers

and p_t^* = hole density at the defect center in the initially uncharged depletion region.

or $$I_{co} = -qA\left[e_p\, p_t^*\, W_i + e_p\, p_t\left(W - W_i\right)\right] \qquad (4.50)$$

The total thermally stimulated current is therefore,

$$I_j = I_{dc} + I_{co} = -\left(\frac{qA}{2W}\right)\left[-\dot{n}_t\left(W-W_i\right)^2 - \dot{n}_t^*\left(2WW_i - W_i^2\right) + e_p p_t^* 2WW_i + e_p p_t 2W\left(W - W_i\right)\right] \tag{4.51}$$

In deriving the above equation use has been made of Eq.(4.45) from which we can express W in the following form.

$$W^2 = \left[W_o^2 \,/\, (1-n_t/N_d)\right] \Big/ \left[1-\left(W_i^2 \,/\, W_o^2\right)\left(n_t - n_t^* \,/\, N_d\right)\right] \tag{4.52}$$

with $$W_o = -\left[\frac{V_i 2\epsilon_s}{qN_d}\right]^{1/2} \tag{4.53}$$

W_o denotes the depletion width if there were no defect states and $W \simeq W_o$ if defect states are very small compared to N_d i.e $N_t << N_d$.

During discharging phase, i.e. holes being emitted from the traps, the parameters which influence the TSC response, are N_d/N_T ratio, β (the heating rate) and the g_i factor which indicates the charged fraction of the depletion region.

The effect of N_d/N_t ratio on TSC curve has been studied and it is found as the ratio increases the resolution of the current peak against the dark current gets poorer. For simplicity if we put $W_i \simeq o$, which implies that all the defects in the depletion region are charged.

We then get for TSC

$$I_J = -\left(q\epsilon_s A W_o N_t\right)\left[\left(e_n n_t + e_p p_t\right) / 2N_t\right] \Big/ \left(1-n_t/N_d\right)^{1/2} \qquad (4.54)$$

The effect of heating rate β on TSC has also been studied and it is found that for $N_d >> N_t$ and for $W_t \simeq 0$, the current peak shifts towards high temperature side as the β-value is increased.

Under these conditions the TSC expression becomes

$$I_j = -qAW_o N_t \left(e_n n_t + e_p p_t\right) / 2N_t \qquad (4.55)$$

4.5.2 Steady state phase

As the centers emit the excess electrons, we reach the steady state condition i.e. $n_t = n_t^* = n_{tf} = \frac{e_p}{(e_n + e_p)} N_t$ and $\bar{n_t} = 0$ and $n_t e_n = e_p p_t$. For this condition the steady state current is offered,

$$I_J = -qAW_o N_t \left[\left(e_p p_{tf} / N_t\right)\right] \Big/ \left(1-n_{tf}/N_d\right)^{1/2} \qquad (4.56)$$

Although above equations are derived for p^+n with acceptor impurity level, the relation may be applicable to the case with p^+n junction and the presence of donor defect states.

However for n^+p junction with either a donor or an acceptor defect the TSC is given by

$$I_J = (n^+p) = (qA/2W)\left[-\bar{p}_t\left(W-W_t\right)^2 - \bar{p}_t^*\left(2WW_t - W_t^2\right)\right.$$
$$\left. +e_n n_t^* 2W W_t + e_n n_t 2W\left(W - W_t\right)\right. \qquad (4.57)$$

4.5.3 DEFECT STATES WITH SINGLE PROCESS:

For generality's sake in the above consideration is capable of emitting electrons as well as holes. The relation derived above may however be applied to defects where only one type of charge carriers are emitted, for example $e_n >> e_p$. In this case the appropriate current equation can be written immediately by putting $e_p = o$ and $n_t^* = 0$; Eq. (4.51) the becomes:

$$I_j = -\frac{qA}{2W}\left[-\bar{n}_t\left(W-W_t\right)\right]$$

and if $W_t = 0$, i.e. all defects in the depletion region we charged.

$$I_j = \frac{qA}{2W}\left[\bar{n}_t W^2\right]$$
$$= \frac{qA}{2}\left(\bar{n}_t W\right) = \frac{qA\, e_n n_t}{2(1-n_t/N_d)}\, W_o \qquad (4.58)$$

Now if further we take n_d

$$I_j = \frac{qA\, e_n n_t}{2}\, W_o \qquad (4.59)$$

Thus we see that TSC is proportional to $(e_n n_t)$. The condition for which the current will reach maximum may be obtained by setting the condition

$$\frac{d(e_n n_t)}{dt} = 0 \tag{4.60}$$

i.e. $$n_t \bar{e}_n + \bar{n}_t e_n = 0 \tag{4.61}$$

Using Eq.

$$\frac{dn}{dt} = e_p p_t - e_n n_t \tag{4.62}$$

or for $e_p = 0$

$$\bar{n}_t = -e_n n_t$$

Using above equation in (4.61), we get the condition for maximum,

$$\bar{e}_n = e_n^2 \tag{4.63}$$

We know the emission rate e_n has temperature dependence

$$e_n = B_n T^2 e^{-\Delta E_t / kT} \tag{4.64}$$

Using (4.64) in (4.63) we get the temperature T_m at which the TSC current peak will occur i.e.

$$\frac{\Delta E_t}{kT_m} = \ln\left[\frac{BkT_m^4}{\beta(\Delta E_t + 2kT_m)}\right] \tag{4.65}$$

where $\beta = \frac{dT}{dt}$ (rate of increase of temperature)

If however we use simpler relation for emission rate i.e.

$$e_n = A\, e^{-\Delta E_i / kT} \qquad (4.66)$$

then Eq.(4.65) becomes

$$\frac{\Delta E_i}{kT_m} = \ln\left[\frac{AkT_m^2}{\beta(\Delta E_i + 2kT_m)}\right] \qquad (4.67)$$

As before A represents the frequency factor. Eq(4.67) can be solved for ΔE_i using Newton-Raphson approximate method[35].

In many experimental situations the above equation may further be simplifieded to:

$$\frac{\Delta E_i}{kT_m} = \ln\left[\frac{AkT_m^2}{\beta \Delta E_i}\right] \qquad (4.68)$$

and

$$\frac{\Delta E_i}{kT_m} = \ln\left[\frac{BkT_m^4}{\beta \Delta E_i}\right] \qquad (4.69)$$

(follows from 4.65)

For CdS diode structure, the space-charge current has been studied under reverse bias during heating process, by Driver and Wright[36] and obtain an expression for current as

$$\bar{I} = \frac{qAW}{2} N_T A \exp\left[-\frac{E_T}{kT} - \frac{kT_m^2}{\beta E_T} A \exp\left(-\frac{E_T}{kT}\right)\right] \qquad (4.70)$$

4.5.4 Capacitance Response curve:

If we look back to capacitance response curves equation (4.27 or 4.36) or their approximate forms (Eq 4.41), we may proceed in the same manner to get the condition of maximum slope of the capacitance step curves. This may be obtained by setting 2nd time derivatives of those equations to zero. We get for maximum slope at temperature T_m given by the identical equation as Eq.(4.65-4.69). Thus we note the capacitance maximum slope shifts towards the high temperature side as TSC peak with higher heating rate β,

let us consider Eq.(4.68) for simplicity, which can be written in the form

$$\ln\left(\frac{T_m^2}{\beta}\right) = \left(\frac{\Delta E_i}{k}\right)\frac{1}{T_m} + \ln\left(\frac{\Delta E_i}{kA}\right) \qquad (4.71)$$

Thus observing shift of capacitance slope maxima or TSC peak for different heating rate β, and then plotting $\ln\left(T_m^2/\beta\right)$ against $\frac{1}{T_m}$ we can estimate ΔE_i from the slope and A from the intercept.

CHAPTER FIVE

EXPERIMENTALS

5.1 DESIGN AND CONSTRUCTION:

5.1.1 Electronics circuitry:

(i) A d.c. power supply unit: A multipurpose power supply unit capable of supplying voltage 0 - 5, 0 - ±12, 0 - ±15 V dc. was constructed using conventional circuit and common IC'S. The power supply unit supplies power to the low voltage equipment and various transistors and IC's used in various electronic circuits built for our experiment. The electronic circuits of the supply unit uses Si-bridge rectifiers and IC-voltage regulators.

(ii) A dc amplifier: In order to monitor temperature of the sample from 77°K to 300°K, a Cu-constantan thermocouple is used. This thermo-emf is used to drive the x-axis of a x-y recorder. In order to increase the driving range, the thermo-emf which is in the order of a few millivolts, needs to be amplified. For this purpose a d.c. amplifier was constructed using simple operational amplifier (741) in inverting mode. The output of the amplifier is being controlled by a potentiometer such that output is approximately given by $e_o = - XR_2/R_1(V_i)$, where XR_2 is the fraction of the output potentiometer resistance and R_1 is the input resistance (Fig. 30).

(iii) A "differential amplifier": As discussed earlier the main object of a TSCAP experiment is to record capacitance change

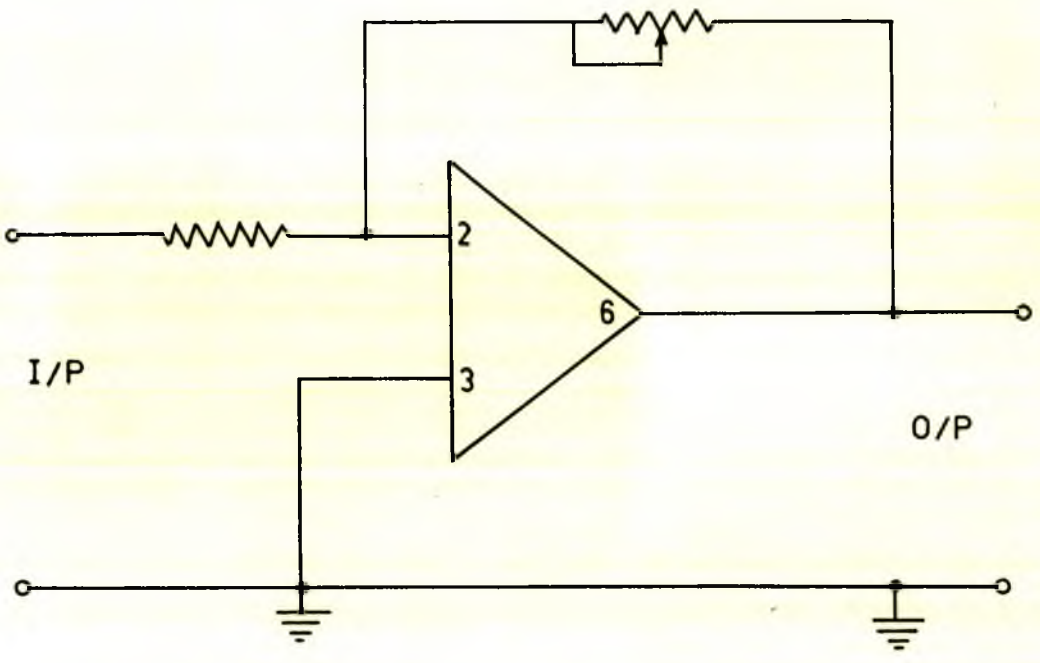


Fig.30 Amplifier circuit

of the depletion region of a p-n junction during the emission of carriers by the trap centres. This change is however very small and is usually masked in the noise and monotonic rise of the capacitance due to simple temperature effect.

This possesses a problem in earlier study of TSCAP, particularly when trap concentration E_T is low. This difficulty has been overcome in our 'set up' by the use of a differential amplifier constructed for our experimental need. The function of a deferential amplifier is, in general, to amplify the difference between two signals (e_1 & e_2) - put into as inputs in an op-amp. In an ideal differential amplifier the output e_o is given by $e_o = Ad(e_1 - e_2)$, Ad is called gain of the differential amplifier. But a practical differential amplifier can not be fully described by the equation because in general, the output (e_o) depends not only upon the difference signal vd (= $e_1 - e_2$) of the two signals, but also upon average level, called the common mode signal v_c defined as $v_c = 1/2(e_1 + e_2)$. A quantity called the 'common mode rejection ratio' (CMMR), which is a measure of figure of merit of a differential amplifier, is defined by

$$CMMR = c = A_d/A_c$$

where $A_c = A_1 + A_2$ (A_1 = voltage amplification from input-1 when input-2 is grounded; A_2 = voltage amplification from input-2, when input-1 is grounded) and $A_d = 1/2(A_1 - A_2)$. Then for a practical

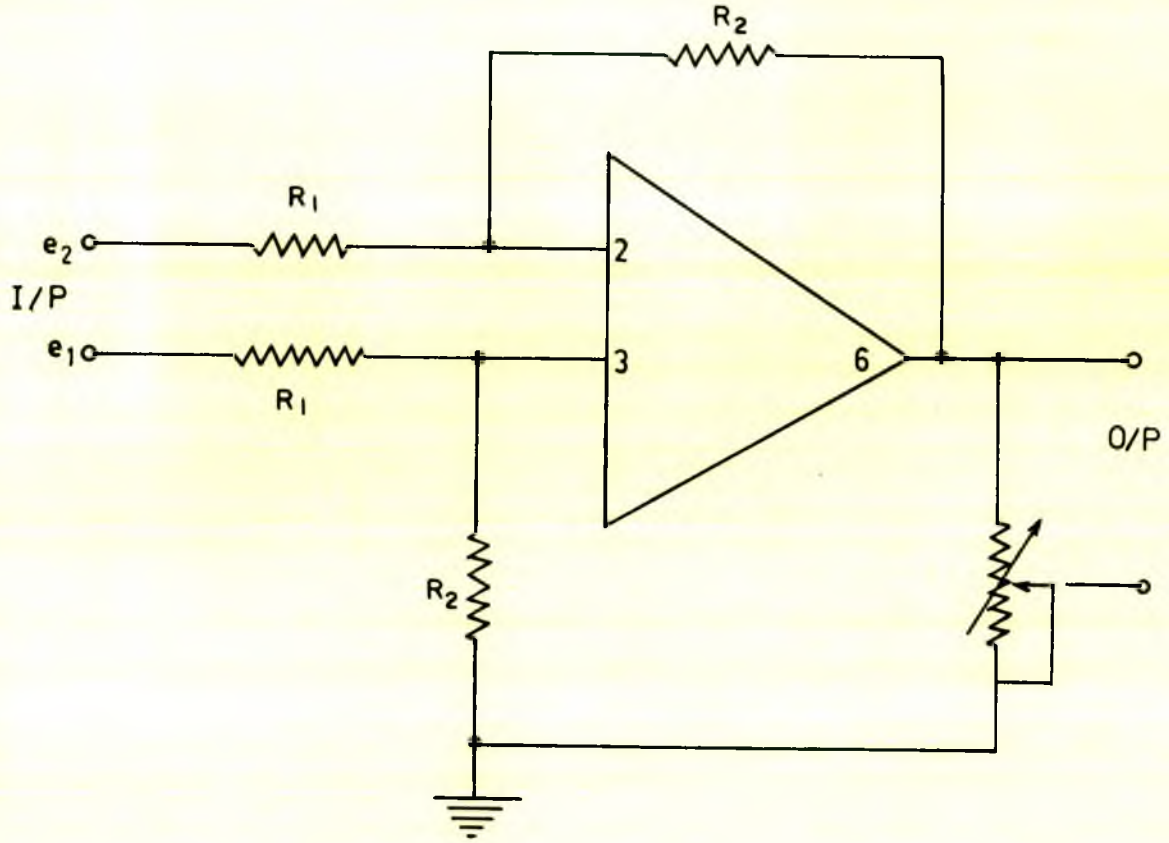


Fig.3 Differential amplifier circuit

differential amplifier the output e_o is given by

$$e_o = A_d V_d (1 + 1/c)(v_c/v_d)$$

So a "diff. amp." should be designed such that c is very large compared to v_c/v_d . Normally an op-amp when used as a diff-amp, with two input resistors (R_i's) the input impedance turns out to be $Z_i = 2R_i$. The circuit is shown in Fig. 31.

5.2 CONSTRUCTION OF SAMPLE HOLDER AND VARIABLE TEMPERATURE CRYOSTAT SYSTEM:

5.2.1 A fixed temperature Cryostat:

For measuring diode current junction capacitance at low temperature, we need a fixed temperature cryostat system and a sample- holder which could be immersed in the cryogenic liquid.

For this purpose we used a liquid nitrogen thermoflask which was well covered with heat insulating material (synthetic foam) into which goes a long sample holder made of a steel pipe and perspex material. On to the perspex sample holder the diode- with its electrical connection and a Cu-constantan thermocouple junction are fixed; the other junction of the thermocouple is kept at melting ice. All the connecting wires goes through the hollow

steel pipe for external electric connection. The temperature of the sample is then raised by slowly removing the flask out. The temperature rise rate is kept constant by blowing a stream of air on to the sample. This also prevents formation of ice on the sample and other electrical contacts. For monitoring the temperature from 77°K to 300°K, we used liquid nitrogen. But, to start from a upper temperature-point we used a mixture of solid carbon dioxide and ethanol (193°K) or a variable temperature cryostat described below.

5.2.2 Variable temperature cryostat system:

In order to scan and monitor from a different starting temperature point, we need a variable temperature cryostat system. In order to suit our purpose we have designed a simple but effective system. The system consists of an L-shaped thick solid Cu-rod of 12" long, the L-bent being 4" - 5" long. L-bent portion has a groove into which the sample is inserted together with the thermocouple junction (Fig.32). The legs of the diodes are connected to the deferential input of the capacitance measuring meter or the electrical connection for TSC measurement. The straight end of the Cu-rod goes into the thermoflask as described above containing boiling liquid nitrogen. After a few minutes temperature of the "cold-finger" gets stabilized. By varying the length of the emerging part of the rod we can decrease or increase

the temperature by a step of 10-15°K. As before after stabilizing the temperature we withdraw the flask and allow the temperature of the system to rise.

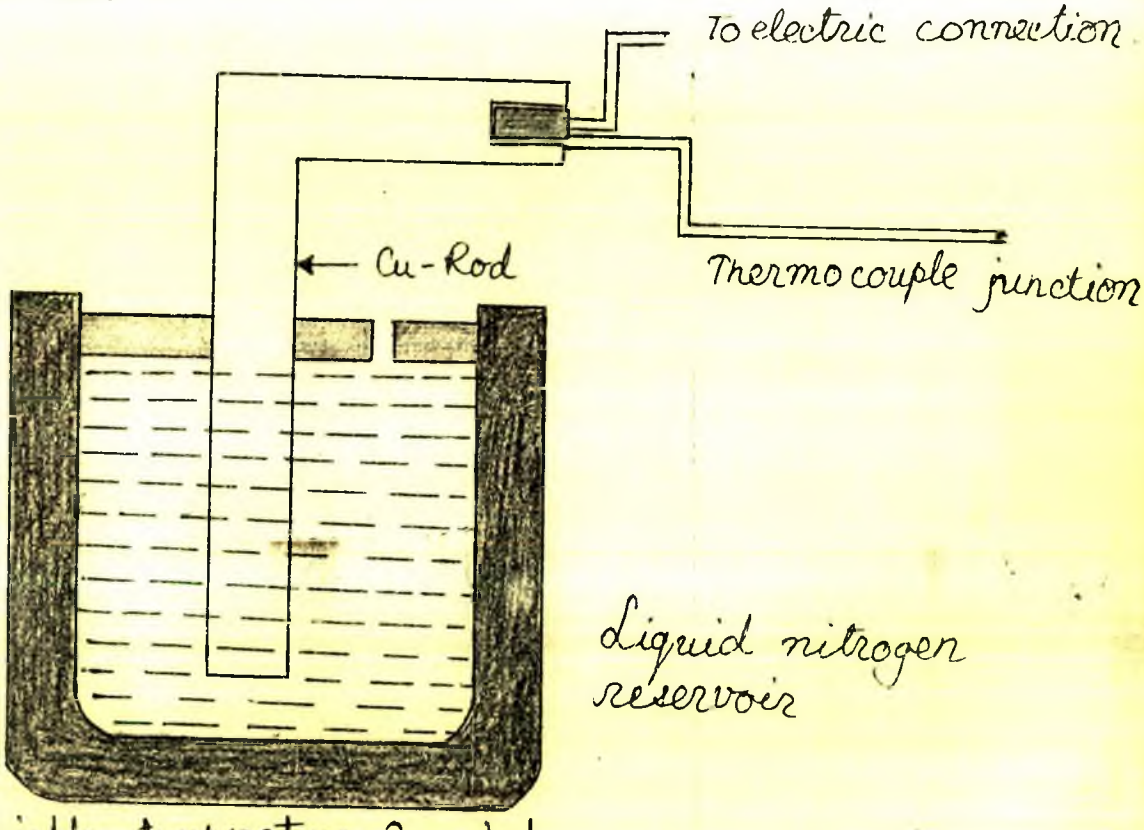


FIG. 32. Variable temperature Cryostat.

5.3 CAPACITANCE MEASURING METER:

Obviously to measure junction capacitance of a semiconducting device one needs a very sensitive and sophisticated measuring system. Normally junction capacitance are in the range of pico-farads. We used a commercial capacitance meter called BOONTON (Model 72B) capacitance bridge. The measuring range is from 0.01 pf to 3000 pf. The operating frequency is ~ 1 MHz. It gives out an analog output, proportional to the value of the

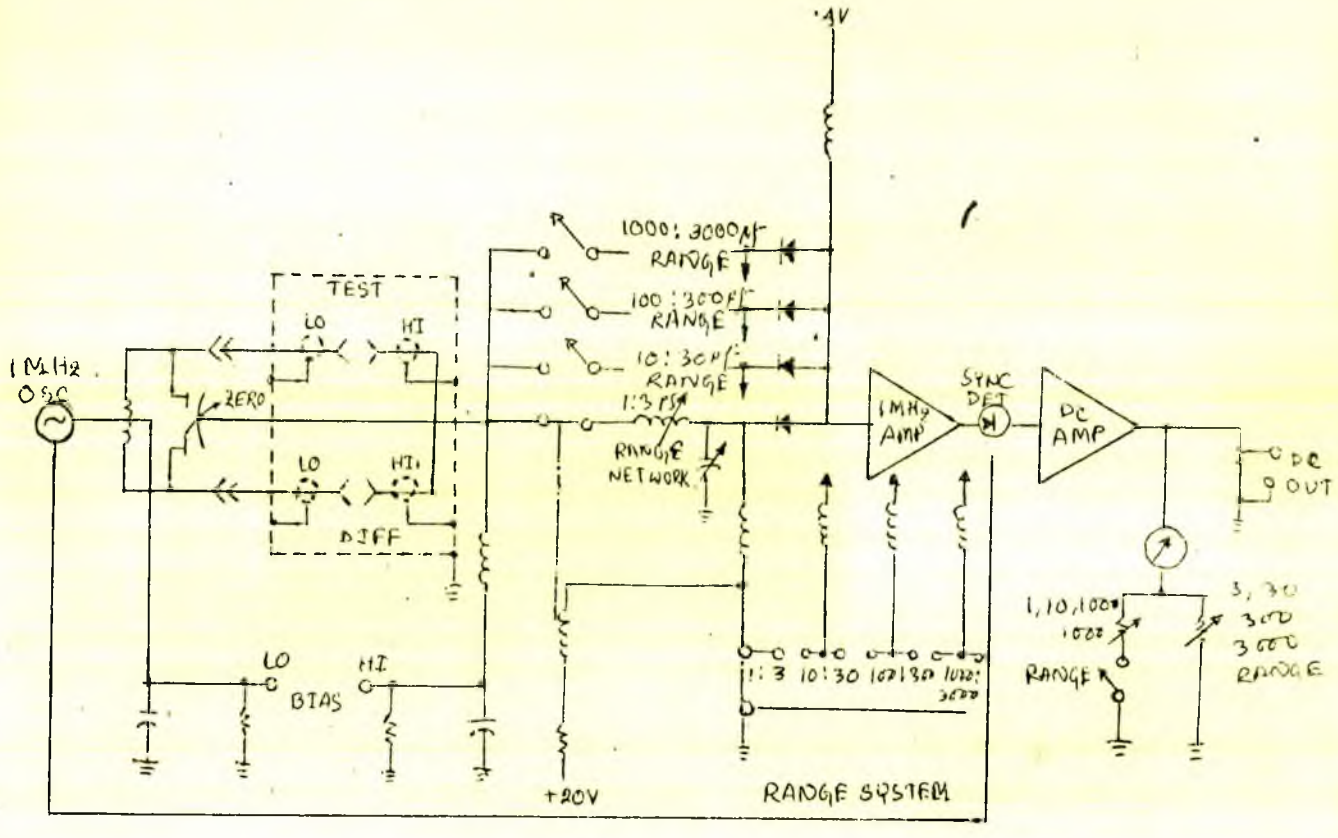


FIG :33 Simplified Schematic diagram of Capacitive

capacitance which can be processed at our will. The sample can be biased via the bias terminal of the meter to a maximum value of 100 volt.

The basic principle on which the meter operates may be stated here in brief. The output of the operating frequency (1MHz) generated from a crystal controlled oscillator, appears across a secondary of a transformer whose central tap is grounded via a capacitor (Fig. 33).

The specimen whose capacitor is to be measured is connected between Lo and Hi test terminals. A current proportional to the susceptance flows through the low impedance series resonant LC-Circuit to ground. The resultant voltage that appears across the capacitance part of the LC circuit is fed, through a tuned amplifier to the synchronous detector. The detector converts the 1 MHz-signal to dc and applies it to the dc amplifier section. The output of the amplifier drives the panel meter and a voltage divider which supplies an adjustable analog output at the rear terminals and also on the rear connector for external indicator or control purpose. However one aspect of the meter, when used to measure transient capacitance response, should be kept in mind. Such a meter works very well for measuring the steady state capacitance, but has certain shortcomings for transient measurement i.e. capacitance change in a very short time. First, its rather slow output time constant (typically ~ 1 msec.) gives

rise to a rather long pulse overload recovery transient. This poses some problem to measure transients faster than 1 msec. Second, in a measuring technique such as DLTS wherein the sample is subject to a repetitive bias pulse, there is no provision for the introduction of a fast bias pulse. The normal bias input reaches the sample through a heavily filtered dc-network which has a long time constant. However, since we are using a single shot transient method, those limitations of the bridge do not seriously affect our measurement. Inspite of the shortcomings mentioned above, the Boonton capacitance meter is widely used for transient capacitance measurement.

5.4 CONSTANT TEMPERATURE BATH:

For the measurement of reverse saturation current at higher temperatures (from 300°K to 470°K) we need to increase the sample-temperature in a constant temperature bath whose temperature must be kept constant during measurement. We have, in our laboratory, constructed a simple constant temperature bath by using a RS-supplied μ-processor controlled temperature controlling system. The controlling system is connected to a immersion heater placed inside a large thermoflask containing water. The temperature could be set from a dial with $\pm$ 2°C. As the temperature goes higher than the set value the heater circuit

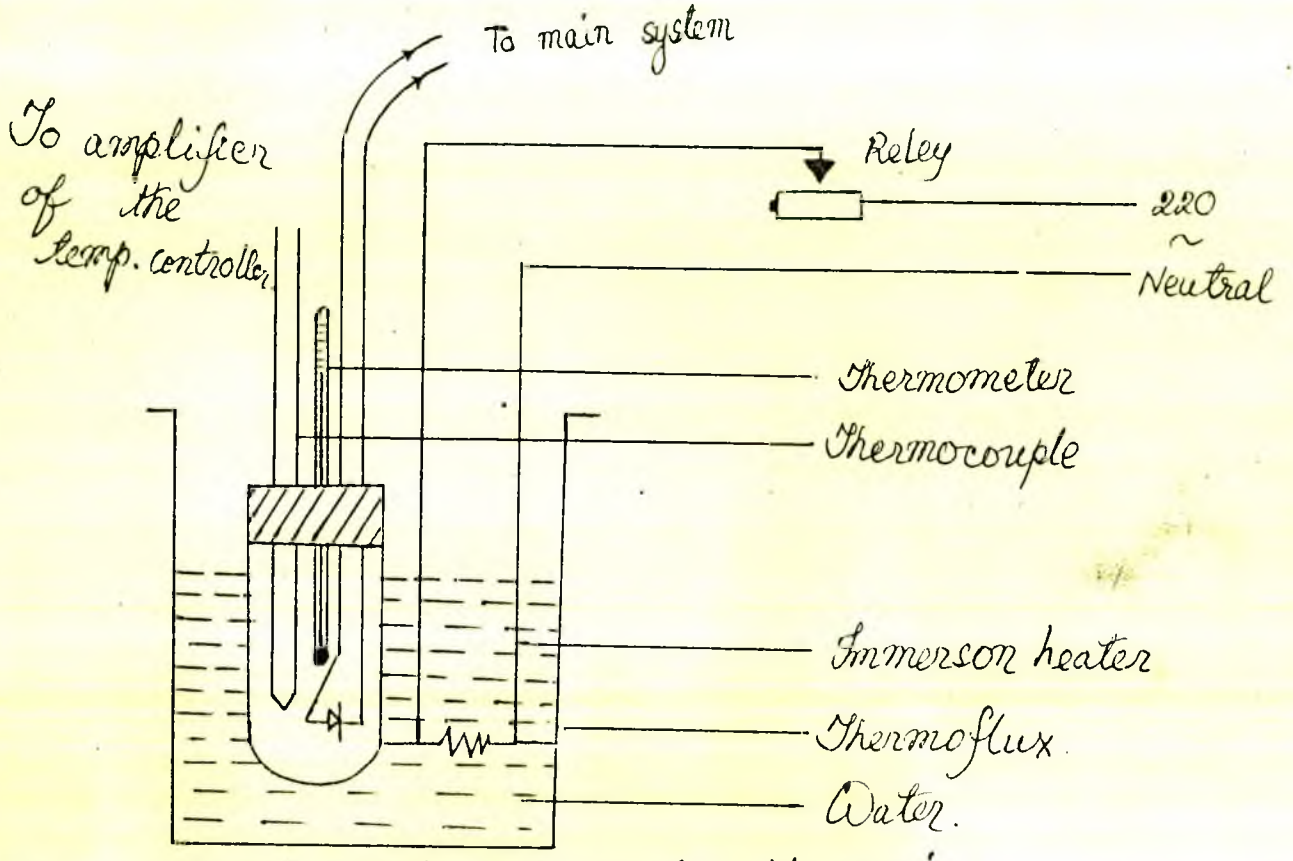


Fig. 34a Experimental Set up for Measuring Reverse Saturation Current.

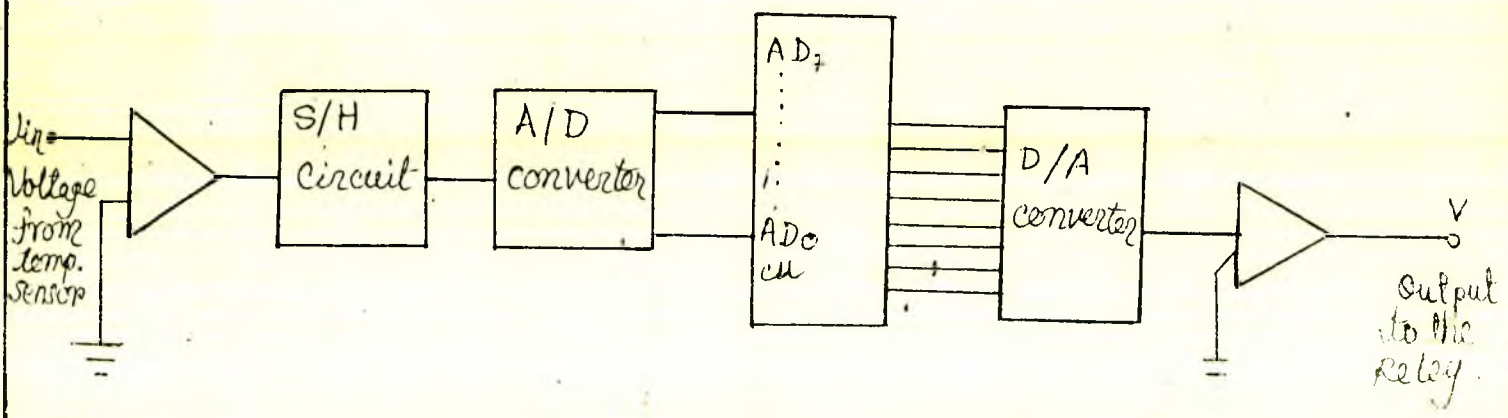


Fig: 34b Microprocessor Controlled constant temperature System.

breaks down or vice versa. The circuit diagram of the system is shown in Fig. 34b.

5.5 I-V Measurement:

For measuring diode current under forward bias, the power is supplied by a highly stabilized d.c. power supply. The voltage across the diode is measured with a digital voltmeter and current through the device by a Keithley electrometer (type 610°C) which can measure current from 0.3 amp to 10^{-14} amp. The diode is inserted on a specially constructed holder and the entire system is placed within an electrically shielded box.

For reverse bias measurement, the sample with its electrical connection and a junction of K-type thermocouple is placed within a thin-walled pyrex tube. The tube is then immersed in the constant temperature bath described above. At different temperature the reverse saturation current are measured using the above mentioned electrometer and the diode-voltage by a digital voltmeter (Fig. 34a).

From both I-V measurements the η-factor used in an empirical diode current formula, cut-in voltage (V_γ), forward resistance (R_f) and saturation current value (I_s) at room temperature have been evaluated.

5.6 C-V MEASUREMENT:

C-V measurement of the devices at room temperature is very simple one. The sample is directly connected to the appropriate terminal of the Boonton capacitance bridge. The d.c. bias is supplied from a highly stabilized power unit and corresponding capacitance is recorded from the capacitance analog output or may be obtained directly from the meter.

The low temperature measurement is done using those cryostatic arrangement and special sample holder described earlier. When special holder are used stray capacitance is usually introduced, which is eliminated by the use of differential input terminal and inserting appropriate standard capacitance on to the differential input.

From the C-V measurement the intrinsic contact potential, (V_o), intrinsic capacitance of the depletion layer (C_o), and shallow level impurity concentration are estimated.

5.7 TRANSIENT MEASUREMENT:

5.7.1 Transient Capacitance Measurement (TSCAP):

This involves our major measuring set up. The following steps are followed:

1. For fixed temperature cryostatic measurement, the sample, its bias connection, and a thermocouple junction-end, - all together mounted on a specially constructed holder.

2. The sample is then subject to a suitable quiescent bias at room temperature. This ensures that defect levels are fully ionized and empty of carriers.

3. The sample is then immersed directly in a liquid nitrogen (or ethanol-solid Carbon dioxide mixture) reservoir and quiescent bias is then reduced to zero. This will fill in the empty deep level traps present in the depletion region. After a few seconds or so, the bias is restored to its quiescent value. The capacitance is then noted and its corresponding analog output, which is connected to one end of the differential amplifier described earlier. The other end of the differential amplifier is fed with equal amount of d.c. voltage, so that output of amplifier is brought to zero or near zero. This procedure facilitates the observation of capacitance change if any. The amplification is adjusted to a suitable level depending on the change observed. The

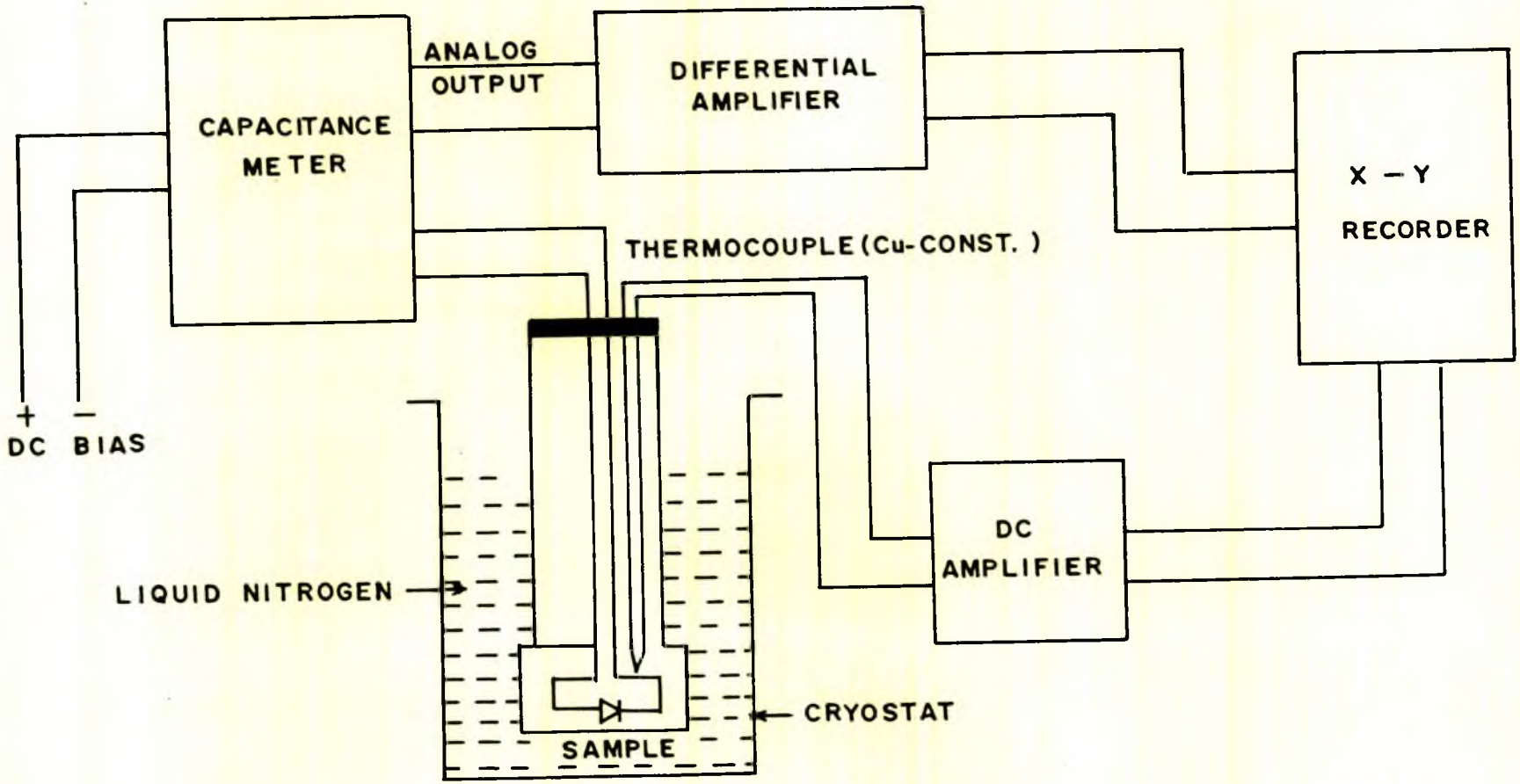


Fig.35 BLOCK DIAGRAM OF TSCAP SET-UP.

output of the differential amplifier is connected to the Y-input of a X-Y recorder. X-axis of the recorder is driven by thermocouple voltage amplified through an amplifier. The system is allowed to reach equilibrium and then the liquid nitrogen dewar (or the holder is moved out of the liquid nitrogen) to raise the temperature of the sample at a fairly constant rate. The capacitance steps will be automatically recorded by the recorder as the sample reaches appropriate temperature corresponding to emission rate of a particular trap centre. In order to scan different temperature zone, the variable temperature cryostat system is used in place of fixed temperature cryostat. The entire experimental set up is shown in fig. 35.

5.7.2 Thermally stimulated current measurement (TSC):

As discussed earlier, the thermally stimulated current measurement technique is basically same, but transient is observed in the reverse saturation current of the junction diode. The following steps are followed:

1. The device under observation is suitably reverse biased, so that depletion layer deep-states are completely empty. As before sample is then cooled to liquid nitrogen using the specially constructed cryostat system. The diode is connected in series with a Keithley electrometer for measuring current; a

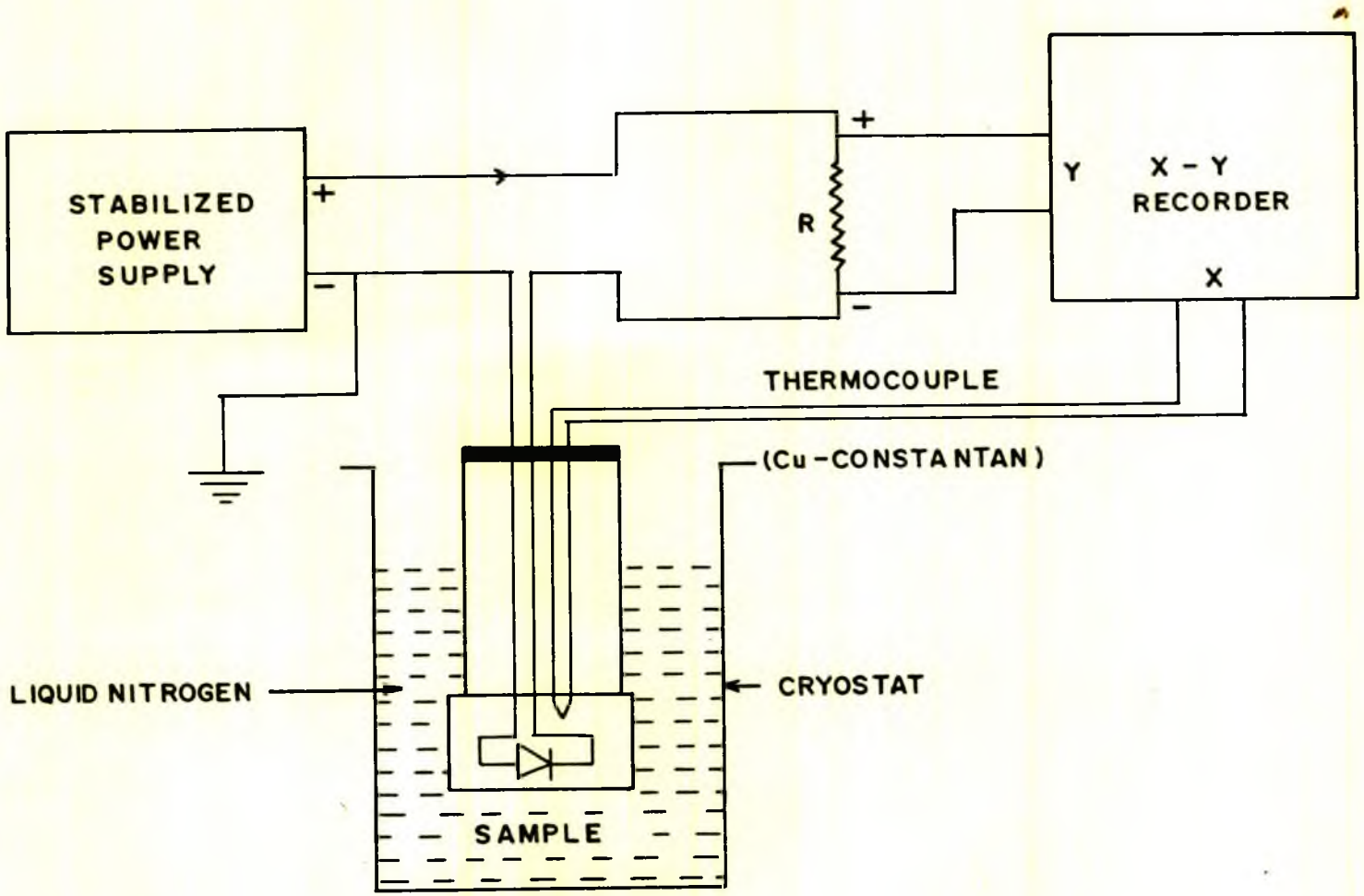


Fig. 36 TSC MEASURMENT SYSTEM

suitable drop-resistor is also connected in series in the circuit. Across the drop resistor is connected the Y input of X-Y recorder with X-axis being driven by the thermocouple voltage; Y-axis thus records the current change.

2. As before the temperature of the sample is then raised either by removing the cryostat or the sample holder. Under various temperature scanning rate observations are made. As the sample temperature reaches the appropriate emission rate, traps are emptied and a TSC peak will be recorded. The experimental setup is shown in Fig. 36.

From the TSCAP slope and TSC peak one can evaluate the ionization energy of a trap level and the trap concentration.

As many as 50 devices including a few transistor samples were investigated and results of some of these devices are reported in the next chapter.

CHAPTER SIX

RESULTS AND DISCUSSION

6.1 I-V MEASUREMENTS:

6.1.1 Forward bias: analysis of data

As mentioned earlier we have investigated over fifty p-n junction devices, mostly in the form of diodes. We report result of about twenties or so. This is because most results are similar and of repetitive nature. Some representative experimental data and their results are presented here.

From forward bias I-V data we estimated η-factor, reverse saturation current I_o at the temperature of observation. These parameters are evaluated using the empirical diode equation (1.42)

$$I = I_o \left[\exp (V/\eta V_T - 1)\right]$$

As discussed in the formulation part, η and I_o can be found from the 'slope' and 'intercept' of lnI VS V plot in low current region; thus

$$\eta = 1/(\text{slope} \times V_T)$$

with $$V_T = \frac{T}{11,000}$$

and $$\ln I_o = \text{"intercept"}$$

The offset or threshold-voltage V_γ and forward resistance R_f have been calculated from the plot of I against V in the region of high current where exponential law gives way to the 'ohmic law'. Slope gives the inverse of R_f and intercept on voltage axis is the measure of threshold voltage V_γ.

These parameters for various junctions are summerised in the Table-9.

TABLE - 6(a): Experimental data of I-V measurement at room temperature; Sample: Silicon

Sample: Si-0103(1)

No. of obs.	Forward bias voltage V(volts)	Forward current I(mA)
1	0.55	0.01
2	0.60	0.04
3	0.70	0.08
4	0.75	0.125
5	0.85	0.165
6	0.95	0.205
7	1.10	0.24
8	1.15	0.285
9	1.25	0.325
10	1.30	0.37
11	1.40	0.41

Sample: Si-0103(2)

1	0.067	0.015
2	0.098	0.027
3	0.124	0.048
4	0.224	0.1
5	0.328	0.16
6	0.441	0.236
7	0.570	0.335
8	0.766	0.492
9	0.859	0.580
10	1.134	0.810

TABLE - 6(a): Experimental data of I-V measurement at room temperature; Sample: Silicon

Sample: Si-2N2369(NPN)
(Base-Collector)

No. of obs.	Forward bias voltage V(volts)	Forward current I(amp $\times 10^{-4}$)
1	0.5	0.0025
2	0.6	0.0325
3	0.7	0.1030
4	0.8	0.1850
5	1.0	0.3561
6	1.2	0.5450
7	1.4	0.7310
8	1.6	0.9250

Sample: Si-NTE50(NPN)
Base-Emitter

No. of obs.	Forward bias voltage V(volts)	Forward current I(mA)
1	0.50	0.015
2	0.55	0.04
3	0.60	0.07
4	0.65	0.103
5	0.70	0.145
6	0.80	0.225
7	0.90	0.310
8	1.00	0.395

Sample: NTE-50(NPN)
(Base-Collector

1	0.50	0.033
2	0.55	0.055
3	0.60	0.083
4	0.65	0.110
5	0.70	0.141
6	0.80	0.208
7	0.90	0.283
8	1.00	0.340

TABLE - 6(b) Experimental data for I-V measurement (at room temperature) Samples - Germanium

Sample: GE-110MP(1)

No. of obs.	Forward bias voltage V(volts)	Forward current I(mA)
1	0.10	0.012
2	0.15	0.034
3	0.20	0.062
4	0.25	0.095
5	0.30	0.13
6	0.40	0.207
7	0.50	0.280
8	0.60	0.359

Sample: Ge-2SB56 (PNP) (Base-Collector)

1	0.067	0.015
2	0.098	0.027
3	0.124	0.048
4	0.224	0.1
5	0.328	0.16
6	0.441	0.236
7	0.570	0.335
8	0.766	0.492
9	0.859	0.580
10	1.003	0.694
11	1.134	0.81
12	1.272	0.925

TABLE - 6(b) Experimental data for I-V measurement (at room temperature) Samples: Germanium

Sample: Ge-2SB54

No. of obs.	Forward bias voltage V(volts)	Forward current I(mA)
1	0.05	0.015
2	0.10	0.04
3	0.15	0.074
4	0.20	0.11
5	0.25	0.15
6	0.30	0.19
7	0.35	0.234
8	0.40	0.276
9	0.45	0.323
10	0.50	0.37
11	0.60	0.475
12	0.70	0.543
13	0.80	0.632
14	0.90	0.720
15	1.00	0.815
16	1.10	0.900

TABLE - 6(c) I-V measurement data (at room temperature): for GaAs samples.

Sample: GaAs-246(1)

No. of obs.	Forward bias voltage V(volts)	Forward current I(mA)
1	0.55	0.007
2	0.60	0.02
3	0.65	0.041
4	0.70	0.072
5	0.75	0.107
6	0.80	0.143
7	0.90	0.225
8	1.00	0.308

Sample: GaAs-246(2)

1	0.50	0.005
2	0.55	0.012
3	0.60	0.024
4	0.65	0.044
5	0.70	0.066
6	0.75	0.093
7	0.80	0.122
8	0.90	0.185
9	1.00	0.25

TABLE - 6(c) I-V measuerment data (at room temperature): for GaAs samples

Sample: GaAs-246(3)

No. of obs.	Forward bias voltage V(volts)	Forward current I(mA)
1	0.55	0.004
2	0.60	0.017
3	0.65	0.038
4	0.70	0.070
5	0.75	0.109
6	0.80	0.146
7	0.90	0.224
8	1.00	0.304

Sample: GaAs-246(4)

1	0.55	0.01
2	0.60	0.025
3	0.65	0.048
4	0.70	0.078
5	0.75	0.110
6	0.80	0.150
7	0.90	0.224
8	1.00	0.313

6.1.2 Reverse Saturation current study:

We also investigated the effect of temperature on reverse saturation current I_s and from the study we have evaluated η-factor from the plot of $\ln I_s$ against $1/T$. The measurement of I_s at various temperature has been done using a constant temperature bath and a highly stabilized power supply unit. The theory of measuring η from such plot has been discussed in the theoretical part (Eq. 1.44).

The result of our study is included in Table-9.

TABLE - 7: Data for Reverse Saturation Current Study

Sample: Ge-110MP(1)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-5}$) amp
20	0.05	0.023
	0.1	0.05
	0.15	0.073
	0.2	0.088
	0.3	0.105
	0.4	0.12
	0.5	0.13
	0.6	0.14
	0.75	0.155
	1.0	0.18
	1.25	0.204
	1.5	0.225
	1.75	0.247
	2.00	0.267
	2.5	0.31
37	0.1	0.076
	0.2	0.16
	0.3	0.233
	0.4	0.3
	0.5	0.345
	0.6	0.375
	0.75	0.41
	1.0	0.47
	1.25	0.52
	1.5	0.565
	1.75	0.616
	2.00	0.655
	2.5	0.745
	3.0	0.82
45	0.1	0.08
	0.2	0.17
	0.3	0.255
	0.4	0.34
	0.5	0.42
	0.6	0.49
	0.75	0.57
	1.0	0.65
	1.25	0.715
	1.5	0.78
	1.75	0.837
	2.00	0.895
	2.5	1.2
	3.0	1.9

TABLE - 7: Data for Reverse Saturation Current Study

Sample: Ge-110MP(1)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-5}$) amp
59	0.1	0.66
	0.2	1.1
	0.3	1.25
	0.4	1.3
	0.5	1.4
	0.6	1.47
	0.75	1.55
	0.0	1.67
	1.25	1.77
	1.5	1.8
	1.75	2.0
	2.00	2.1
	2.5	2.33
	3.00	2.5
69	0.1	0.7
	0.2	1.45
	0.3	2.0
	0.4	2.38
	0.5	2.4
	0.6	2.50
	0.75	2.63
	1.0	2.84
	1.25	3.0
	1.5	3.1
	1.75	3.28
	2.00	3.4
	2.5	3.7
	3.00	3.95

TABLE - 7: Data for Reverse Saturation Current Study

Sample: Si-NTE50

(Base-Emitter)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-6}$) amp
22.5	0.5	0.004
	1.0	0.008
	1.5	0.012
	2.0	0.017
	2.5	0.02
	3.0	0.024
	3.5	0.03
	4.0	0.035
35	0.5	0.012
	1.0	0.02
	1.5	0.035
	2.0	0.05
	2.5	0.07
	3.0	0.10
	3.5	0.12
	4.0	0.17
45	0.5	0.02
	1.0	0.05
	1.5	0.07
	2.0	0.1
	2.5	0.12
	3.0	0.14
	3.5	0.2
	4.0	0.26
54.5	0.5	0.1
	1.0	0.13
	1.5	0.16
	2.0	0.19
	2.5	0.22
	3.0	0.25
	3.5	0.34
	4.0	0.48
64	0.5	0.10
	1.0	0.20
	1.5	0.24
	2.0	0.28
	2.5	0.34
	3.0	0.43
	3.5	0.50
	4.0	0.64

TABLE - 7: Data for Reverse Saturation Current Study

Sample: Si-NTE50(PNP)

(Base-Collector)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-8}$) amp
22.5	0.55	0.01
	0.75	0.03
	1.0	0.038
	1.25	0.045
	1.5	0.053
	1.75	0.058
	2.0	0.062
	2.5	0.07
	3.0	0.078
	3.5	0.083
	4.0	0.09
30	0.55	0.01
	0.75	0.055
	1.0	0.1
	1.25	0.118
	1.5	0.134
	1.75	0.148
	2.0	0.16
	2.5	0.183
	3.0	0.195
	3.5	0.205
	4.0	0.217

TABLE - 7: Data for Reverse Saturation Current Study

Sample: Si-NTE50(PNP)

(Base-Collector)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-8}$)amp
44.5	0.55	0.12
	0.75	0.17
	1.0	0.23
	1.25	0.24
	1.5	0.26
	1.75	0.28
	2.0	0.30
	2.5	0.34
	3.0	0.37
	3.5	0.4
	4.0	0.42
52	0.55	0.25
	0.75	0.37
	1.0	0.45
	1.25	0.54
	1.5	0.6
	1.75	0.65
	2.0	0.7
	2.5	0.77
	3.0	0.82
	3.5	0.85
	4.0	0.9
64	0.55	0.6
	0.75	0.8
	1.0	1.0
	1.25	1.15
	1.5	1.28
	1.75	1.32
	2.0	1.5
	2.5	1.63
	3.0	1.73
	3.5	1.8
	4.0	1.9

TABLE - 7: Data for Reverse Saturation Current Study

Sample: GaAs-246(1)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-7}$) amp
22	0.05	0.007
	0.1	0.01
	0.2	0.014
	0.3	0.017
	0.5	0.022
	0.75	0.028
	1.0	0.034
	1.5	0.047
	2.0	0.058
	2.5	0.07
	3.0	0.08
35	0.05	0.009
	0.1	0.015
	0.2	0.023
	0.3	0.028
	0.5	0.034
	0.75	0.04
	1.0	0.045
	1.5	0.053
	2.0	0.06
	2.5	0.07
	3.0	0.078

TABLE - 7: Data for Reverse Saturation Current Study

Sample: GaAs-246(1)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-7}$) amp
44.5	0.05	0.13
	0.1	0.25
	0.2	0.37
	0.3	0.44
	0.5	0.54
	0.75	0.6
	1.0	0.68
	1.5	0.8
	2.0	0.9
	2.5	1.0
	3.0	1.1
57	0.05	0.2
	0.1	0.5
	0.2	0.7
	0.3	0.98
	0.5	1.3
	0.75	1.4
	1.0	1.53
	1.5	1.65
	2.0	1.78
	2.5	1.95
	3.0	2.3

TABLE - 7: Data for Reverse Saturation Current Study

Sample: GaAs-246(2)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-7}$) amp
20	0.05	0.007
	0.1	0.02
	0.2	0.054
	0.3	0.12
	0.4	0.177
	0.5	0.264
	0.6	0.335
	0.7	0.42
	0.8	0.535
	0.9	0.613
	1.0	0.7
	1.25	0.95
30	0.1	0.07
	0.2	0.12
	0.3	0.18
	0.4	0.245
	0.5	0.32
	0.6	0.39
	0.7	0.47
	0.8	0.55
	0.9	0.64
	1.0	0.75
	1.25	0.96
44.5	0.1	0.072
	0.2	0.13
	0.3	0.19
	0.4	0.255
	0.5	0.33
	0.6	0.405
	0.7	0.513
	0.8	0.58
	0.9	0.68
	1.0	0.76
	1.25	0.99

TABLE - 7: Data for Reverse Saturation Current Study

Sample: GaAs-246(2)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-6}$) amp
	0.1	0.055
	0.2	0.135
	0.3	0.195
	0.4	0.27
54.5	0.5	0.34
	0.6	0.42
	0.7	0.53
	0.8	0.6
	0.9	0.69
	1.0	0.78
	1.2	0.90
	0.1	0.013
	0.2	0.035
	0.3	0.07
	0.4	0.097
64	0.5	0.17
	0.6	0.237
	0.7	0.31
	0.8	0.4
	0.9	0.48
	1.0	0.57
	1.25	0.67

TABLE - 7: Data for Reverse Saturation Current Study

Sample: GaAs-246(4)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-7}$) amp
20	0.05	0.01
	0.1	0.021
	0.15	0.027
	0.2	0.031
	0.3	0.035
	0.5	0.038
	0.75	0.040
	1.25	0.044
	2.0	0.050
	2.5	0.057
	3.0	0.073
35	0.15	0.15
	0.2	0.24
	0.25	0.28
	0.3	0.32
	0.4	0.37
	0.5	0.4
	0.6	0.43
	0.75	0.45
	1.0	0.48
	1.25	0.52
	2.0	0.58
	2.5	0.67

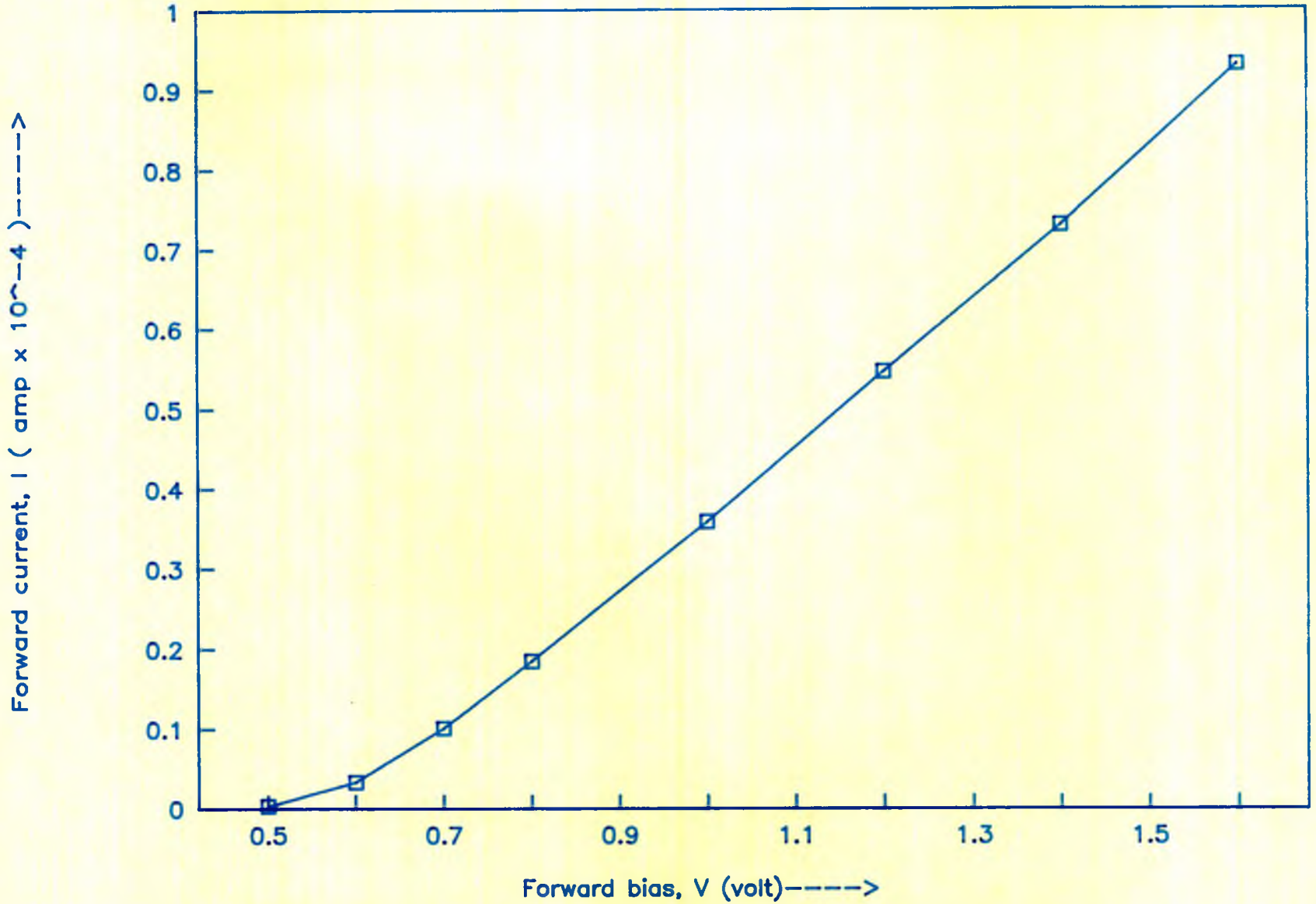
TABLE - 7: Data for Reverse Saturation Current Study

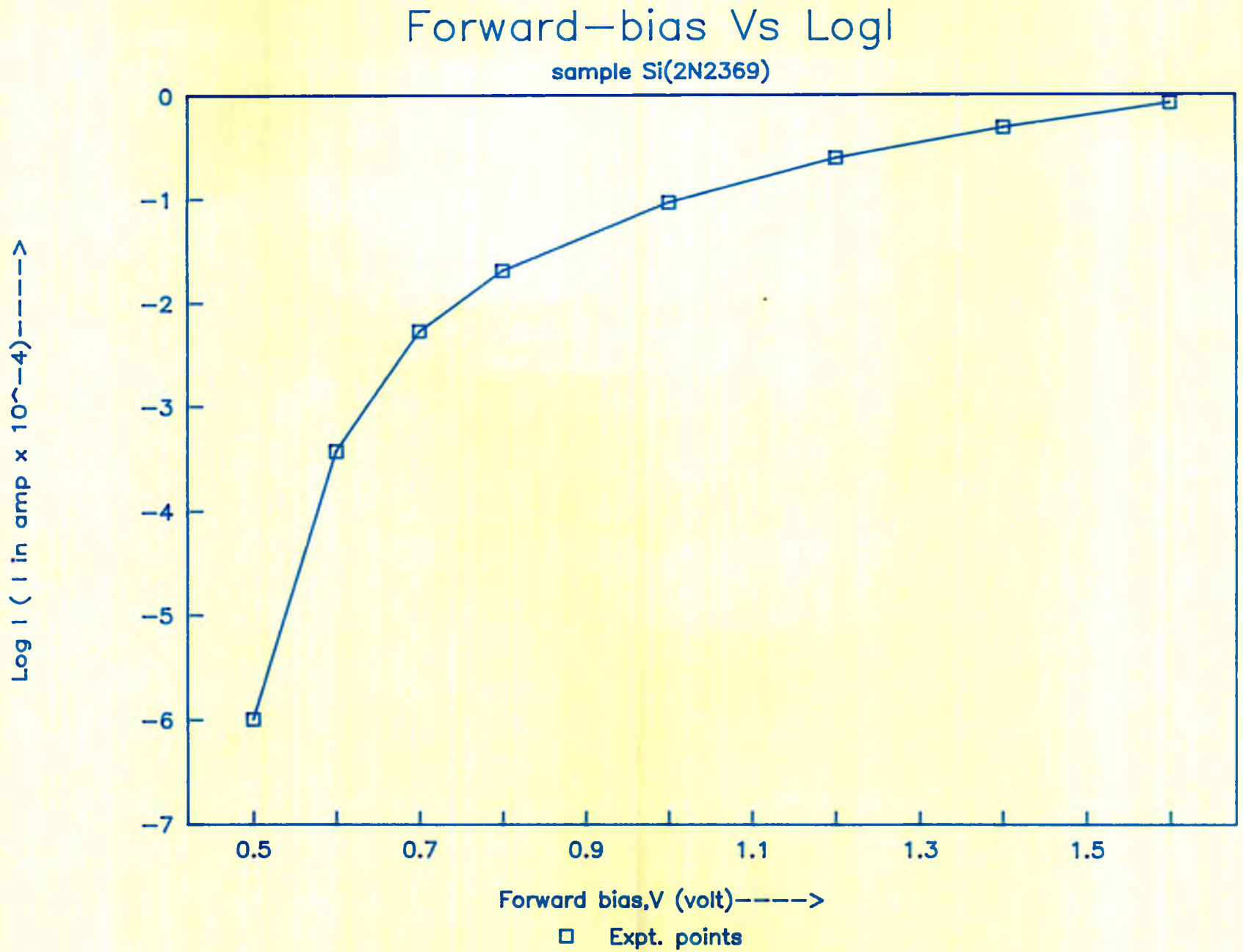
Sample: GaAs-246(4)

Temperature (°C)	Voltage (volts)	Current ($I \times 10^{-7}$)amp
44.5	0.15	0.16
	0.2a	0.24
	0.25	0.37
	0.3	0.45
	0.4	0.53
	0.5	0.58
	0.6	0.62
	0.75	0.67
	1.0	0.7
	1.50	0.77
	2.0	0.85
	2.5	1.0
	3.0	1.23
52	0.15	0.3
	0.2	0.45
	0.25	0.57
	0.3	0.65
	0.4	0.8
	0.5	0.88
	0.6	0.98
	0.75	1.02
	1.0	1.05
	1.50	1.13
	2.0	1.24
	2.5	1.4
	3.0	1.65
64	0.15	0.35
	0.2	0.57
	0.25	0.78
	0.3	0.9
	0.4	1.17
	0.5	1.35
	0.6	1.47
	0.75	1.63
	1.0	1.78
	1.50	1.95
	2.0	2.12
	2.5	2.35
	3.0	2.7

Forward bias Vs forward current

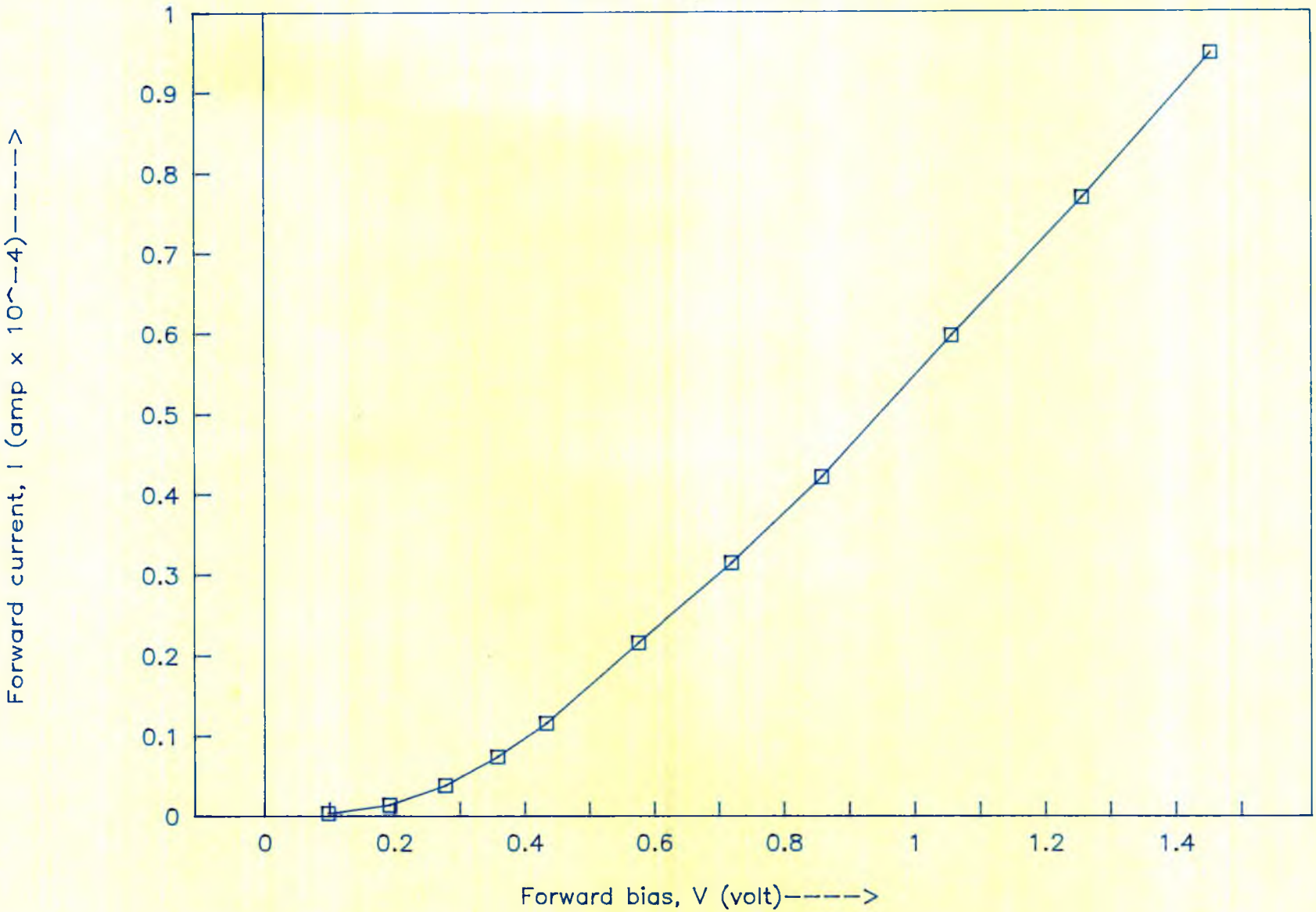
Sample: Si–2N2369

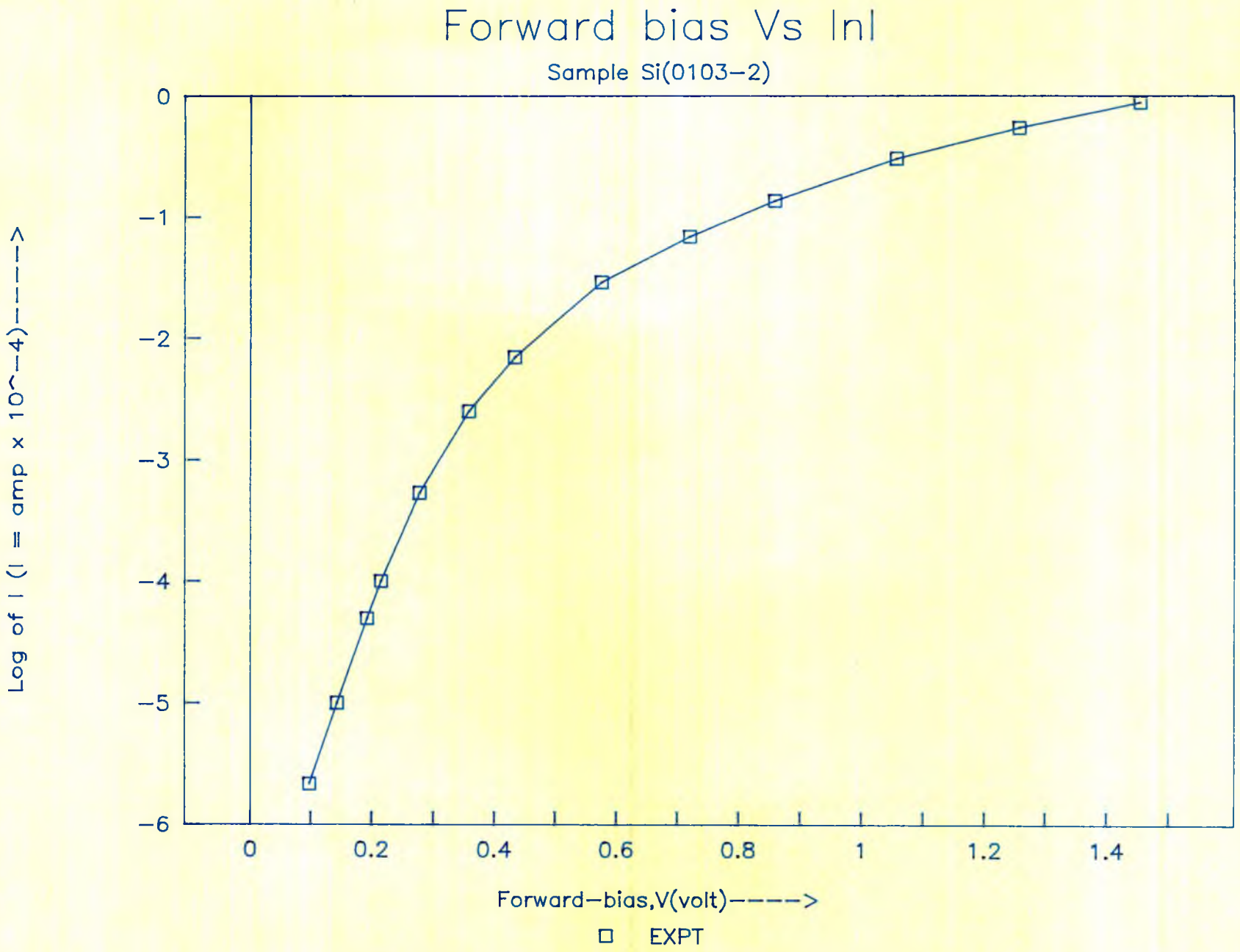



Forward–bias Vs Logl
sample Si(2N2369)
0
−1
−2
−3
−4
−5
−6
−7
0.5
0.7
0.9
1.1
1.3
1.5
Log I (I in amp x 10^−4)−−−−>
Forward bias,V (volt)−−−−>
Expt. points

Forward bias Vs forward current

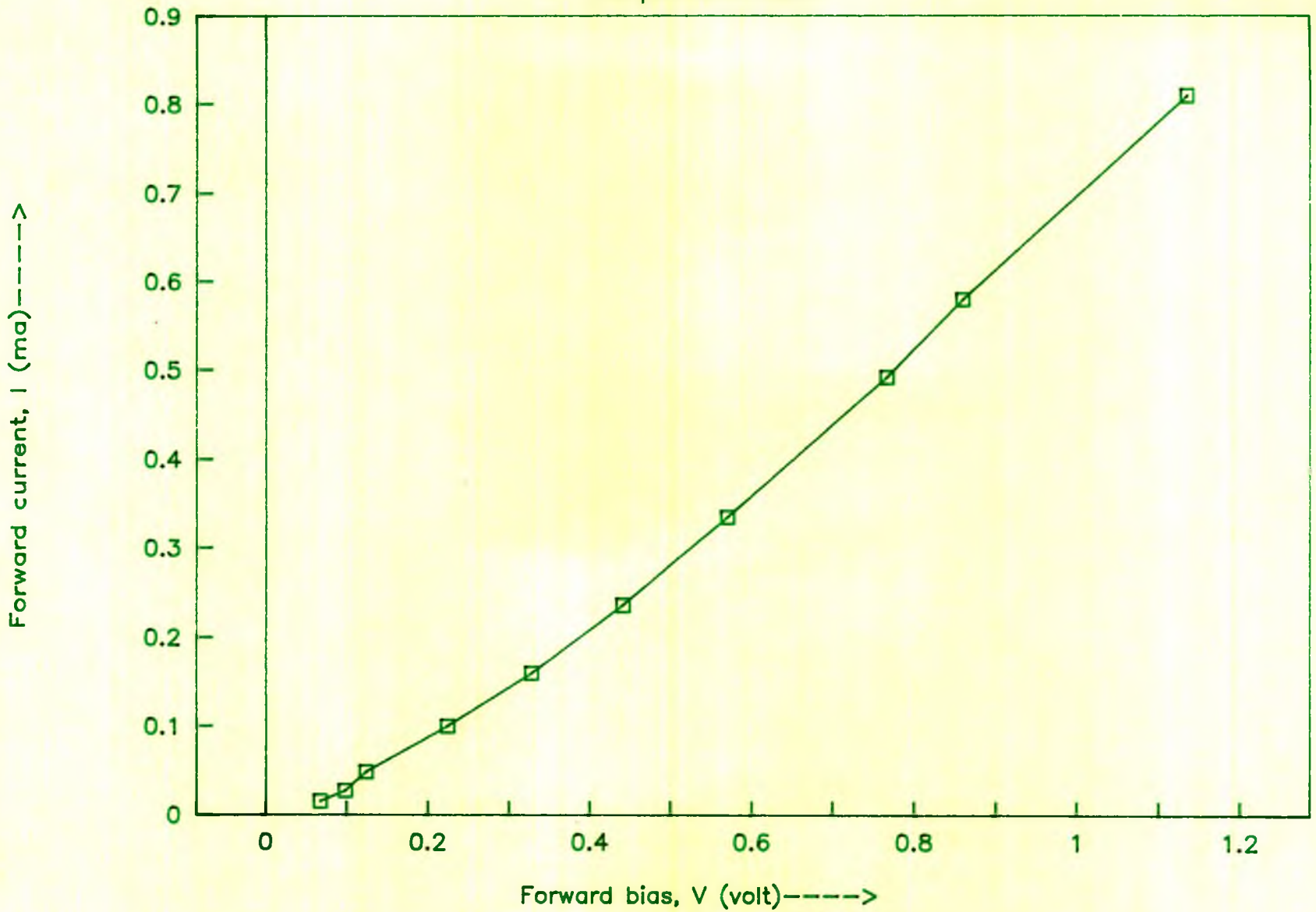
Sample: Si-0103 (2)

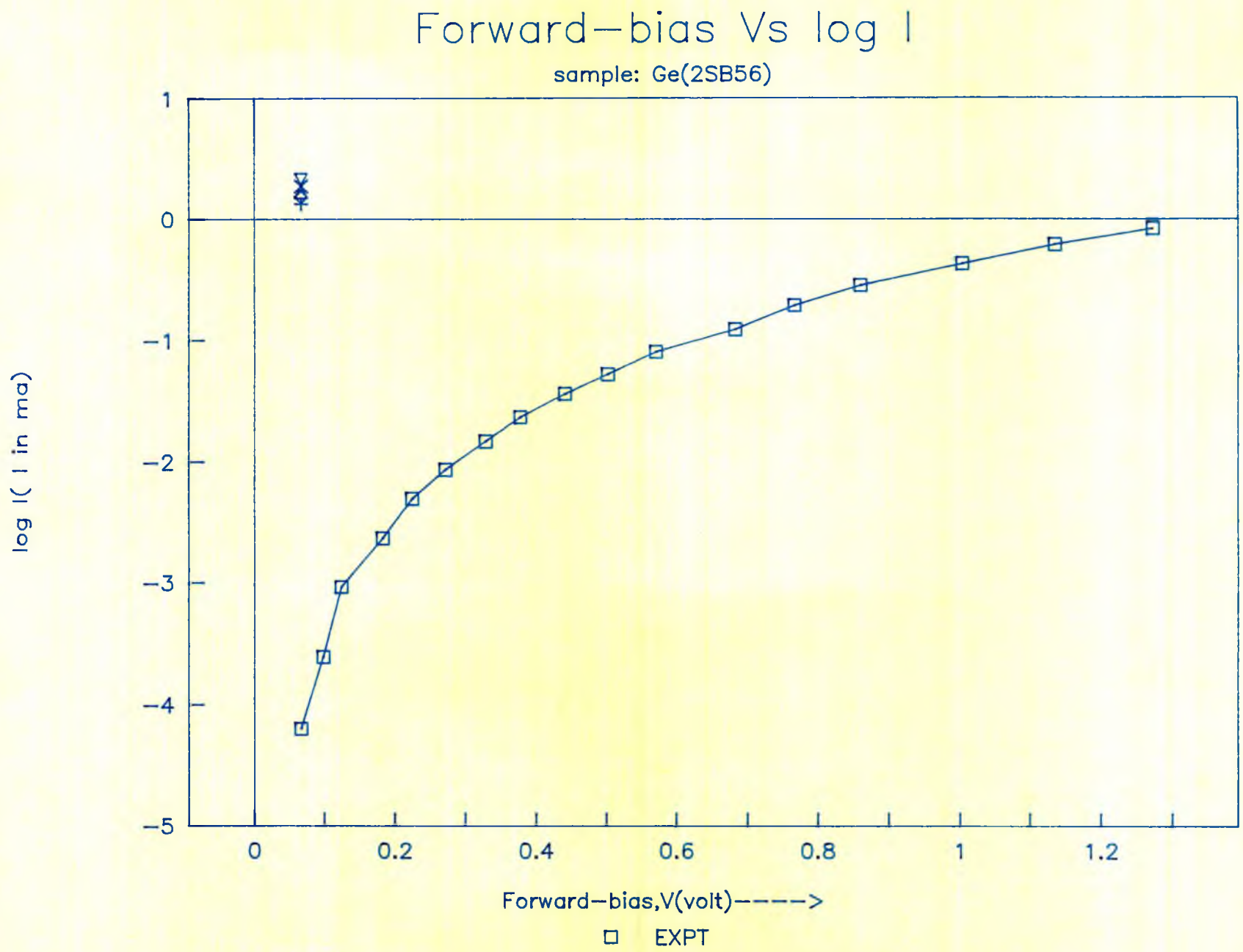



Forward bias Vs Inl
Sample Si(0103-2)
Log of I (I = amp x 10^-4)----->
0
-1
-2
-3
-4
-5
-6
0
0.2
0.4
0.6
0.8
1
1.2
1.4
Forward-bias,V(volt)---->
EXPT

Forward bias Vs forward current

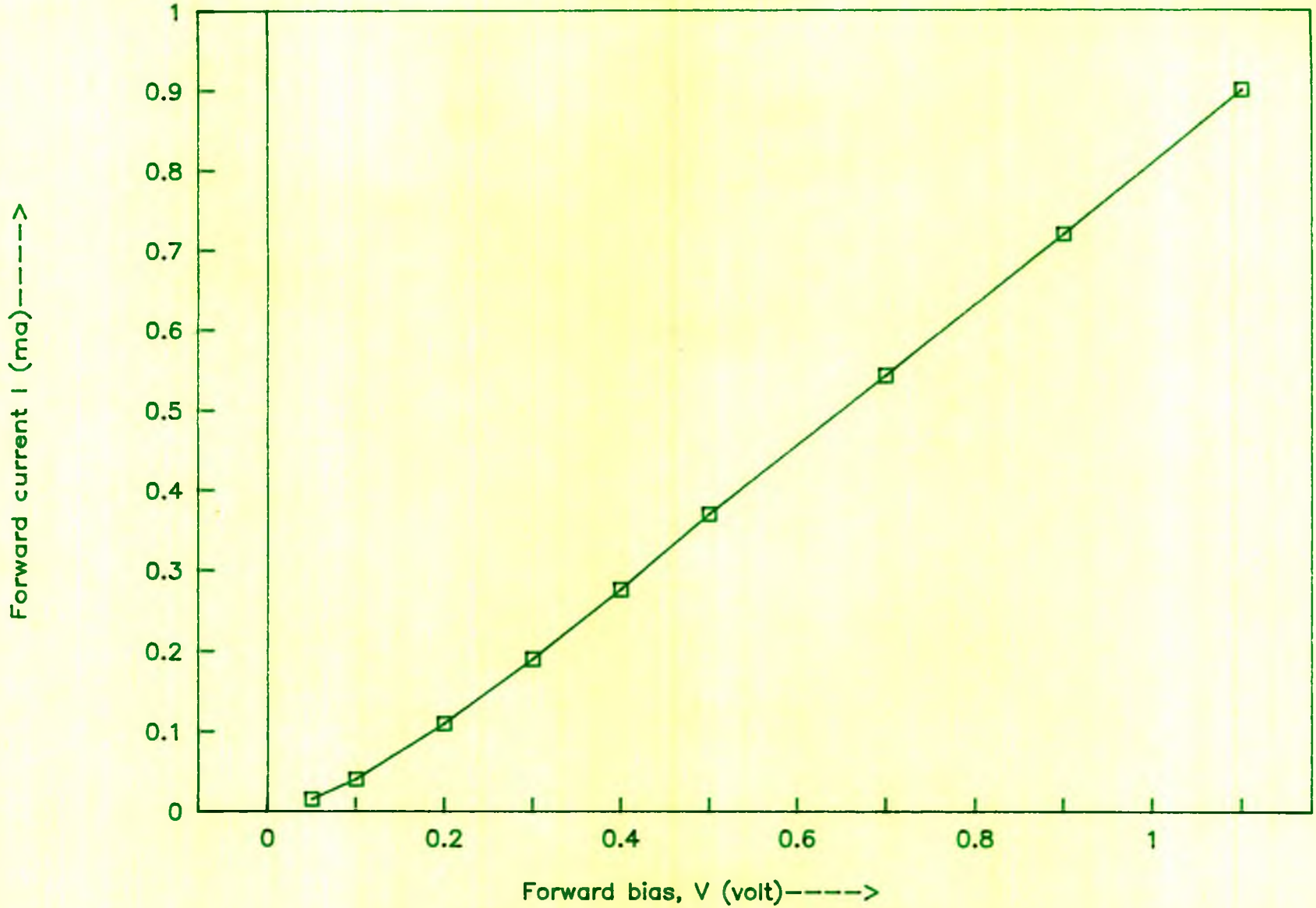
Sample: Ge 2SB56

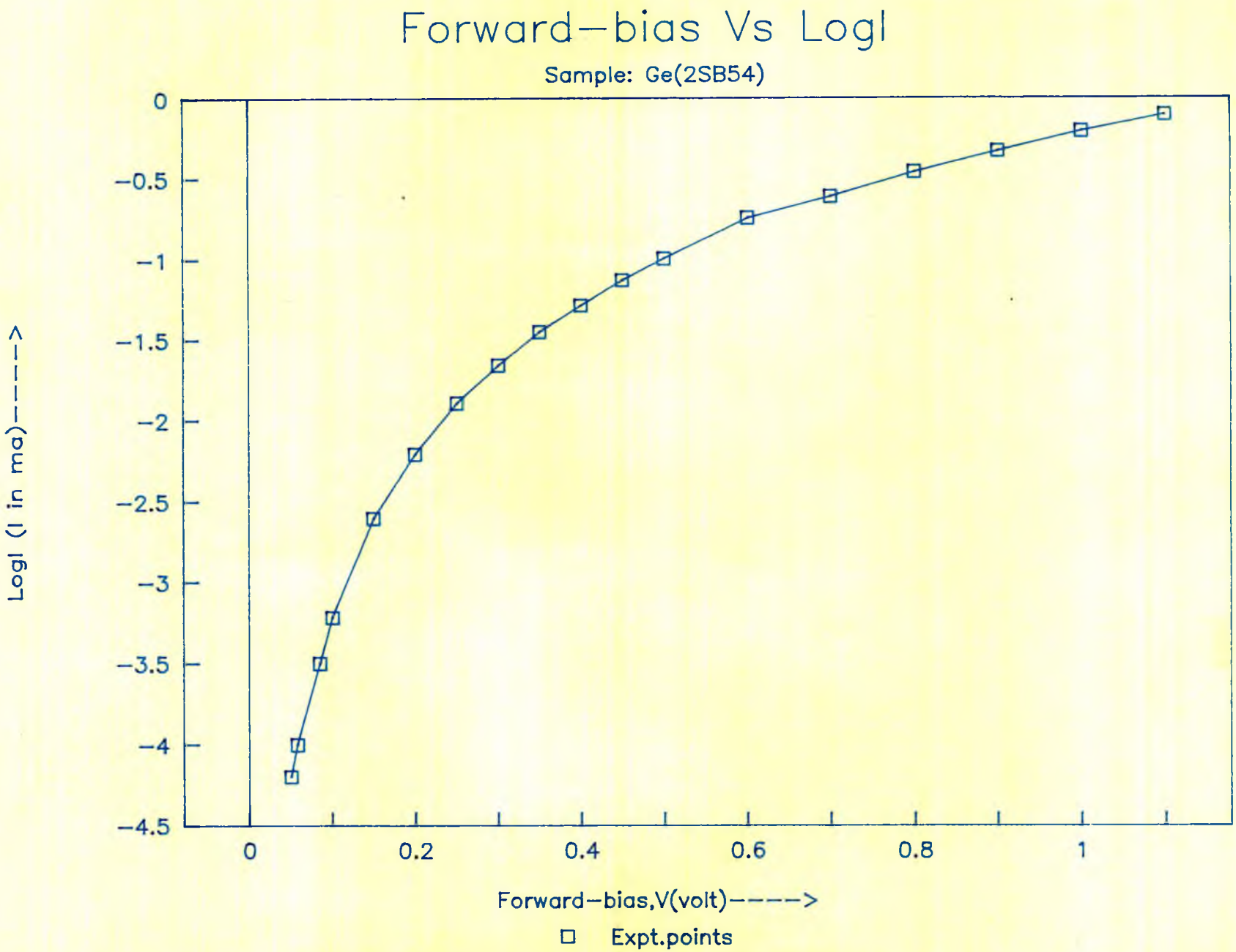


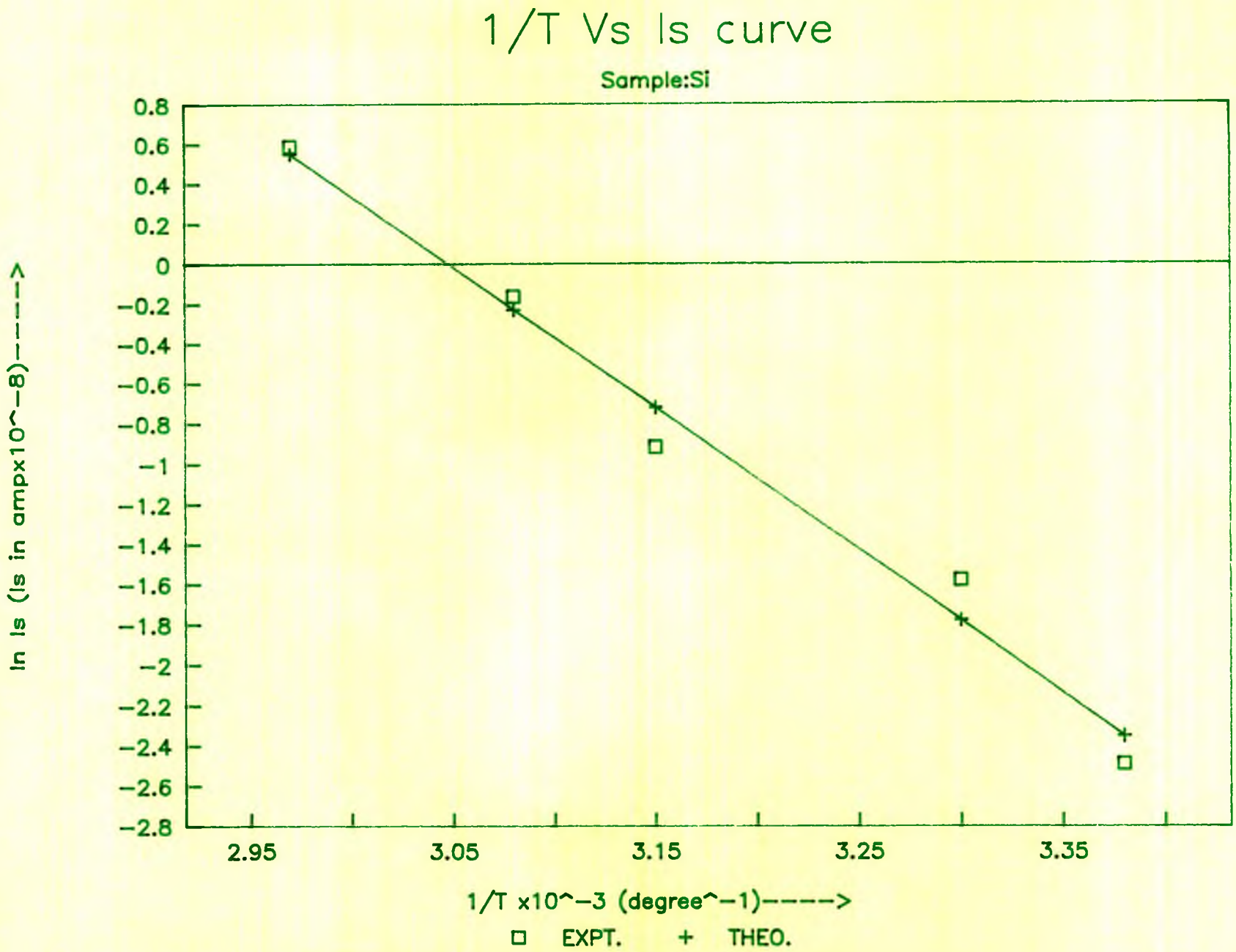

Forward–bias Vs log I
sample: Ge(2SB56)
log I(I in ma)
1
0
−1
−2
−3
−4
−5
0
0.2
0.4
0.6
0.8
1
1.2
Forward–bias,V(volt)–––––>
EXPT

Forward bias Vs forward current

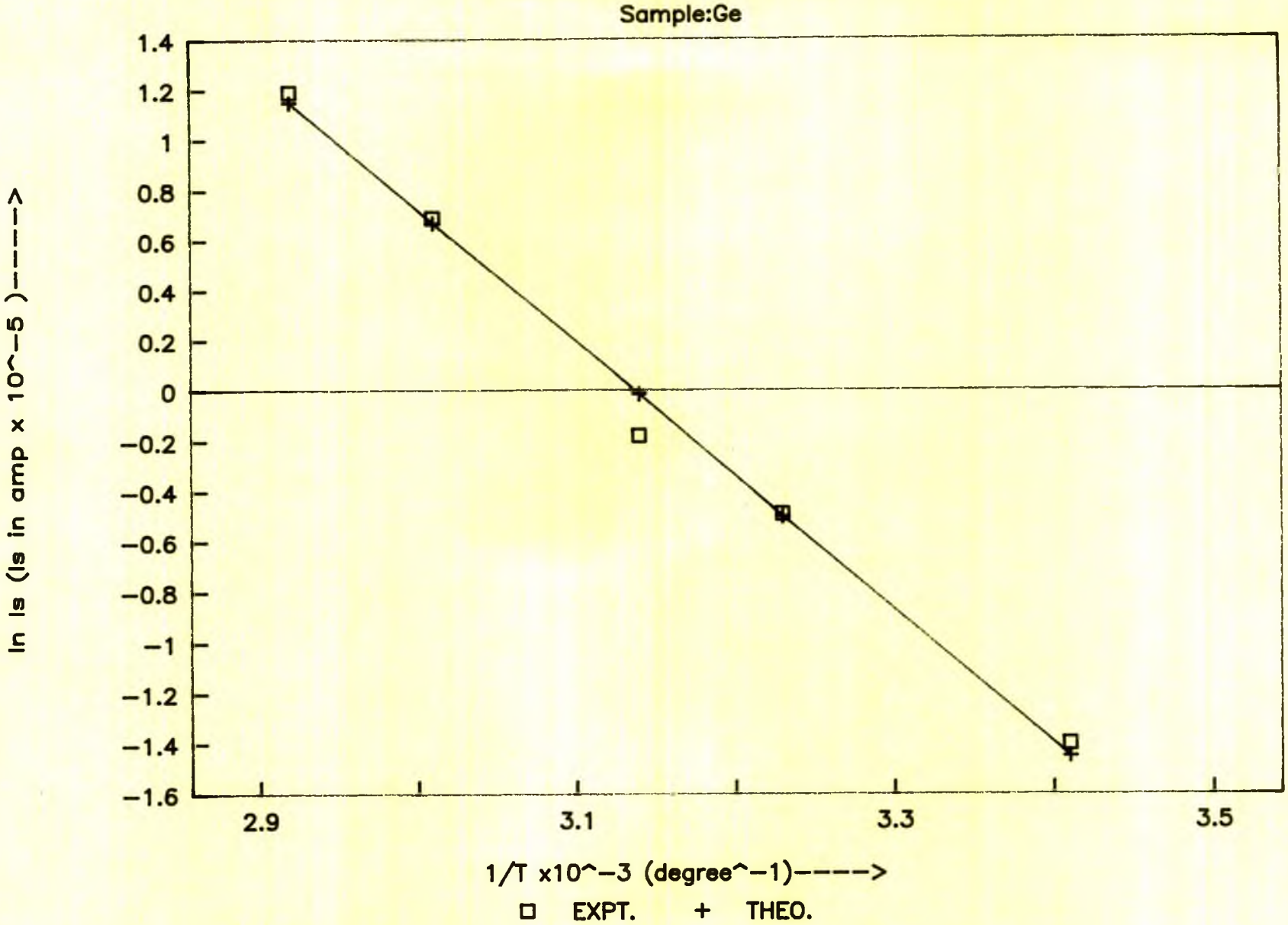
Sample: Ge 2SB54

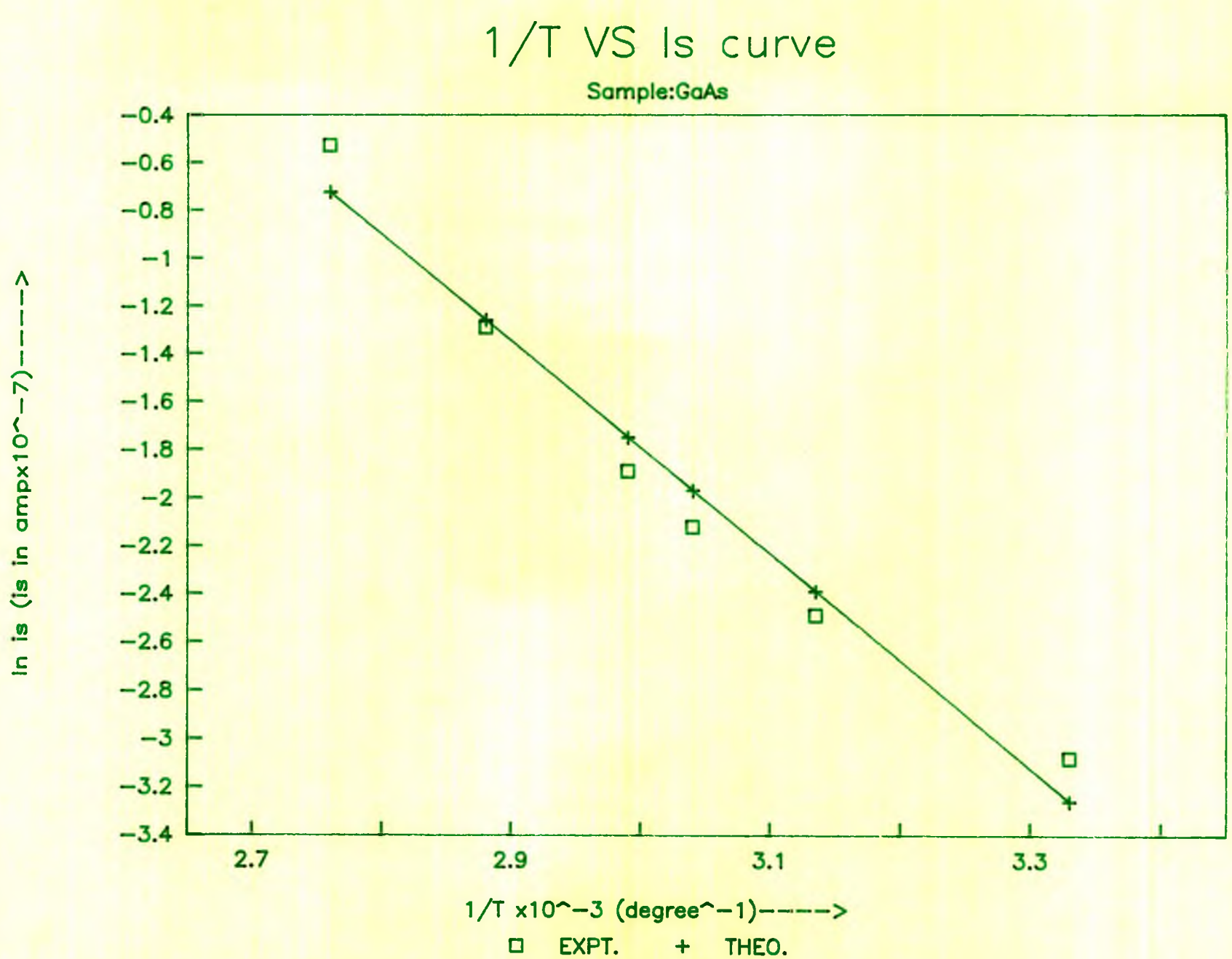



Forward–bias Vs LogI
Sample: Ge(2SB54)
0
−0.5
−1
−1.5
−2
−2.5
−3
−3.5
−4
−4.5
LogI (I in ma)——>
0
0.2
0.4
0.6
0.8
1
Forward–bias,V(volt)———>
Expt.points


1/T Vs Is curve
Sample:Si
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−1
−1.2
−1.4
−1.6
−1.8
−2
−2.2
−2.4
−2.6
−2.8
ln Is (Is in ampx10^−8)−−−−>
2.95
3.05
3.15
3.25
3.35
1/T x10^−3 (degree^−1)−−−−>
□ EXPT. + THEO.

1/T Vs ln Is curve




1/T VS Is curve
Sample:GaAs
-0.4
-0.6
-0.8
-1
-1.2
-1.4
-1.6
-1.8
-2
-2.2
-2.4
-2.6
-2.8
-3
-3.2
-3.4
ln is (is in ampx10^-7)----->
2.7
2.9
3.1
3.3
1/T x10^-3 (degree^-1)----->
EXPT.
THEO.

6.2 C-V MEASUREMENT:

C-V measurement of depletion layer forms an important study of our work. The importance of the study and volumes of information about the depletion region that can be extracted from have been thoroughly discussed in Chapter 2. Measuring technique and experimental details are given in Chapter-5. From C-V measurement we estimated intrinsic contact potential V_o, intrinsic capacitance C_o, dopping concentration etc. The summary of our study for various junctions is presented in Table-10.

TABLE - 8(a): C-V measurements (at room temperature)
Silicon Samples

Sample: Si-0103(1)

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-7}(pf^{-2})$
1	0.0	2204	2.059
2	0.05	2106	2.255
3	0.15	1938	2.663
4	0.3	1738	3.310
5	0.5	1560	4.109
6	0.8	1393	5.153
7	1.2	1245	6.452
8	1.6	1146	7.614
9	2.4	1023	9.555
10	3.2	940	11.317
11	4.0	875	13.061

Sample: Si-0103(2)

1	0.0	1945.0	2.643
2	0.1	1807.5	3.061
3	0.2	1690.0	3.501
4	0.4	1522.5	4.314
5	0.8	1322.5	5.718
6	1.2	1197.5	6.973
7	1.6	1115.0	8.045
8	2.4	990.0	10.203
9	3.2	917.5	11.879
10	4.0	857.5	13.600
11	5.0	797.5	15.721

TABLE - 8(a): C-V measurements (at room temperature)

Silicon Samples

Sample: Si-2N2369

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-2} (pf^{-2})$
1	0.0	4.35	5.285
2	0.4	3.87	6.677
3	0.8	3.62	7.613
4	1.4	3.36	8.858
5	1.8	3.22	9.645
6	2.4	3.09	10.473
7	2.8	3.01	11.037
8	3.2	2.95	11.491
9	4.0	2.83	12.486
10	4.4	2.77	13.033

Sample: Si-NTE50

Base-Emitter

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{5} (pf^{-2})$
1	0.0	111	8.12
2	0.05	108	8.57
3	0.1	105	9.07
4	0.2	101	9.80
5	0.3	97	10.63
6	0.5	91	12.08
7	0.75	85	13.84
8	1.0	80	15.63
9	1.25	76	17.31
10	1.5	72	19.29
11	2.0	68	22.96
12	2.5	62	26.01
13	3.0	58	29.73
14	3.5	55	33.06
15	4.0	52	36.98

TABLE - 8(a): C-V measurements (at room temperature)

Silicon Samples

Sample: Si-NTE50

Base-Collector

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^5$ (pf^{-2})
1	0.0	43.5	1.21
2	0.05	42.3	1.32
3	0.1	40.8	1.47
4	0.2	38.6	1.74
5	0.3	36.7	2.02
6	0.4	35.3	2.27
7	0.5	33.8	2.59
8	0.75	30.6	3.49
9	1.0	28.0	4.55
10	1.25	23.8	7.42
11	1.5	21.0	10.79
12	1.75	20.0	12.5
13	2.0	19.0	14.58
14	2.5	17.6	18.34
15	3.0	16.5	22.26
16	3.5	15.7	25.84
17	4.0	14.9	30.23

TABLE - 8(b): C-V measurements (at room temperature)

Sample: Germanium

Sample: Ge-110MP

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2}$ (pf^{-2})
1	0.0	2.23	0.201
2	0.025	1.89	0.279
3	0.05	1.67	0.359
4	0.1	1.37	0.533
5	0.2	0.97	1.06
6	0.3	0.8	1.56
7	0.4	0.7	2.04
8	0.5	0.63	2.51
9	0.75	0.53	3.56
10	1.0	0.48	4.34
11	1.25	0.43	5.41
12	1.5	0.4	6.25
13	2.0	0.37	7.30
14	2.5	0.34	8.65
15	3.0	0.32	9.77

Sample: Ge-2SB56

No. of obs.	Reverse bias V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-5} (pf^{-2})$
1	0.0	524	0.362
2	0.05	315	1.008
3	0.1	274	1.332
4	0.2	230	1.890
5	0.3	203	2.427
6	0.5	167	3.586
7	0.7	147	4.628
8	0.9	133	5.653
9	1.2	118	7.182
10	1.5	107	8.734
11	2.0	95	11.080
12	2.5	86	13.521

TABLE - 8(b): C-V measurements (at room temperature)

Sample: Germanium

Sample: Ge-7001 (PNP)

Base-Collector jtn

No. of obs.	Reverse bias V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-8}(pf^{-2})$
1	0.0	870	0.132
2	0.1	544	0.338
3	0.3	405	0.610
4	0.5	341	0.860
5	0.75	296	1.141
6	1.0	260	1.479
7	1.25	236	1.795
8	1.5	219	2.085
9	2.0	192	2.713
10	2.5	170	3.460
11	3.0	157	4.057
12	4.0	138	5.251

TABLE - 8(c) Data for C-V measurements: Samples: GaAs

Sample: GaAs-246(1)

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-5}(pf^{-2})$
1	0.0	242.33	1.70
2	0.1	291.00	1.91
3	0.4	201.33	2.47
4	0.8	175.33	3.25
5	1.2	157.00	4.06
6	1.6	144.67	4.78
7	2.0	134.33	5.54
8	2.8	119.00	7.06
9	3.6	108.67	8.49
10	4.5	99.67	10.07

Sample: GaAs-246(2)

1	0.0	256.00	1.53
2	0.1	244.33	1.68
3	0.4	212.33	2.22
4	0.8	185.33	2.91
5	1.2	165.00	3.63
6	1.6	152.00	4.33
7	2.0	140.67	5.05
8	2.8	125.00	6.40
9	3.6	114.67	7.61
10	4.5	105.00	9.07

TABLE - 8(c) Data for C-V measurements: Samples: GaAs

Sample: GaAs-246(3)

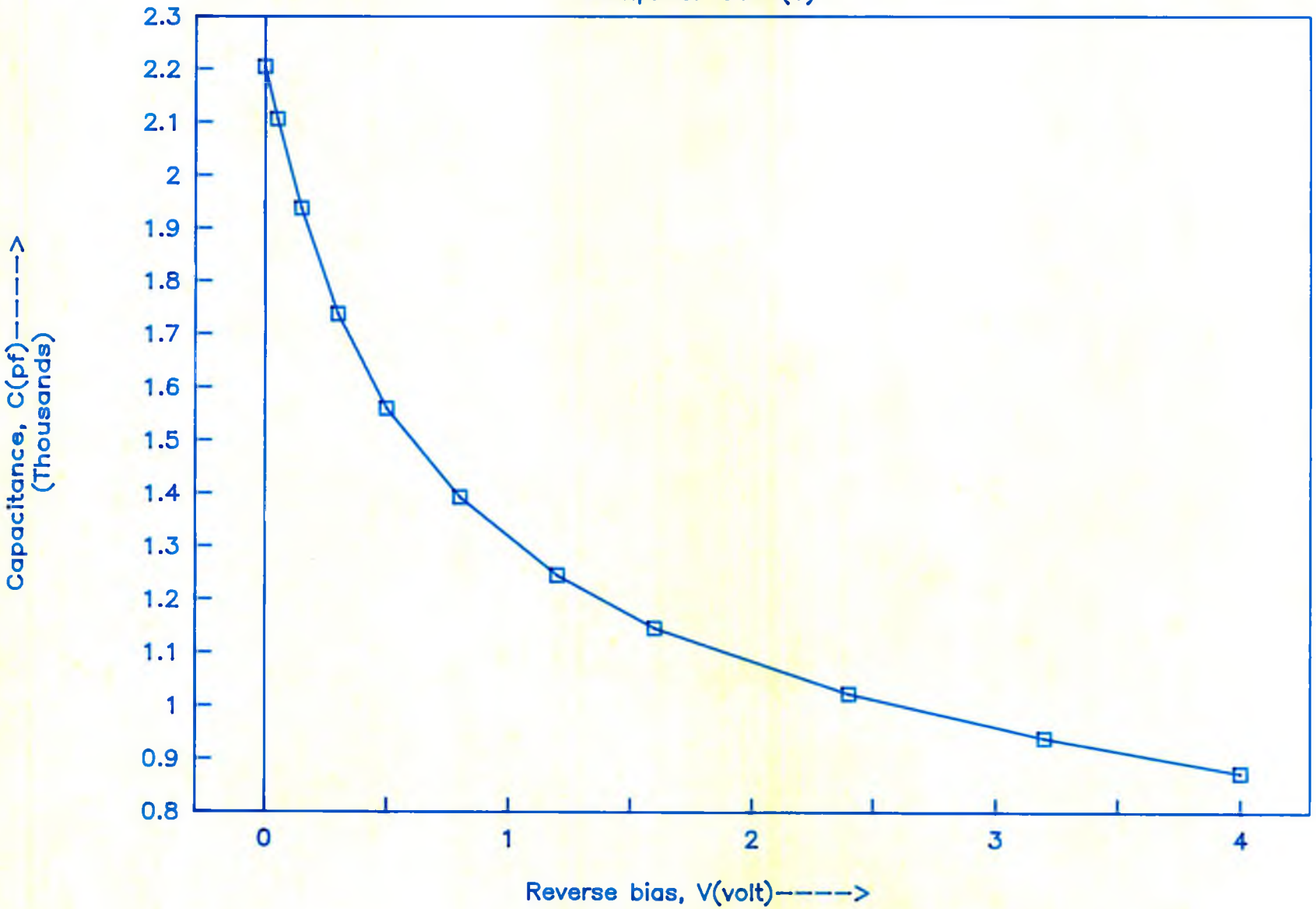
No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-5}(pf^{-2})$
1	0.0	230.00	1.89
2	0.1	217.00	2.12
3	0.4	189.67	2.78
4	0.8	165.00	3.67
5	1.2	149.00	4.50
6	1.6	130.33	5.89
7	2.0	126.33	6.27
8	2.8	113.00	7.83
9	3.6	102.67	9.49
10	4.5	94.67	11.16

Sample: GaAs-246(4)

No. of obs.	Reverse voltage V(volts)	Capacitance C(pf)	$\frac{1}{C^2} \times 10^{-5}(pf^{-2})$
1	0.0	285.00	1.23
2	0.2	260.00	1.48
3	0.4	235.33	1.81
4	0.8	205.33	2.37
5	1.2	185.00	2.92
6	1.6	168.00	3.54
7	2.0	156.00	4.11
8	2.8	138.33	5.23
9	3.6	126.00	6.30
10	4.5	116.00	7.43

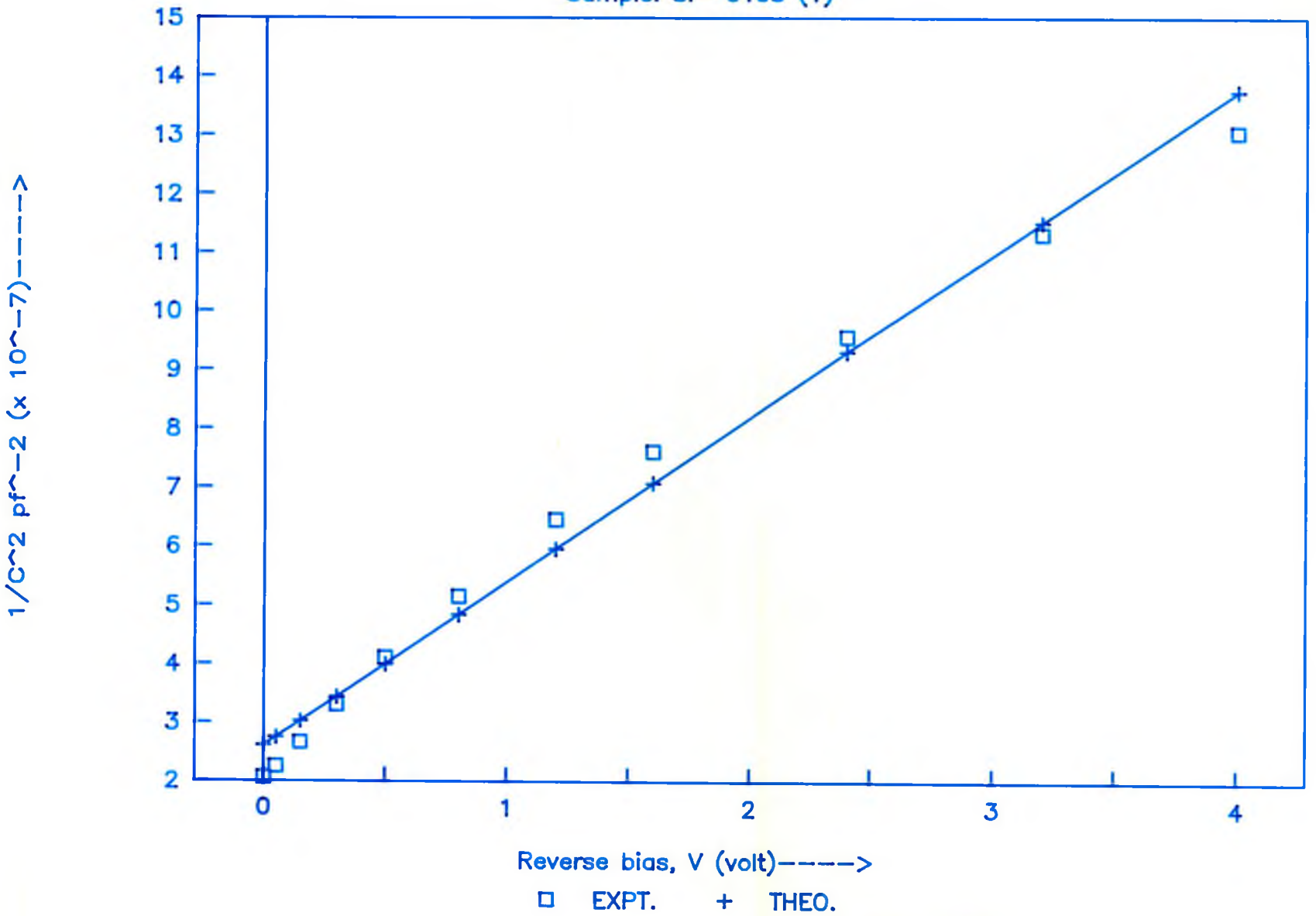
Reverse bias Vs capacitance

Sample:Si–0103(1)



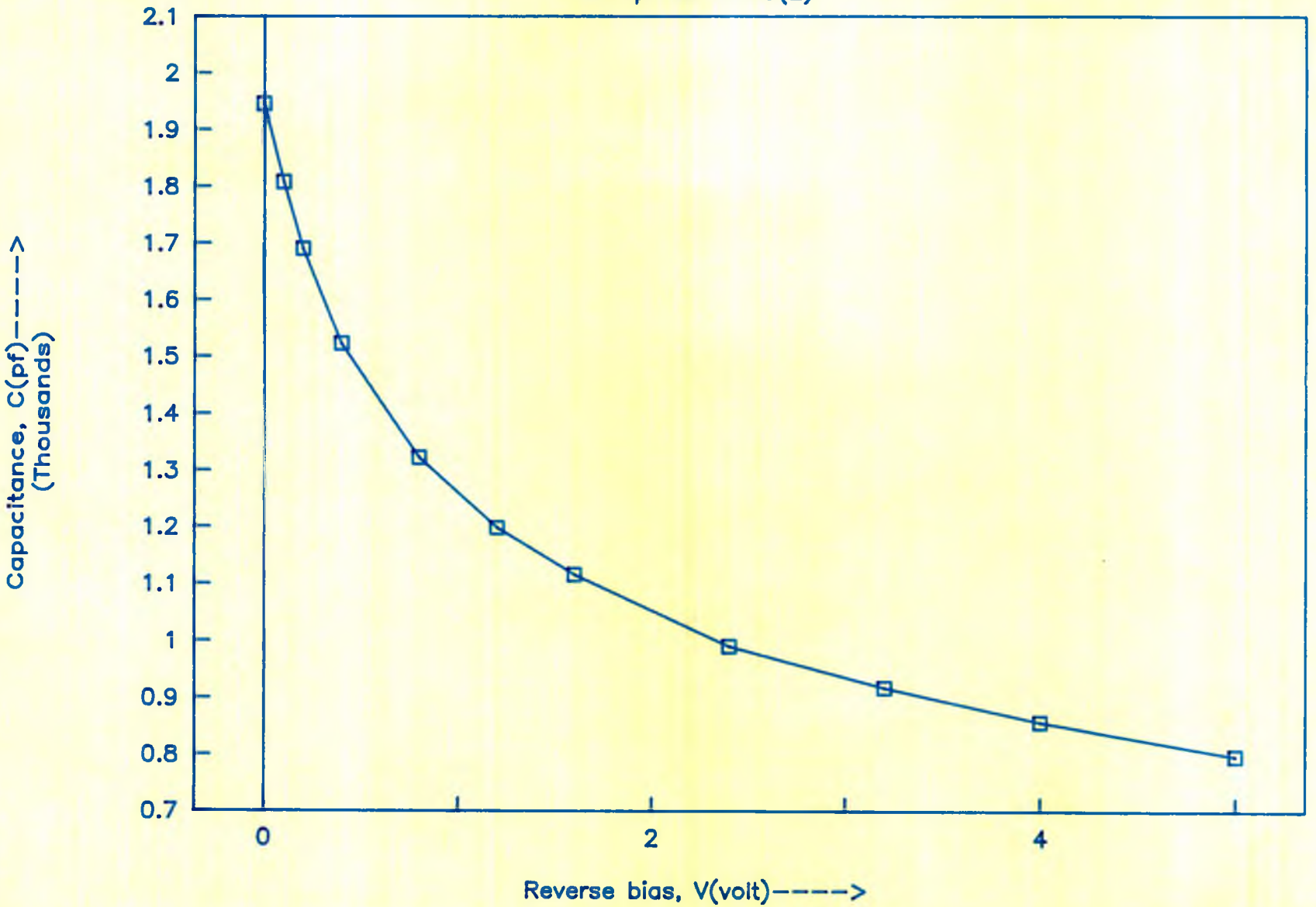
Reverse bias Vs 1/C^2 curve

Sample: Si– 0103 (1)

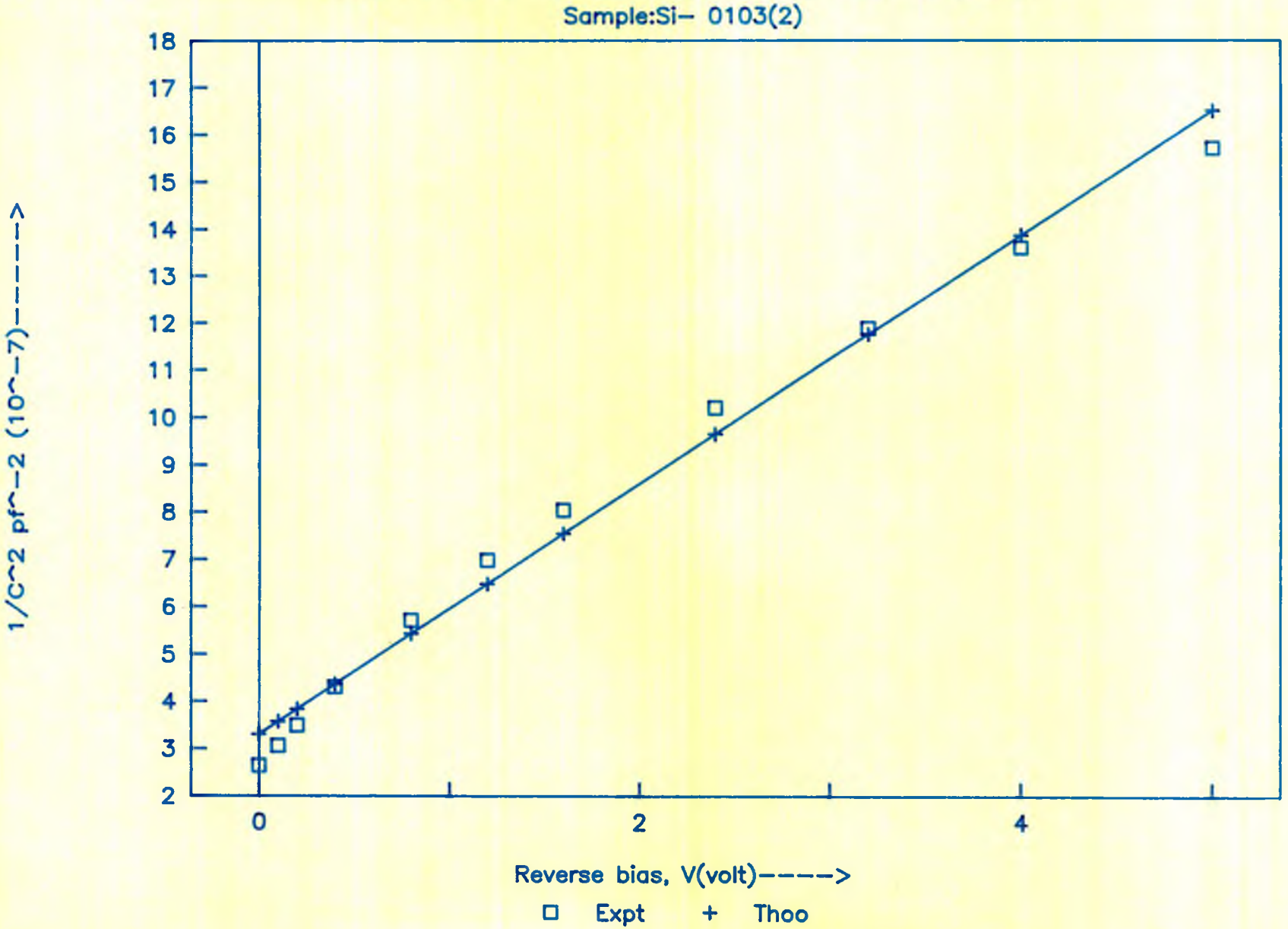


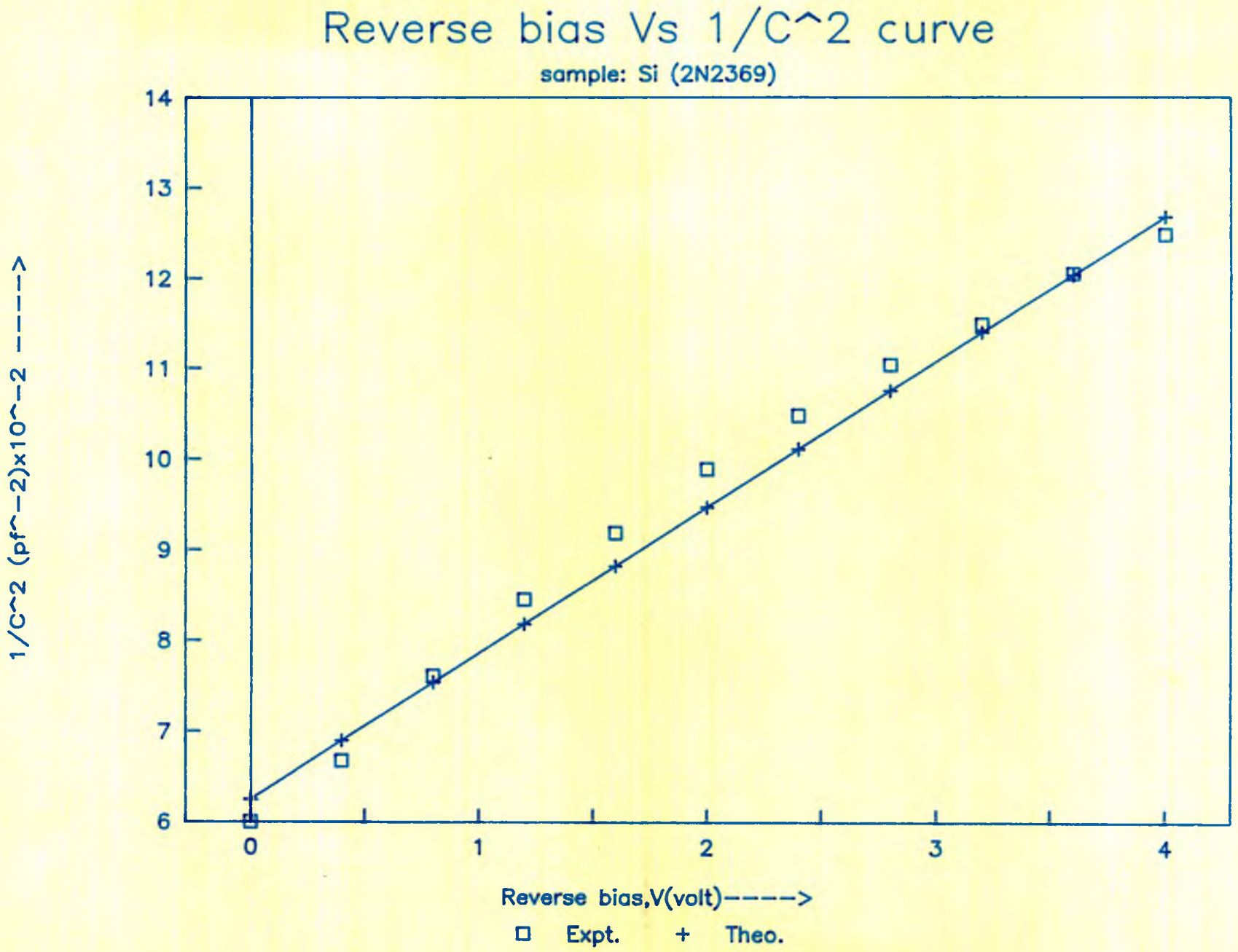
Reverse bias Vs capacitance

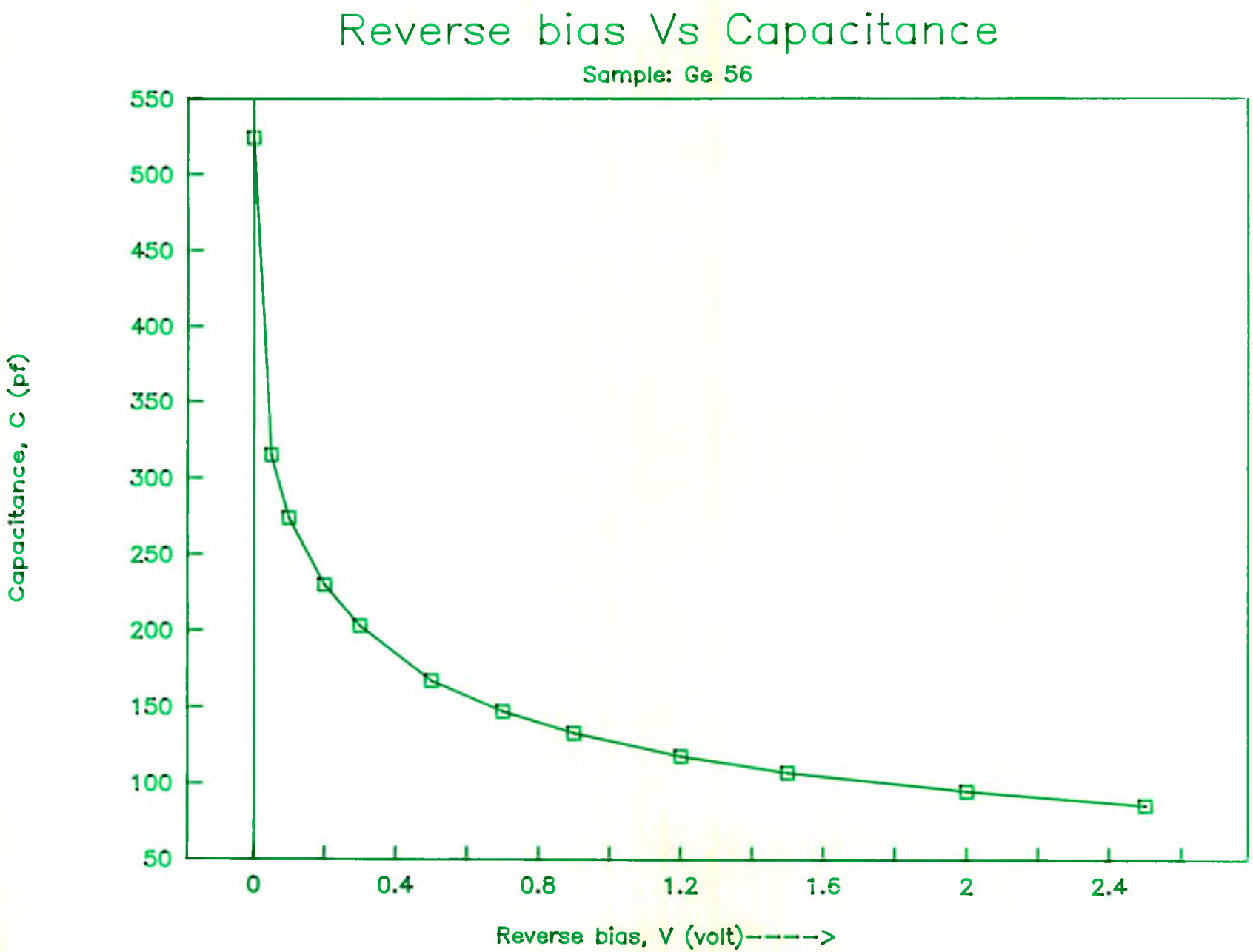
Sample:Si–0103(2)



Reverse bias Vs 1/C^2 curve

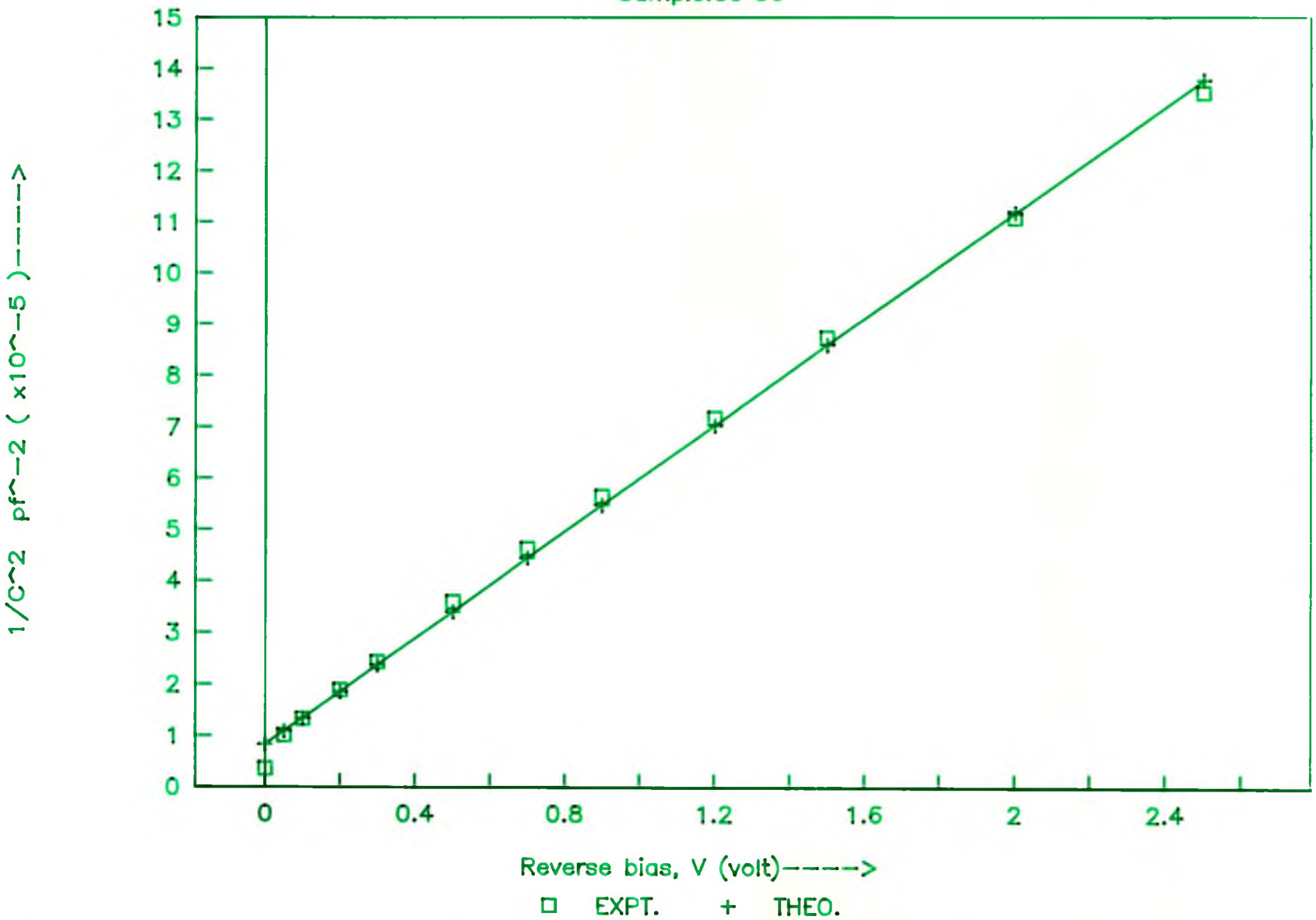



Reverse bias Vs 1/C^2 curve
sample: Si (2N2369)
1/C^2 (pf^-2)x10^-2 ----->
14
13
12
11
10
9
8
7
6
0
1
2
3
4
Reverse bias,V(volt)----->
Expt.
+
Theo.

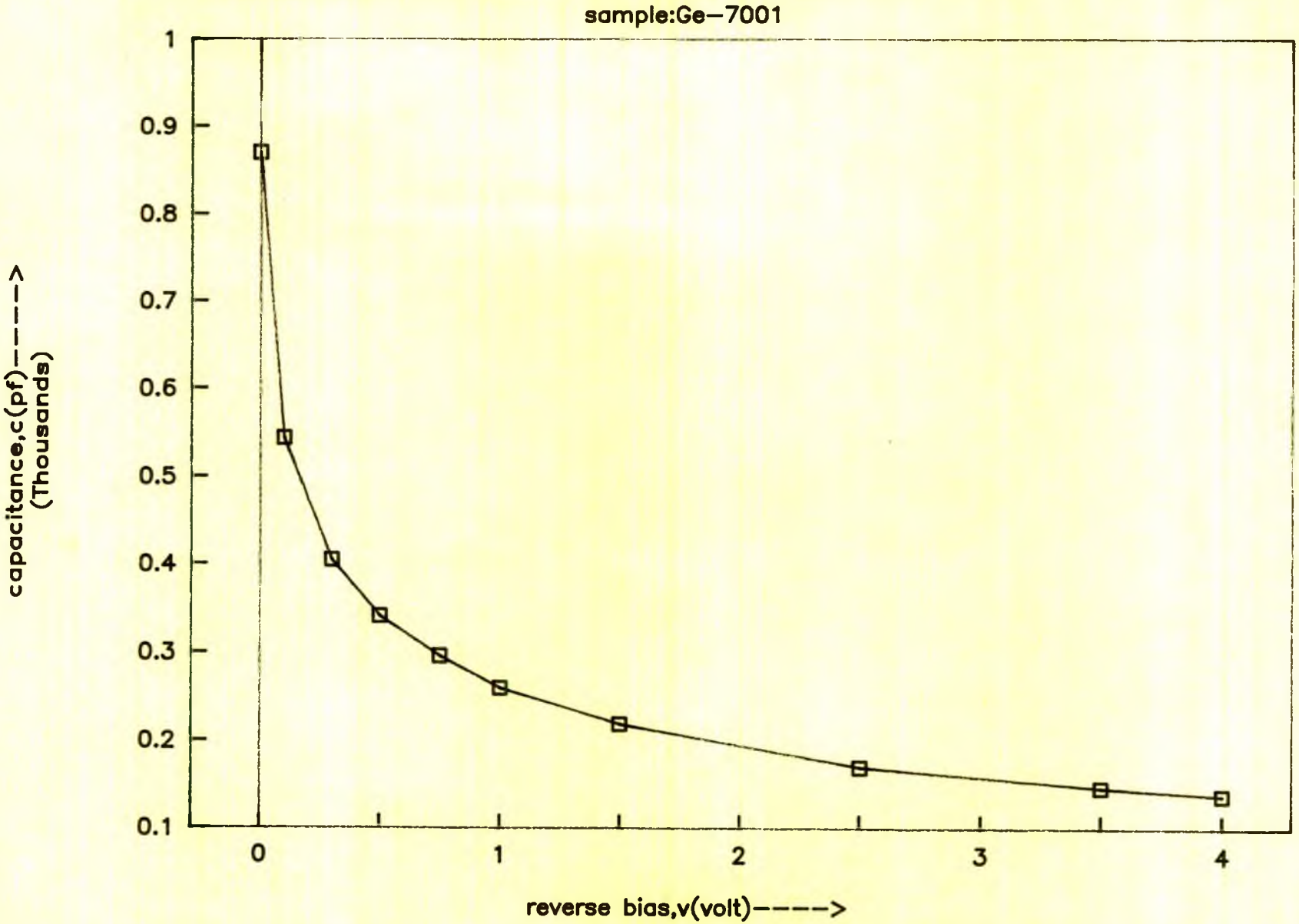

Reverse bias Vs Capacitance
Sample: Ge 56
Capacitance, C (pf)
550
500
450
400
350
300
250
200
150
100
50
0
0.4
0.8
1.2
1.6
2
2.4
Reverse bias, V (volt)----->
0
0.4
0.8
1.2
1.6
2
2.4

Reverse bias Vs 1/C^2 curve

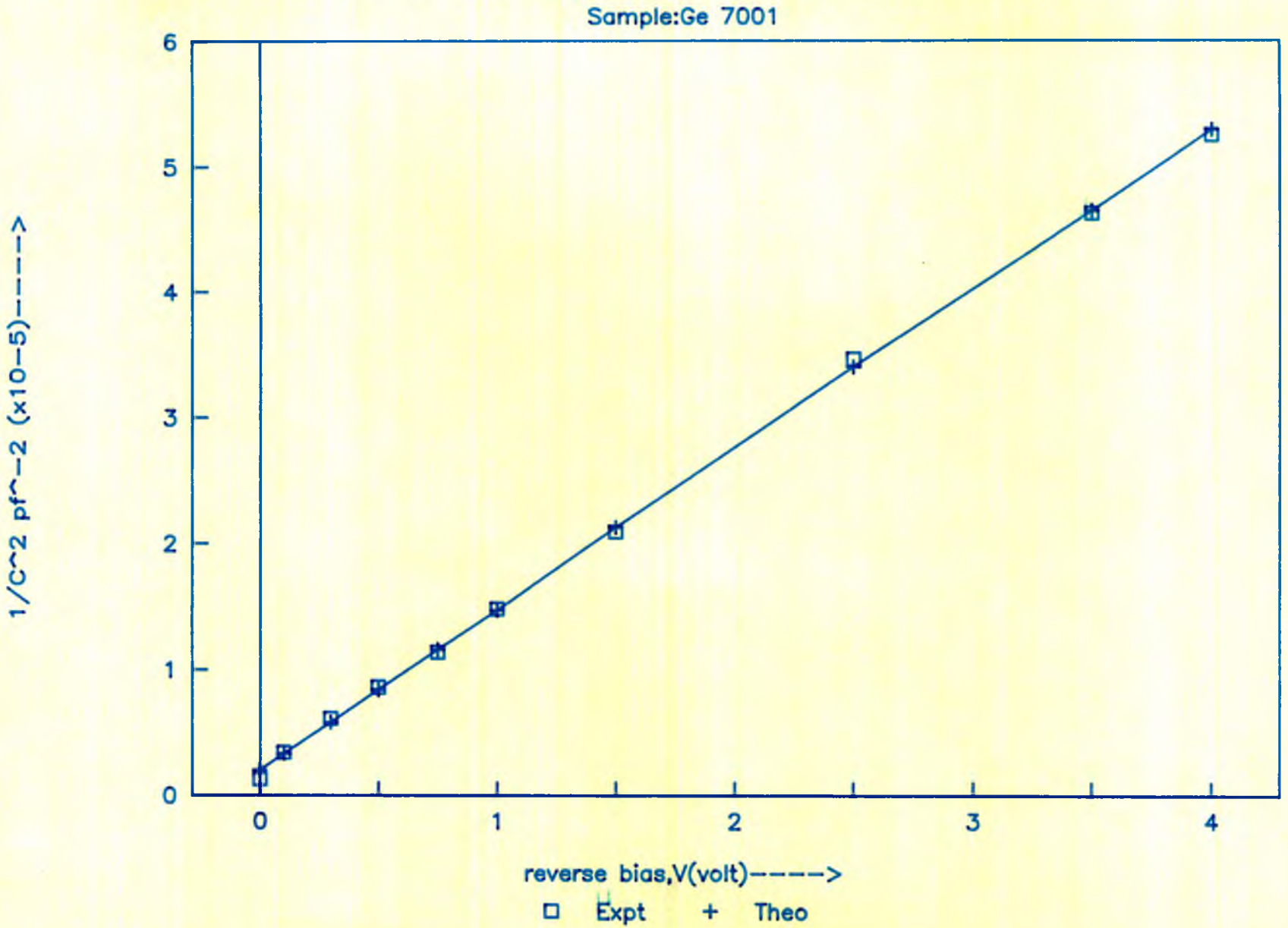
Sample:Ge 56

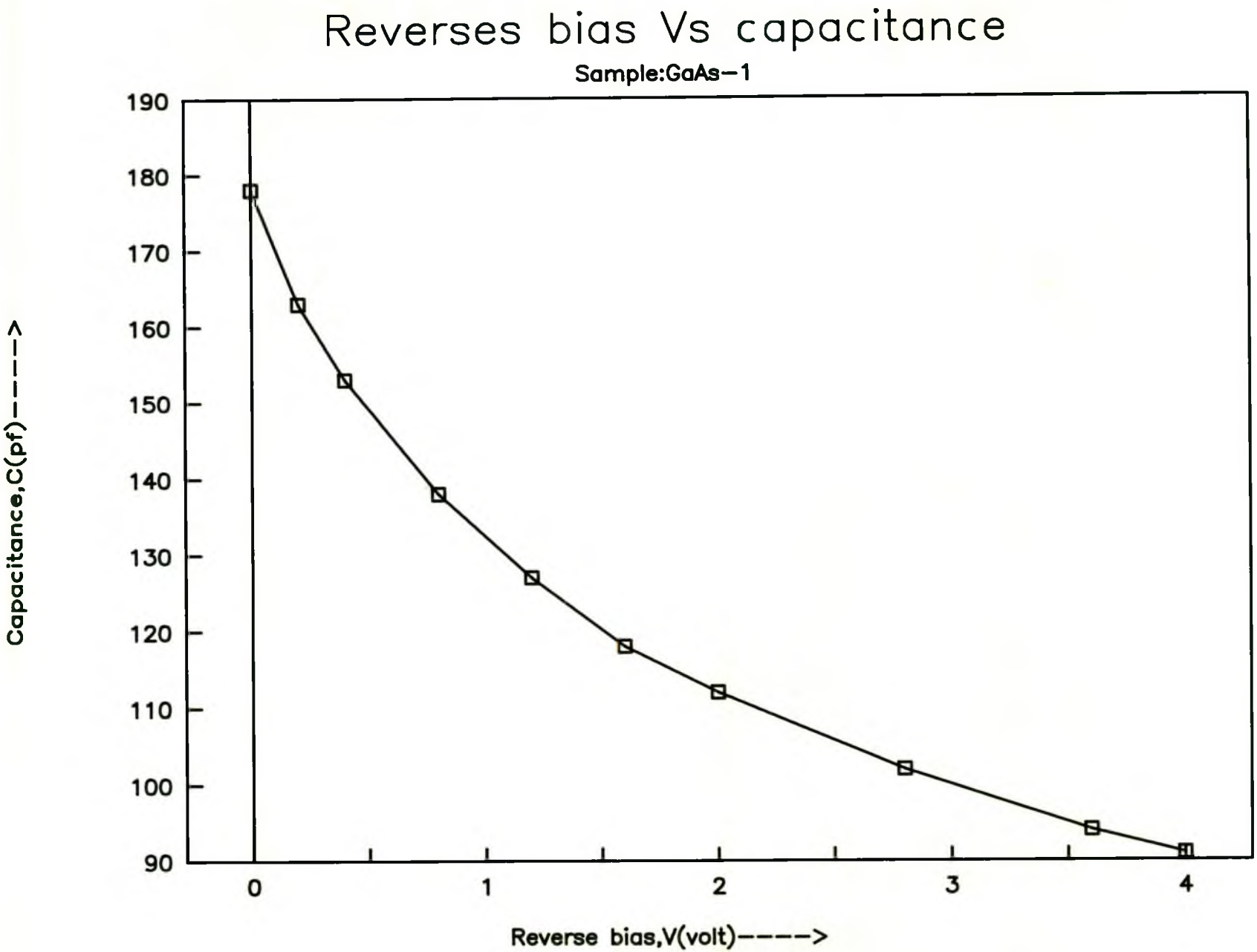


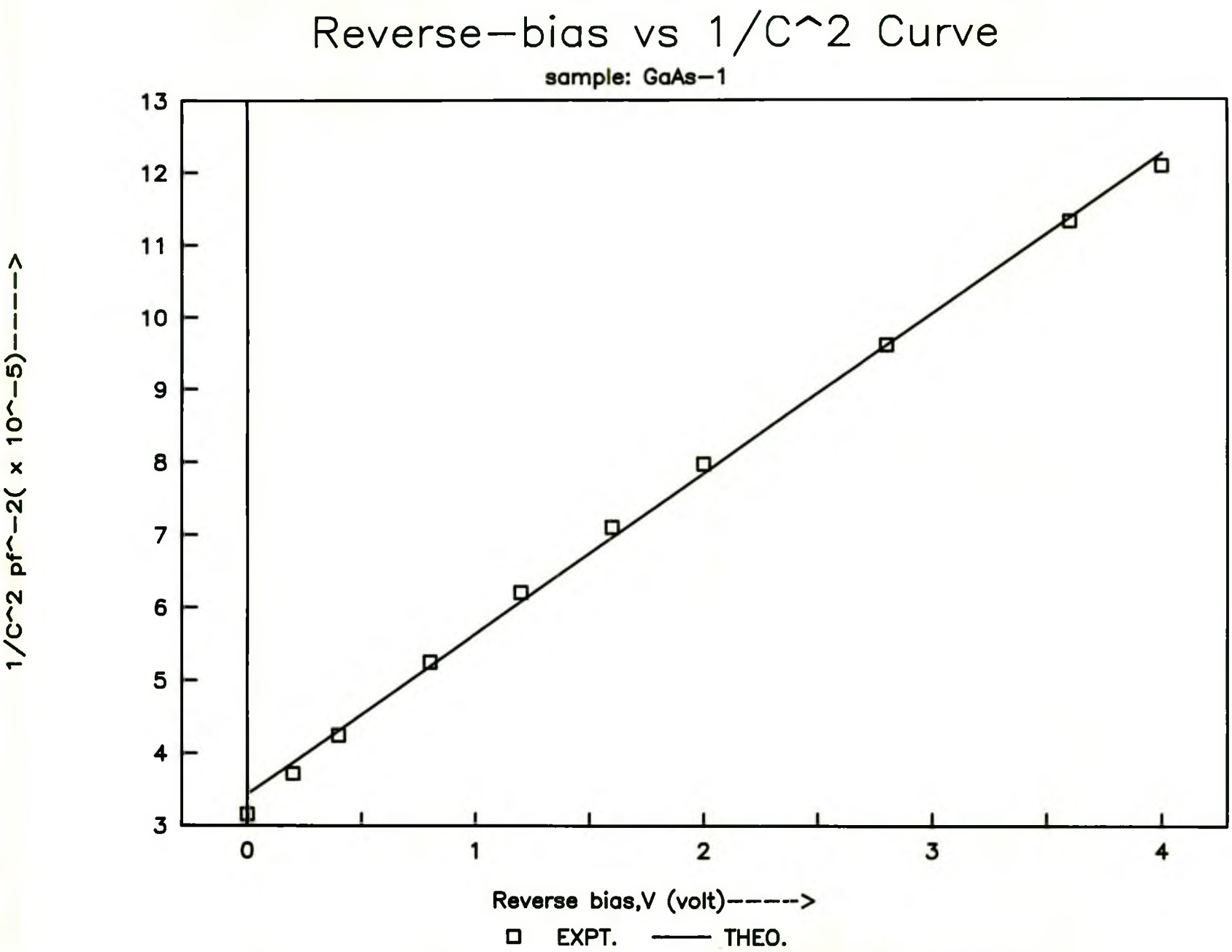
Reverse bias vs capacitance



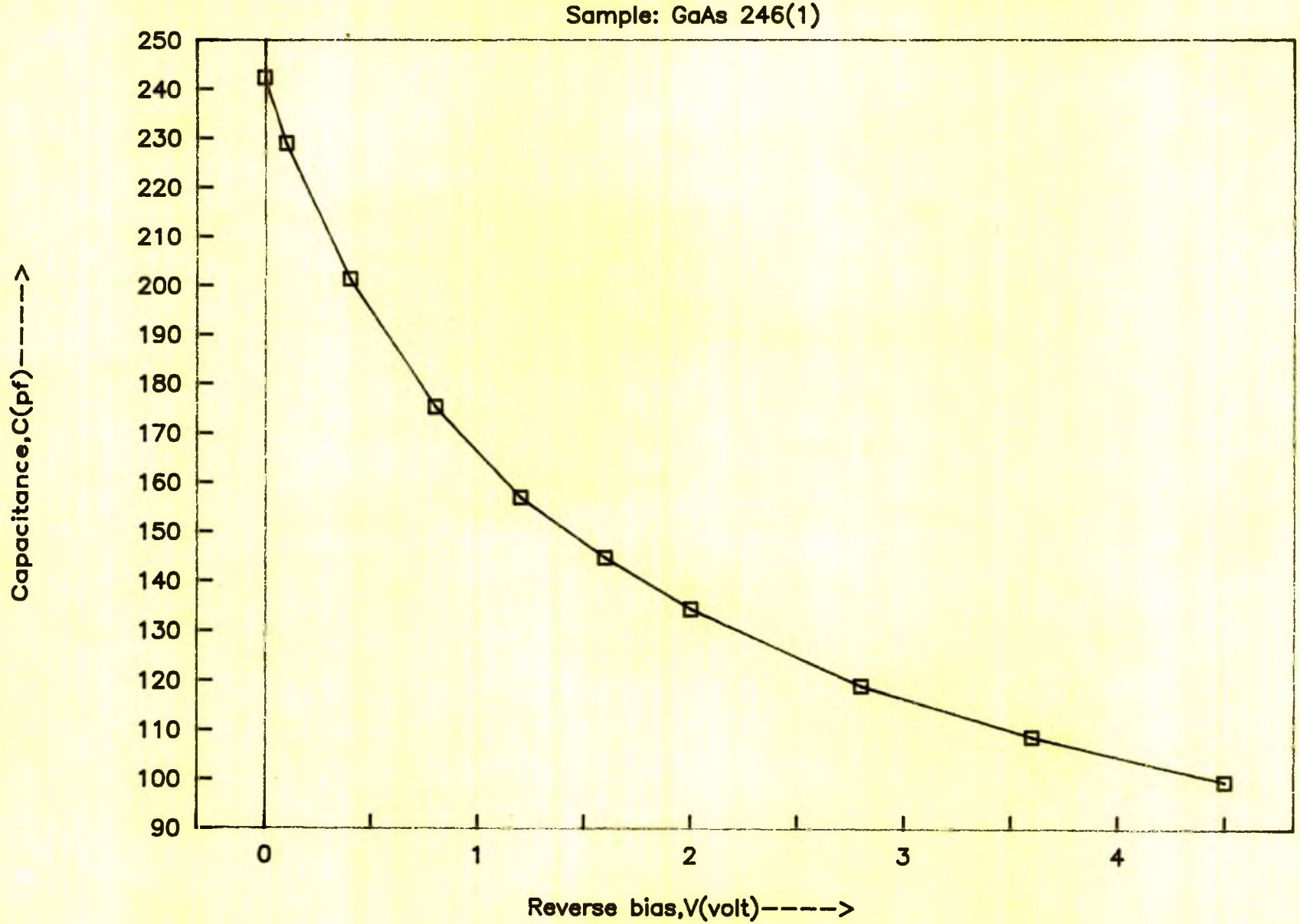
Reverse bias Vs 1/C^2 curve




Reverses bias Vs capacitance
Sample:GaAs–1
190
180
170
160
150
140
130
120
110
100
90
0
1
2
3
4
Capacitance,C(pf)----->
Reverse bias,V(volt)----->
0
1
2
3
4


Reverse–bias vs 1/C^2 Curve
sample: GaAs–1
1/C^2 pf^–2(x 10^–5)----->
13
12
11
10
9
8
7
6
5
4
3
0
1
2
3
4
Reverse bias,V (volt)----->
EXPT.
THEO.

Reverse bias Vs Capacitance



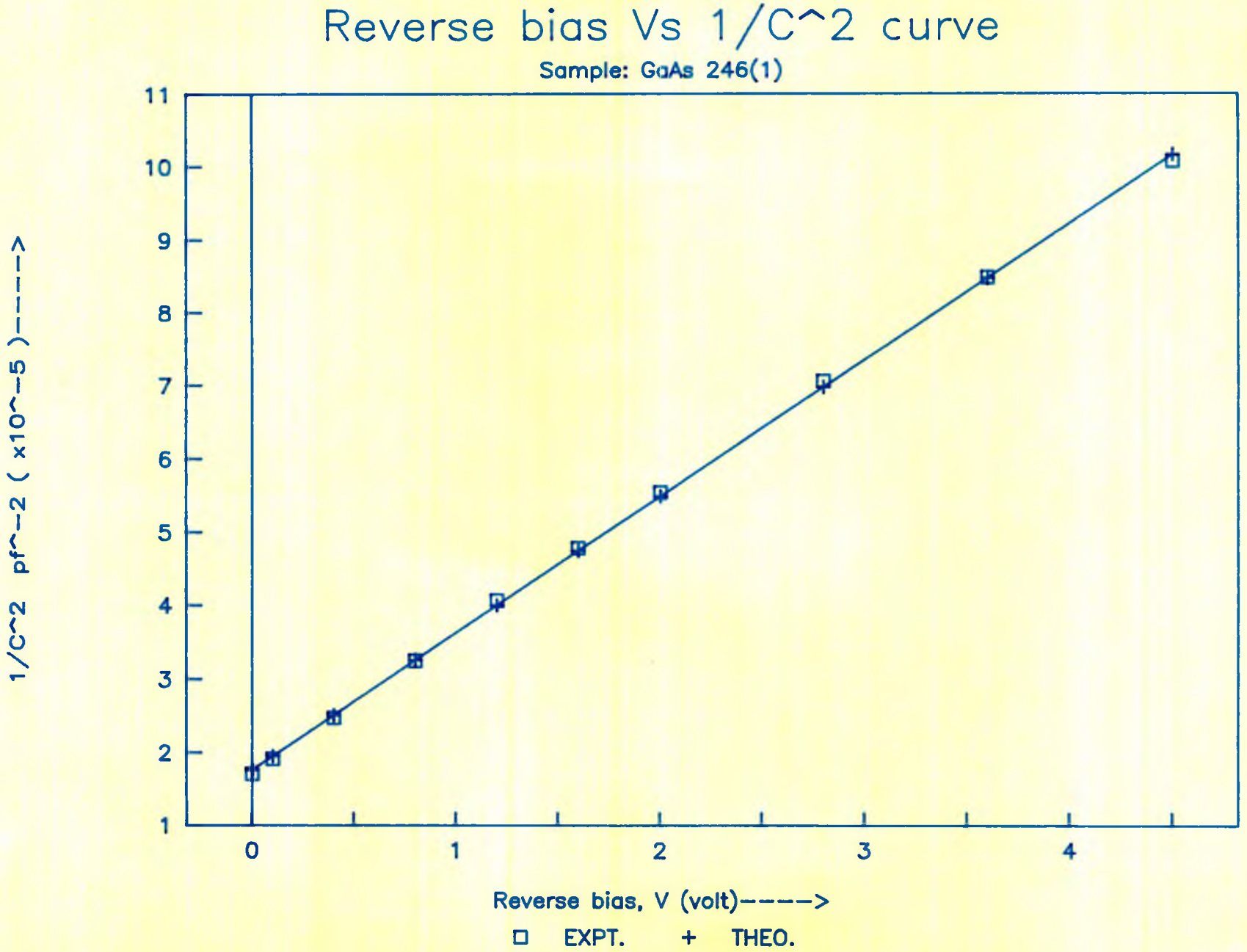

Reverse bias Vs 1/C^2 curve
Sample: GaAs 246(1)
1/C^2 pf^-2 (x10^-5)----->
11
10
9
8
7
6
5
4
3
2
1
0
1
2
3
4
Reverse bias, V (volt)----->
EXPT.
+ THEO.

TABLE : 9 RESULTS OF I-V MEASUREMENTS

SAMPLE AND TYPE NUMBER	PARAMETERS ESTIMATED				
	OFFSET VOLTAGE V_r (volts)	FORWARD RESISTANCE R_f (OHMS)	SATURATION CURRENT I. at R.T(μA)	EFFICIENCY FACTOR, η	
				FROM FORWARD CURRENT	FROM REVERSE CURRENT
Si-0103(1)	0.65	1.79	0.01	2.99	--
Si-0103(2)	0.38	1.14	0.087	2.72	--
Si-2N2369	0.62	1.06	0.002	2.62	--
Si-NTE50(PNP) (B-E jn)	0.53	1.20	0.007	2.51	1.78
Si-NTE50(PNP) (B-C Jn)	0.45	1.49	0.333	4.18	2.13
Ge-110MP	0.12	1.33	2.500	2.35	1.55
Ge-2SB56(pnp) BC Jn	0.18	1.18	3.97	1.93	--
Ge-2SB54 (pnp) BC Jn	0.09	1.11	5.72	1.97	--
GaAs-246(1)	0.61	1.26	0.0044	2.18	1.49
GaAs-246(2)	0.58	1.68	0.0020	2.46	2.14
GaAs-246(3)	0.61	1.28	0.0018	1.72	--
GaAs-246(4)	0.60	1.27	0.0018	2.55	--
Schottky diode (n-Si)	0.25	1.08	0.2965	3.22	--

TABLE : 10 RESULT OF C-V MEASUREMENT

SAMPLE WITH TYPE	ESTIMATED PARAMETERS						
	Contact potential, V_0 (volt)	Na.Nd (product of acceptor and donor concentration. $(cm)^{-6}$	N^+ (doping concentration on highly doped side) (cm^{-3})	Junction width, W_0 (μm)	Junction capacitance, C_0 (pf)	Junction capacitance/area c_0 (pf/cm^2)	Effective area of the junction cm^2
Si-0103(1)	0.94	1.28×10^{36}	8.81×10^{19}	0.2904	1957.94	3.60×10^{4}	.0544
Si-0103(2)	1.25	2.96×10^{41}	8.21×10^{19}	6.75	1736.83	1.55×10^{7}	1.12×10^{-4}
Si-2N2369 npn (BC-Jn.)	3.49	--	--	--	4.0	--	--
Si-NTE50(PNP) (BE-Jn)	1.18	1.51×10^{39}	6.05×10^{21}	0.0785	109.12	1.33×10^{5}	8.20×10^{-4}
Si-NTE50(PNP) (BC-Jn)	0.44	--	--	--	46.60	--	--
Si-NTE500(npn) (BC-Jn)	1.07	--	--	--	62.36	--	--
Ge-7001(pnp) (BC-Jn)	0.16	2.73×10^{29}	6.65×10^{18}	83.01	702.06	1.70×10^{2}	4.11
Ge-2SB56 (pnp) BC Jn	0.16	2.81×10^{29}	6.68×10^{18}	82.21	347.30	1.72×10^{2}	2.01
Ge-2SB54 (pnp) BC Jn	3.04	--	--	--	262.48	--	--
Ge-110MP(1)	0.17	5.22×10^{29}	6.88×10^{18}	64.11	1.31	2.21×10^{2}	5.91×10^{-3}
Ge-110MP(2)	0.12	--	--	--	1.41	--	--
Ge-110MP(3)	0.17	--	--	--	1.40	--	--

Contd.

TABLE :10 RESULT OF C-V MEASUREMENT (Contd. from previous page)

SAMPLE WITH TYPE	ESTIMATED PARAMETERS						
	Contact potential, V_0 (volt)	Na.Nd (product of acceptor and donor concentration. $(cm)^{-6}$	N^+ (doping concentration on highly doped side) (cm^{-3})	Junction width, W_0 (μm)	Junction capacitance, C_0 (pf)	Junction capacitance/area C_0 (pf/cm^2)	Effective area of the junction cm^2
GaAs 246(1)	0.95	8.62×10^{29}	1.13×10^{21}	1.772×10^{2}	238.15	65.97	3.61
GaAs 246(2)	0.94	6.65×10^{29}	2.66×10^{19}	2.342×10^{2}	251.31	49.90	
GaAs 246(3)	0.98	3.65×10^{29}	1.66×10^{19}	0.81×10^{2}	222.01	144.67	1.53
GaAs 246(4)	0.96	2.80×10^{29}	2.50×10^{19}	3.442×10^{2}	280.92	33.95	
GaAs 246(5)	0.96	1.33×10^{30}	2.02×10^{19}	1.457×10^{2}	224.83	80.19	2.80
GaAs 246(6)	0.96	1.27×10^{30}	2.45×10^{19}	1.638×10^{2}	249.32	71.33	3.50
GaAs (ASEA)-1	1.55	1.34×10^{40}	2.99×10^{20}	7.101×10^{-3}	170.80	1.64×10^{6}	1.04×10^{-4}
GaAs (ASEA)-2	1.54	8.40×10^{39}	2.71×10^{20}	8.52×10^{-3}	192.99	1.372×10^{6}	1.41×10^{-4}

TABLE : 11 RESULTS OF TSCAP MEASUREMENT

System/Devices	No. of trap levels found	Ionization energy of trap levels, ev		Trap concentration cm^{-3}	Doping concentration cm^{-3}
Si-0103(1) (p^+n jn)	10		0.19	1.40×10^{15}	---
			0.29	---	---
		ELEC.	0.40	2.57×10^{15}	---
		TRAP	0.50	1.92×10^{15}	1.45×10^{6}
			0.62	---	---
			0.68	---	---
			0.46	---	---
		HOLE	0.56	1.72×10^{15}	---
		TRAP	0.67	---	---
			0.71	---	---
Si-0103(2) (p^+n jn)	2	ELEC.	0.749	---	---
		TRAP	0.750	---	---
Si-2N2369 (npn-tranistor) BC jn, n^+p	5			N_T/N_d	
		ELEC.	0.746	0.0149	---
		TRAP	0.792	0.0100	---
		HOLE	0.741	0.0080	---
		TRAP	0.747	0.2367	---
			0.771	0.0516	---
Ge-7001 (pnp-transistor) BC jn, p^+n	2	ELEC.	0.14	5.35×10^{8}	4.1×10^{10}
		TRAP	0.426	8.62×10^{8}	
Ge-2SB56 (pnp-transistor) BC jn, p^+n	3	ELEC.	0.13	1.38×10^{9}	
		TRAP	0.43	3.57×10^{8}	4.2×10^{10}
		HOLE	0.47	2.72×10^{8}	
GaAs (ASEA-2)	2	TRAP	0.44 0.76		

TABLE: 12 RESULTS OF TSC MEASUREMENTS

SYSTEM/DEVICES	NO. OF TRAP LEVELS FOUND	IONIZATION ENERGY OF TRAP LEVELS, ev	TYE OF TRAPS
Si-0103(1) p^+n jn	5	.1852 .7796 .8085 .8234 .2927	Electron trap Hole trap
Si-0103(2) p^+n jn	9	.682 .704 .715 .737 .740 .746 .749 .752 .754	Electron trap
Si-2N2369 (npn-transistor) BC jn, n^+p	13	.756 .758 .759 .762 .764 .765 .769 .8426 .8447 .8454 .8459 .8462 .8466	Hole trap
Ge-2SB56 (pnp-transistor) BC jn, p^+n	3	.4920 .4927 .4945	Electron trap
Ge-2SB54 (pnp-transistor) BC jn, p^+n	6	.4617 .4623 .4637 .4642 .4866 .4882	Electron trap

6.3. TSCAP Measurement:

Theory underlying TSCAP measurement and its importance in defect state study has been developed and discussed in chapter-4, and chapter 5 gives the experimental details.We note that, from such measurement, we can detect the presence of defect states and characterize a state i.e estimate its activation energy (ΔE_i) and trap concentration N_T. In an actual experiment capacitance steps are recorded as the temperature of the sample is allowed to rise steadily. Although, ideally it is derivable that from the plot of $\ln\left[T_m^2 / \beta\right]$ against $\frac{1}{Tm}$, we should estimate ΔE_i from the slope of the curve ($\Delta E_i/k$). But since it is difficult to keep the heating rate β steady and uniform, we refrain from doing so. Instead we took the generally widely accepted value of 'attempt to escape frequency' parameter A in the emission rate equation e_n. The accepted value is $A \simeq 10^{12}$. Then marking maximum slope point (T_m) at the observed capacitance step and using Eq. 4.67 i.e.

$$\frac{\Delta E_i}{kT_m} = \ln\left[\frac{AkT_m^2}{\beta(\Delta E_i + 2kT_m)}\right]$$

we estimated activation energy (ΔE_i) of the defect state level in question. Concentration of an observed defect state has been estimated from the formula given by Eq 4.17b or Eq.4.19a (for approximate value). The result of observation is shown in the Table-11. A few typical TSCAP-spectrum for some devices are presented here for illustration.

6.3.1 TSC measurement:

TSC measurement is identical to TSCAP and is complementary rather the competitive. The theory underling such measurement has been presented in chapter-4. We stated there that from the observed TSC peak we can evaluate activation energy ΔE_i from peak temperature (T_m) using a similar equation as used in TSCAP technique. Results are presented in Table-12.

6.3.2 DLTS measurement:

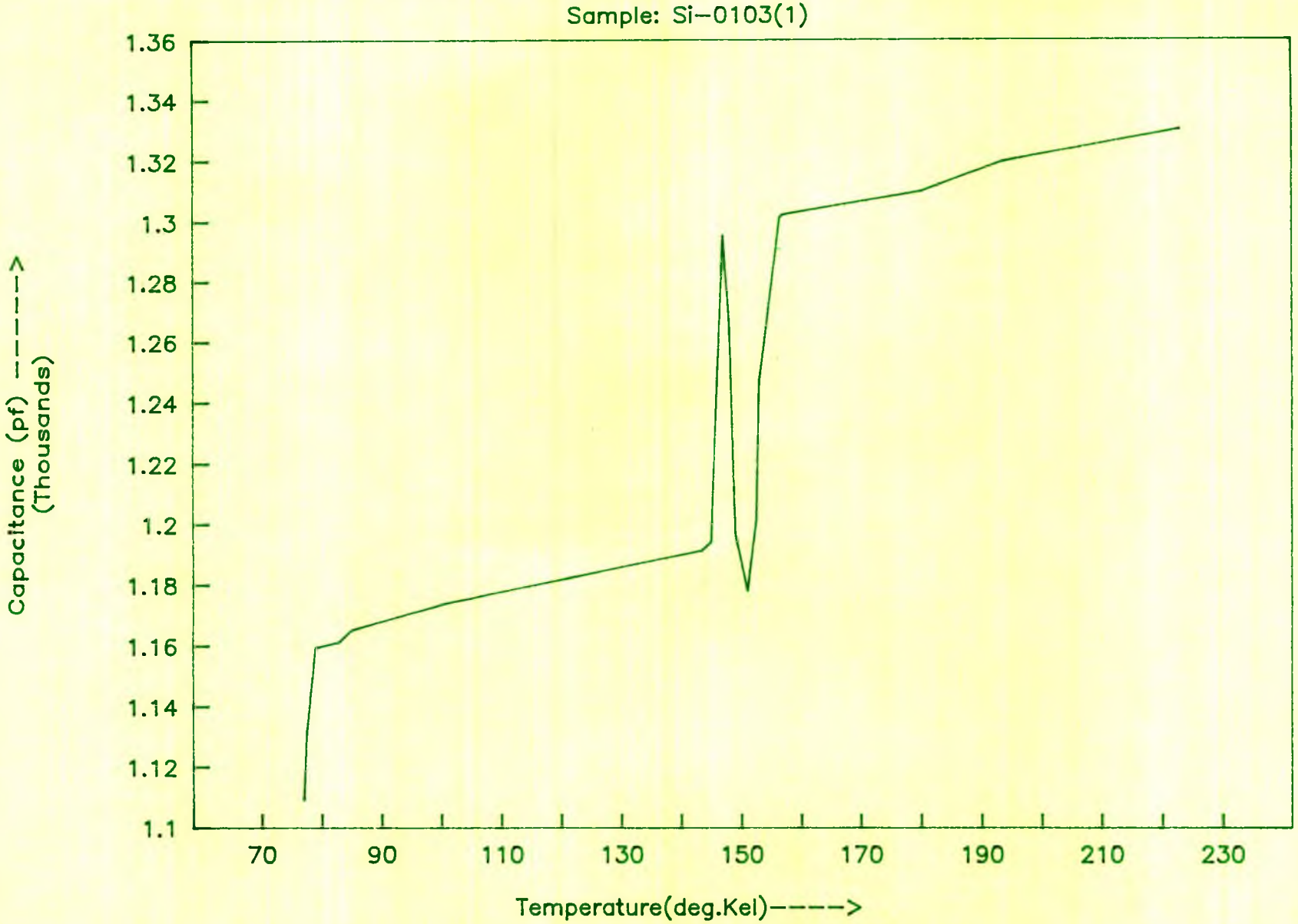
Although we have not used DLTS technique for our work, we present two DLTS spectrum: one for Si(p^+n) device containing defect states and another of a p-n-p transistor (base-collector) for comparison. The spectra were obtained from our laboratory built DLTS - spectrometer..

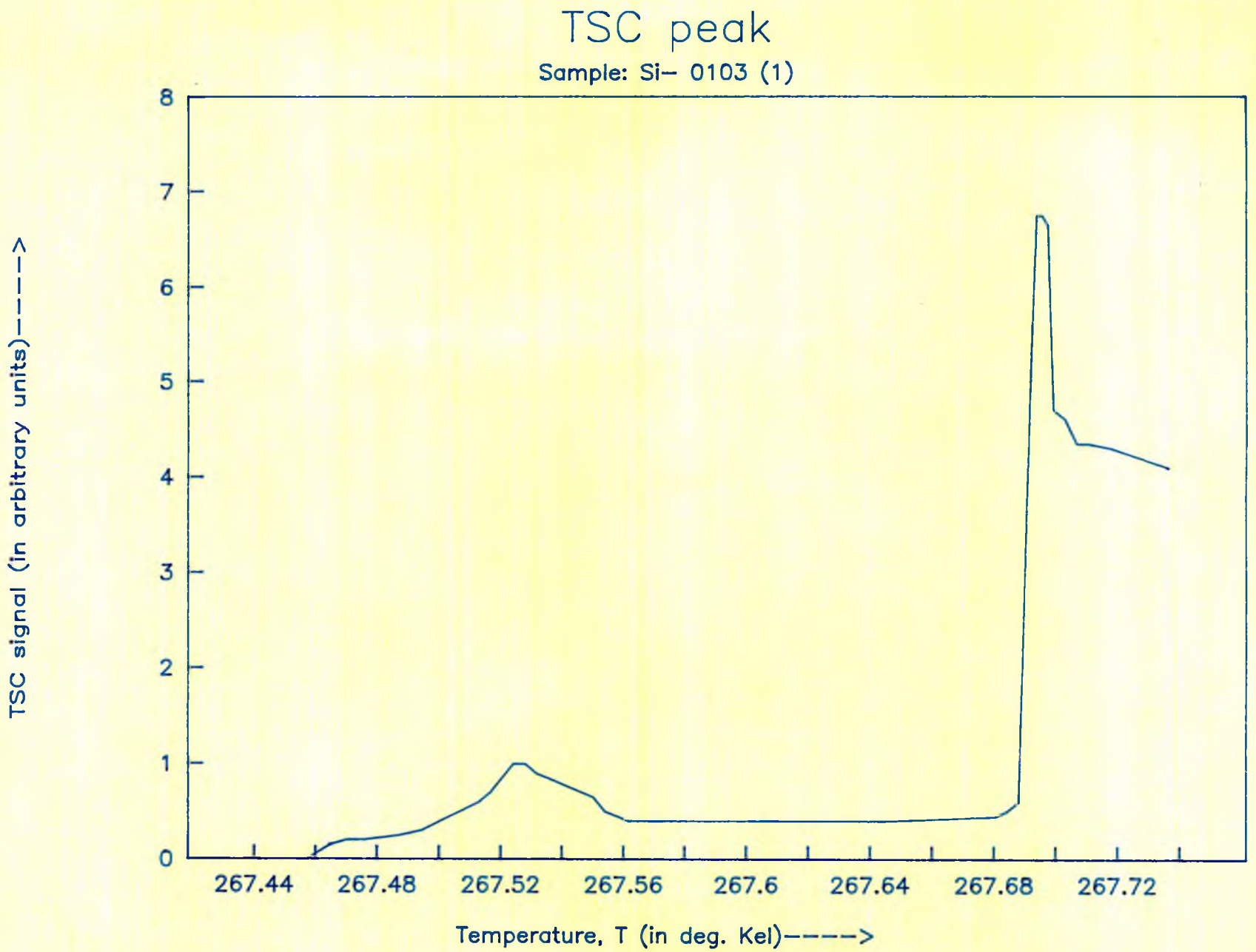
The characterization of the defect states found in some devices of our study are presented in Fig. (37).

6.4 CALCULATION AND NUMERICAL ANALYSIS:

Numerical calculations for such a large number of samples have been done using computer facilities of the University of Dhaka. It is worth noting that in our calculation for extracting various parameters from assumed formulae, we have to plot linear equation between two variables one being assumed independent many a times. We thus need a least-square fit i.e. we need to find a least square regression line. We developed a computer programing

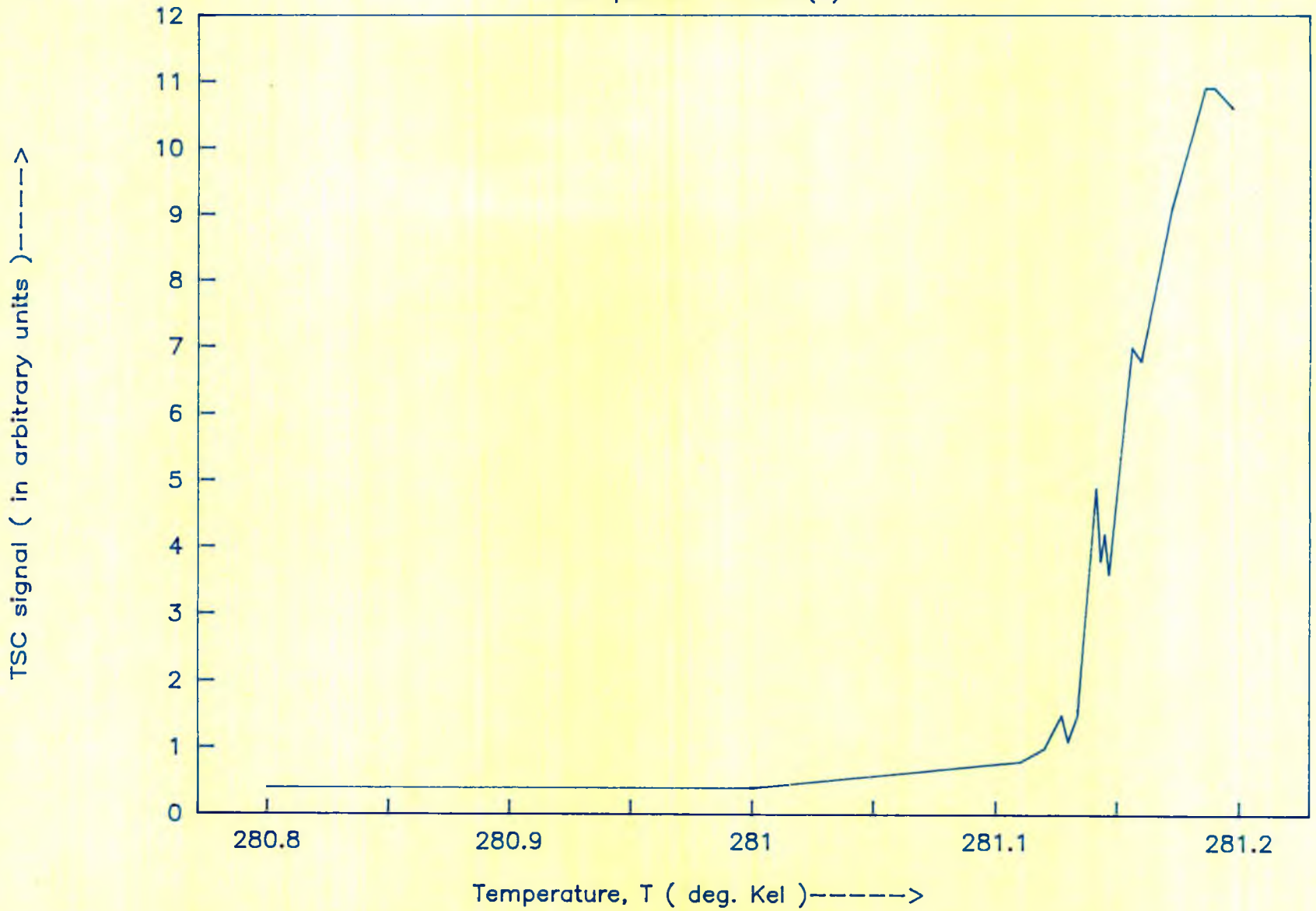
CAPACITANCE STEP VS TEMPERATURE




TSC peak
Sample: Si– 0103 (1)
TSC signal (in arbitrary units)----->
8
7
6
5
4
3
2
1
0
267.44
267.48
267.52
267.56
267.6
267.64
267.68
267.72
Temperature, T (in deg. Kel)----->
0
1
2
3
4
5
6
7
8

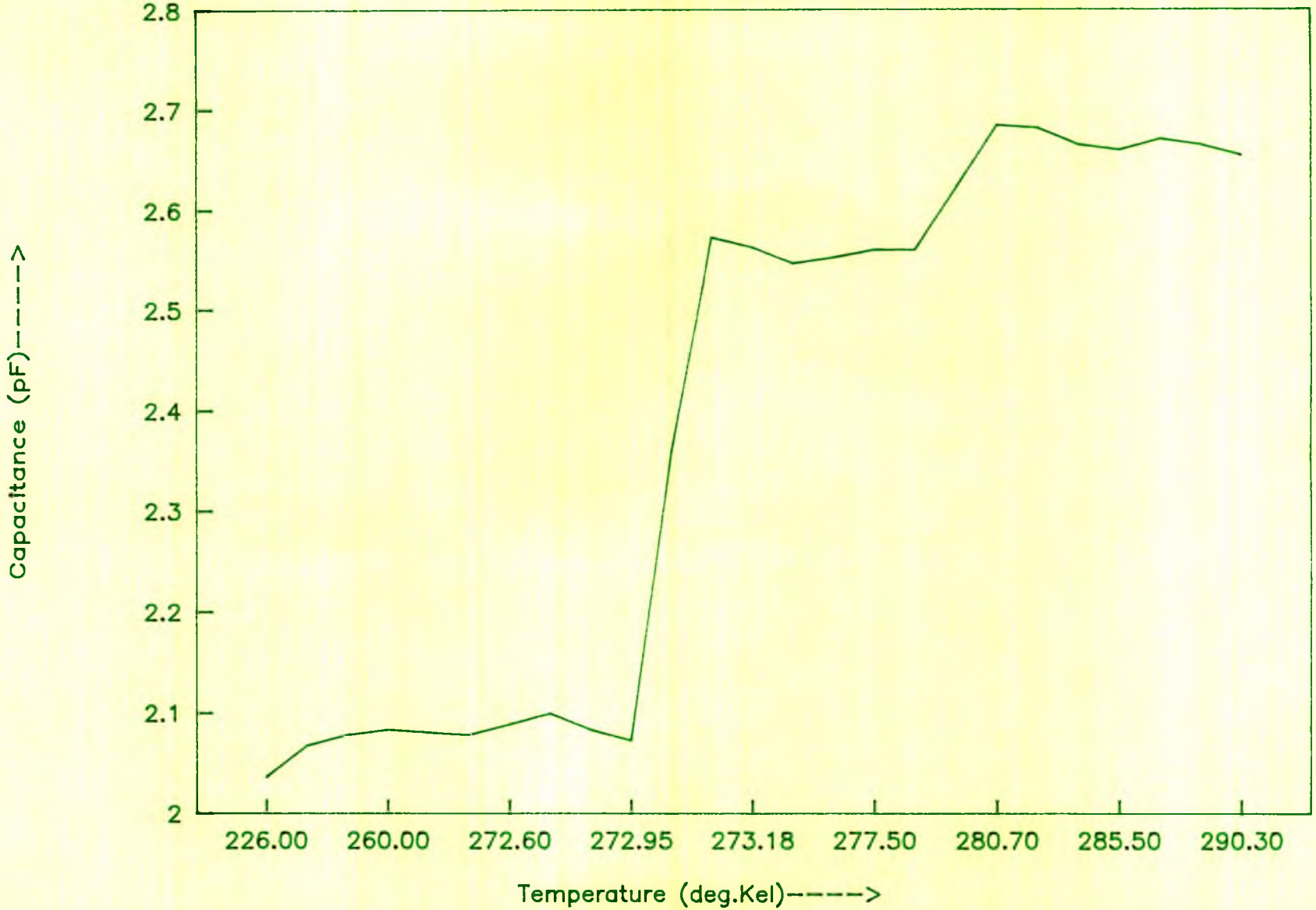
A typical TSC peak

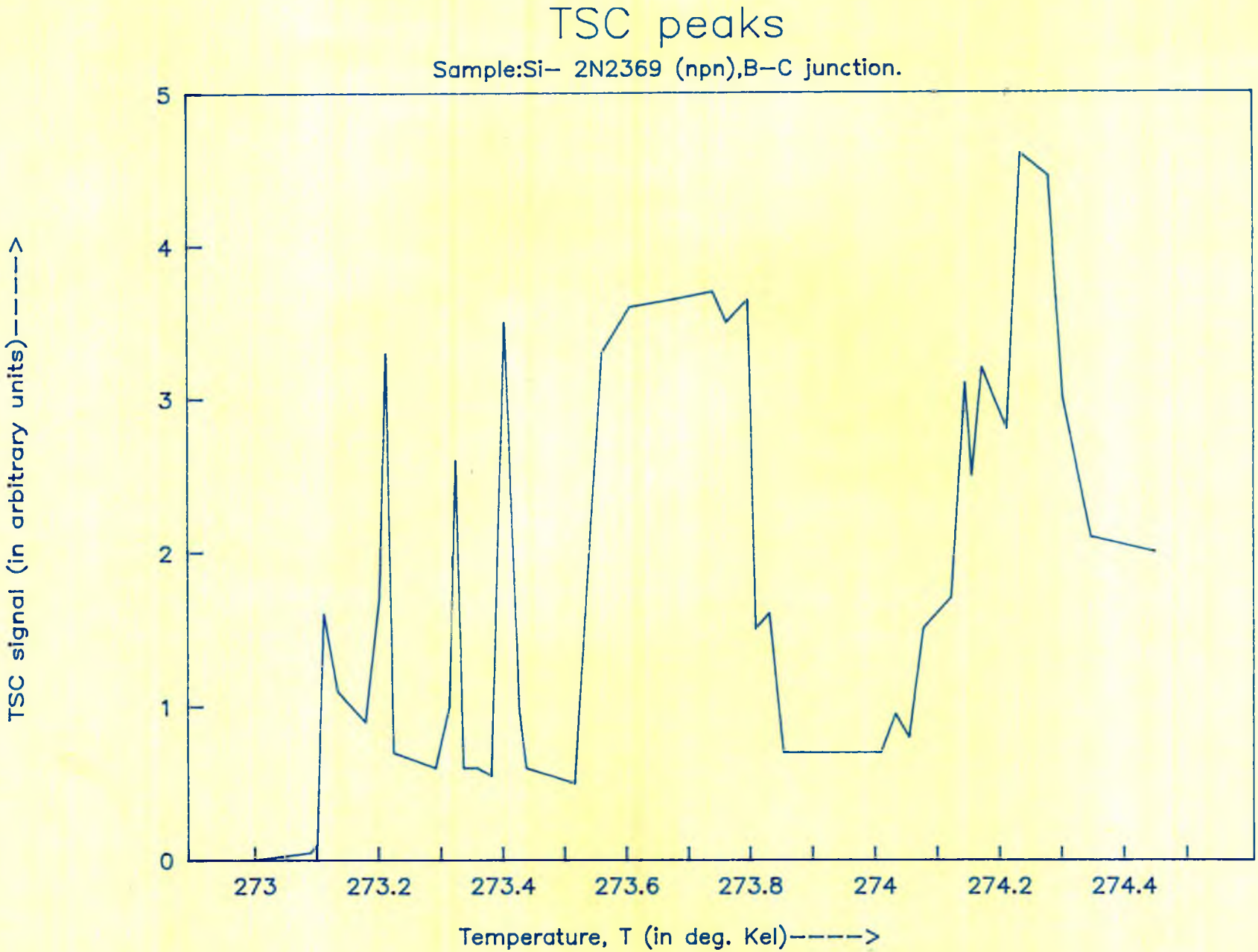
Sample: Si – 0103 (1)

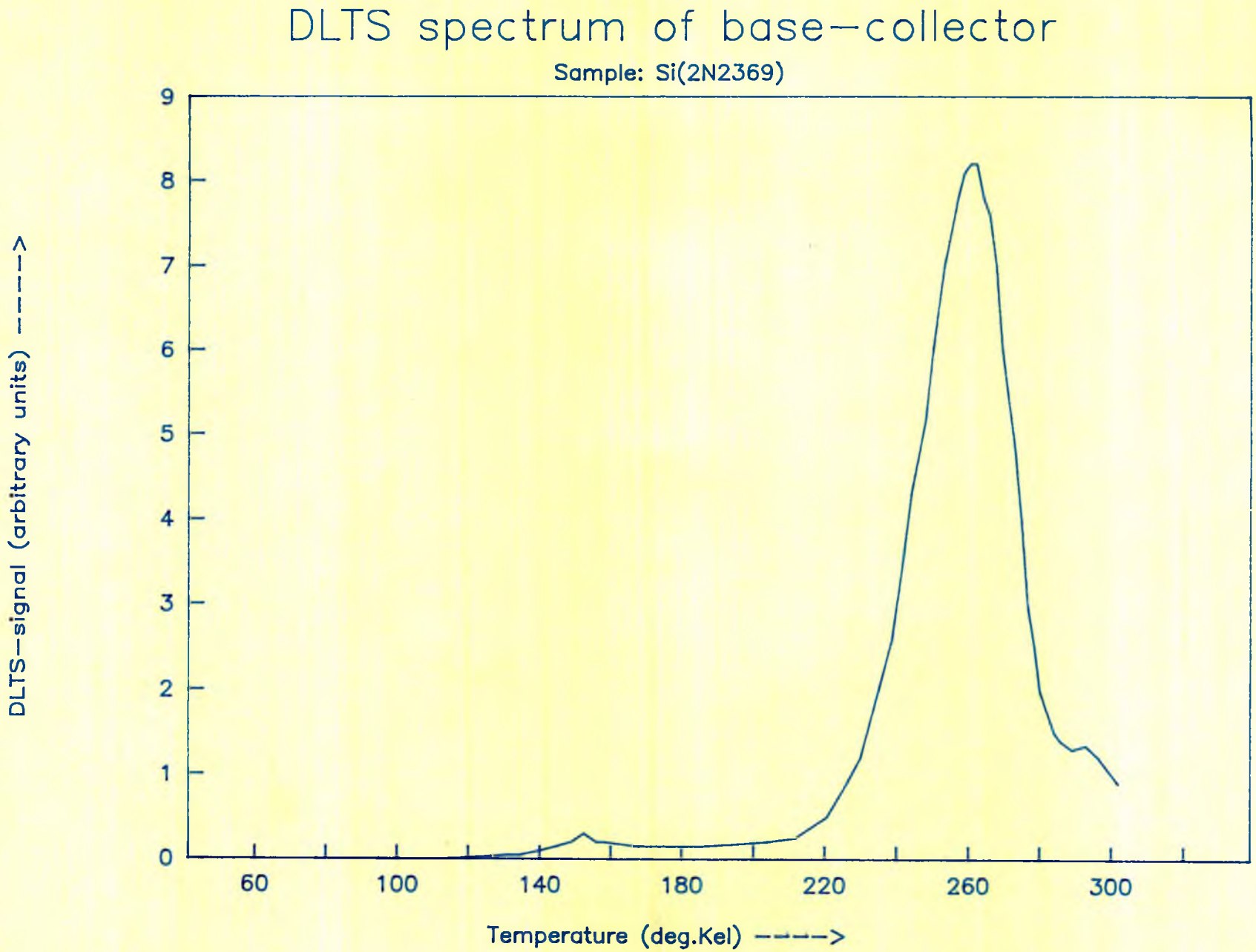


CAPACITANCE STEP VS TEMPERATURE

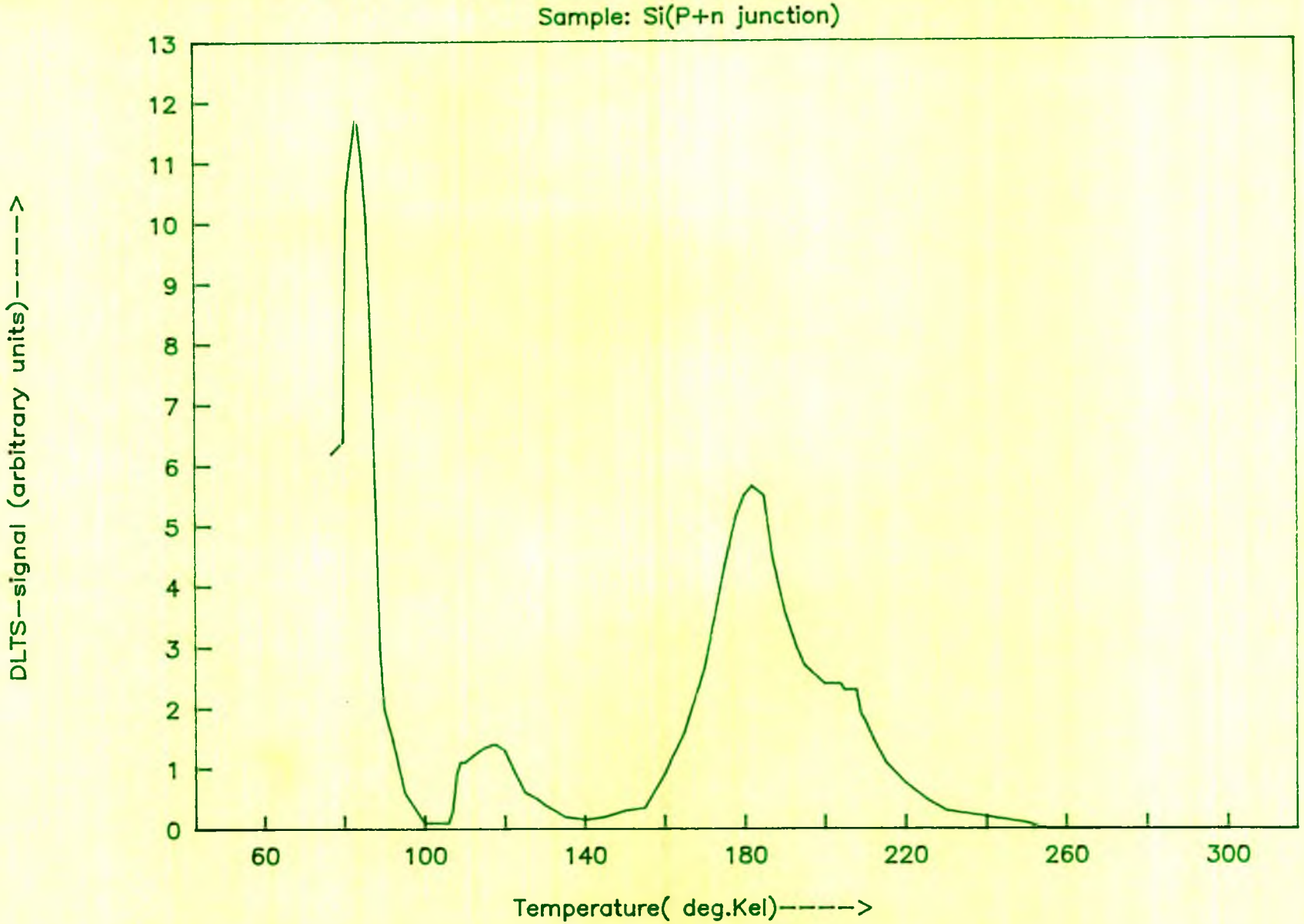
Sample: Si-2N2369(npn) B-C junction




TSC peaks
Sample:Si– 2N2369 (npn),B–C junction.
TSC signal (in arbitrary units)----->
0
1
2
3
4
5
273
273.2
273.4
273.6
273.8
274
274.2
274.4
Temperature, T (in deg. Kel)----->
0
1
2
3
4
5


DLTS spectrum of base-collector
Sample: Si(2N2369)
DLTS-signal (arbitrary units) ---->
0
1
2
3
4
5
6
7
8
9
60
100
140
180
220
260
300
Temperature (deg.Kel) ---->

A DLTS spectrum in e–irradiated Si



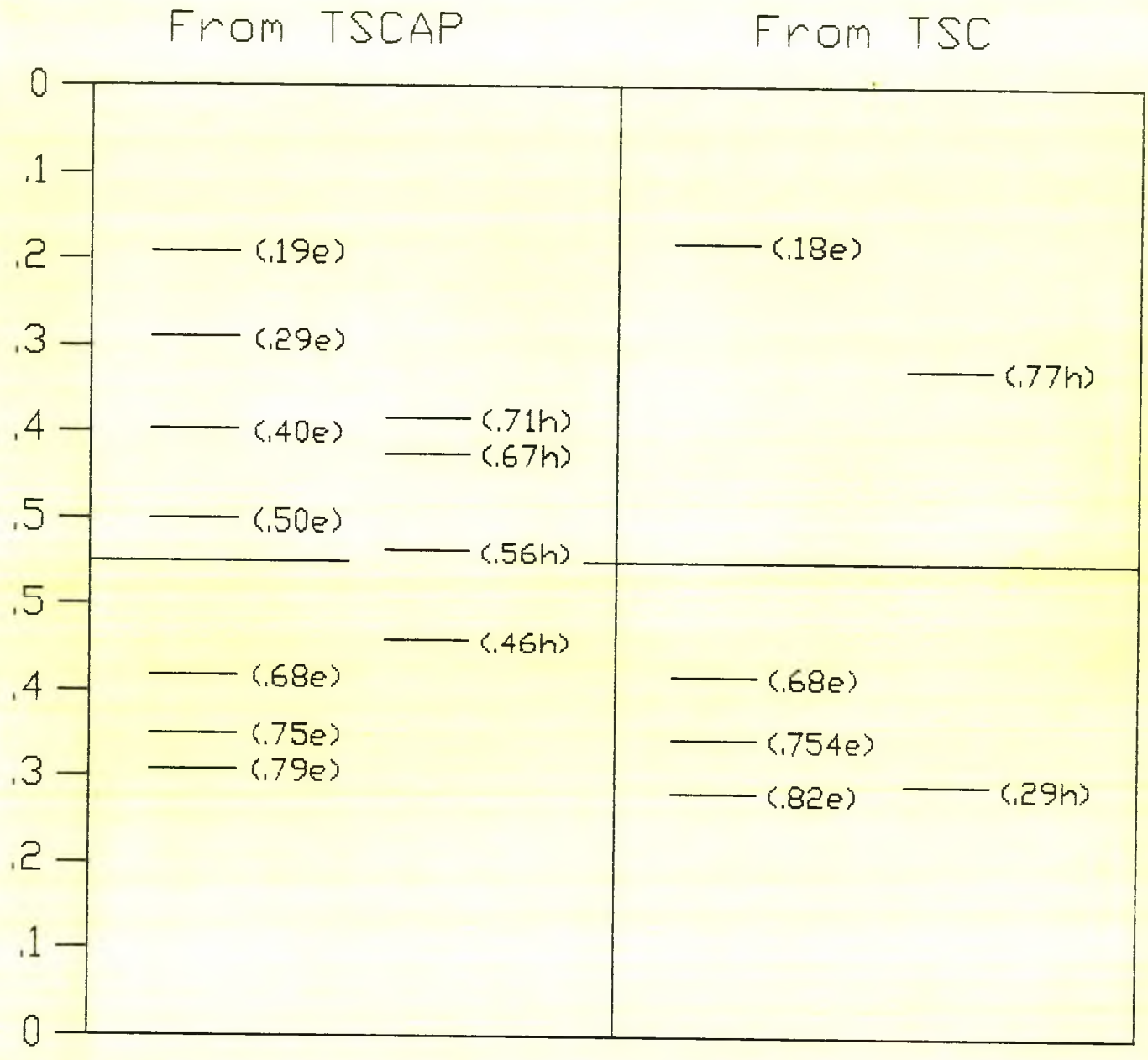


Fig. 37 Electrical deep levels found in SI-devices studied here in

for regression line and many programmes for other calculations. The programmes are written in BASIC and (or) FORTRAN.

To estimate ΔE_i from maximum slope point in TSCAP step (or peak point in the case of TSC) we need to solve an equation of the general form

$$x = \ln\left[\frac{a}{\beta(x+c)}\right]$$

Analytically solution of such an equation is not possible. We therefore solved this equation numerically using Newton-Raphson method; we may go on improving the assumed solution by repeating the method several times.

Let $F(x) = x - \ln\left[\frac{a}{\beta(x+c)}\right]$, then according to Newton-Raphson method, the improvement is carried on by using the formula

$$a_n = a_{n-1} - \frac{f'\left(a_{n-1}\right)}{f\left(a_{n-1}\right)}$$

where a_n = new root

a_{n-1} = the previous value of the root

$F'(a_{n-1})$ = value of the first derivative of the $F'(x)$ at $x = a_{n-1}$

$F(a_{n-1})$ = value of $F(x)$ at $x = a_{n-1}$

For numerical solution, we developed a computer programing in BASIC.

6.5 DISCUSSION

The study presented here is of survey type. Our main purpose has been to look into the behavior of the commercially fabricated p-n junctions and how their characteristics compare with the theoretically predicted behavior. We studied over fifty p-n junction devices in the form of simple diodes or transistors. We limited our survey within devices made of most common semiconductors such as Si, Ge and GaAs. Although more then 50 samples have been studied, we presented here results of 20 samples or so. This is because of the repetitive nature of our findings. The experimental data presented here is of representative type. As stated earlier our study includes (i) I-V measurements, (ii) C-V measurements and the (iii) transient capacitance and current measurements.

I-V studies reveal that most of the commercial diodes are far from the ideal behavior. Even the generally accepted empirical formula $\exp\left[qV/\eta kT - 1\right]$ fails to explain many of the diode-behavior. In many cases η-factor evaluated by us exceeds the normally accepted value of 2 (for Si or GaAs) (Table - 8). Even in the case of Ge, the η-factor is found to be greater then unity in many cases.

As we pointed out and discussed earlier (ch1: Sec 1.5-1.6) that the deviation from ideal behavior is primarily due to series resistance effect and presence of generation-recombination centers in the depletion region. The recombination centers create an extra

current component in the total diode current for forward bias condition, whereas generation centers affect the reverse saturation current.

When a diode is operating under forward bias, the carrier concentration in the depletion region is quite high and it is natural that substantial recombination occurs. The recombination rate (when p = n) in the depletion region is usually taken as, $r = \frac{1}{2\tau_o}\left[n_i \exp(qV/2kT)\right]$, This is the reason why one expects that η-value should be 2. The recombination falls exponentially on either side of the "p-n junction interface" with a characteristic diffusion length kT/qE. E is the electric field produced by contact potential. One would expect an additional current in the diode given by $J_r = \left[\frac{kT}{qE}/\tau_o\right] \times \exp\left[qV/2kT\right]$. This additional current is not taken into account in simple Schokley treatment of diode current. The problem has been further looked into by Sah and Noyce. If the reverse current dominates because of generation of carriers in the depletion region, it will obviously depend on depletion width and hence on the nature of the junction. Because of this complicity of the problem one attempts to use the empirical law i.e. to replace 2 by η. The factors contributing to the term in the empirical equation are many and varied. Our study reveals that in many cases the value is greater than 2 and it also depends on temperature and type of diodes. It is therefore not unusual to have η-value as larger as 4. Probably in such cases the series resistance effect comes into play. We noted that if the

series resistance effect is included, even in the low current region, a considerable improvement is obtained in I-V characteristics for many practical diodes. Thus even in the case of low current region series resistance affects the behavior.This has been amply proved from the comparison of η-values calculated from reverse saturation current measurement with that of forward bias measurement. In the former case series resistance does not come into effect and η-value is found to be more close to 2.

Our C-V measurement also confirms that many a practical diodes are not in conformity with their ideal behavior as is assumed in theory. The presence of recombination and generation centers that comes from the introduction of impurity or defects in the host crystal. The departure from the ideal behavior is an indication that devices are contaminated by the presence of defect centers. The presence of defect centers greatly influences the properties of the depletion region and hence it must be reflected in the C-V behavior of a diode. The effect of defect states on the junction capacitance has been dealt with in ch-3 (sec 3.11-3.12).

We therefore undertook the study of deep defects centers, if any, in commercially fabricated diodes particularly those which gave indication from C-V and I-V studies that they may contain defect states. Our study reveals that most of the diodes contain defect states lying deep inside the forbidden gap.

Both TSCAP and TSC techniques reveal their presence. In most of Si-devices we found defect centers. As for example in one of

the sample of Si(0103) there are as many as 10 defect centers. We have characterized those defect states, and note with interest that there are some common centers which occur in most Si-diodes. These are 0.19eV, 0.40eV, 0.50eV and 0.75eV. The devices contain both electron traps as well as hole traps. The most important hole traps we found in Si are 0.54eV, 0.67eV, 0.71eV. In another sample (2N2369) we found 3 hole traps of activation energy 0.741eV, 0.747eV and 0.771eV of which 0.747eV is the strongest.

TSC study also confirms the result although lower states do not show up in TSC measurement. From TSC study it is further observed that the hole trap corresponding to 0.75eV is in infact a bundle of few defect states lying close to each other. Infact it is found that there are three group of closely packed lines, one group having 3-lines (0.68, 0.70, 0.71eV), another group of four lines (0.72, 0.79, 0.74, 0.74eV) and last group having two lines (0.751, 0.76). This is true for other lines too. It seems TSC technique offers better resolution and may be more useful for studying finer details.

In most Ge-samples, we observed three levels, two electron traps (0.13eV, 0.43eV) and one hole trap (0.47eV). TSC result also confirms these findings, although once again we do not get signal from the shallower levels lying on the low temperature side.

We note with interest that in one Si-sample there exists hole trap near 0.29eV revealed by TSC measurement. Although we have been able to detect and characterize the deep states found in Si-

and Ge- devices, we are not in a position to identify the centers. Neither TSCAP nor TSC is capable of doing so. Therefore we made no attempt to identify or assign any structure to the defect centers found in our study.

We may however compare our characteristic values with most commonly occurring defect centers those have been identified by many authors.

Oxygen is a very common impurity in Si. It is always present in crucible-grown silicon. Usual impurity centers associated with oxygen are 0.16eV, 0.38 below E_c and 0.35 above E_v. The observed 0.40eV found in our Si-sample may well be compared with state 0.38eV. On the other hand Fe is another frequently occurring impurity in Si. It is observed that an impurity center associated with 0.40eV and a state 0.51eV below E_c. Our observed 0.50 level in Si may well be such an impurity state. But this is just a speculation.

On the other hand if we look to the defect states that we obtained in Si either produced by high energy irradiation or by chemical method, Si may contain $V_2^=$, V_2^- and V_2^o defect centers. $V_2^=$ center is associated with 0.40eV, and 0.23eV below E_c, V_2^- center has two levels below Ec (0.54eV and 0.40eV) whereas V_2^o is associated with many states including one 0.75eV below Ec.[a] All such levels are found in our Si samples.

In order to compare our findings with defects states we may compare the finding of DLTS studies being made in our laboratory.

From DLTS spectrum it has been found that electron irradiated-Si gives prominent peaks having activation energy 0.20eV, 0.23eV, 0.29eV, 0.39eV, 0.51eV, and 0.559eV [b]. Our 0.19eV, 0.29eV, 0.40eV, and 0.51eV are to be compared with those levels. Therefore 0.19eV, 0.29eV, 0.40eV and 0.51eV may well be attributed to V_2^- and $V_2^=$ defect centers. There are many other TSC peaks we find in the range of 0.84eV to 0.68eV. Their identification remains uncertain. It is noted that in most Si samples a group of lines near 0.75 -0.78eV appears (also seen in some Si- in TSCAP). For comparison we took a DLTS spectrum of this sample (2N2369) and found a strong DLTS signal in the region of 0.75eV. This observation is in agreement with TSC and TSCAP results.But TSC gives a better resolution than DLTS. From Ge - devices we note that there are three levels, two electrons traps - 0.12eV, 0.43eV below Ec and a hole trap 0.47eV above Ev, whereas TSC measurement reveals a series of consecutive levels at higher temperature ranging from 0.4617 to 0.4945eV below Ec. These finer states are really unknown centers, and these are not associated with any common impurity centers.

None of the GaAs samples we studied show any defect states except one marked as GaAs (ASEA - 2) in Table -8. This sample shows only two peaks that is associated with native defect states A(0.44eV) and B(0.76eV). But unfortunately the sample has been damaged during measurement and we could not make any detail measurement. It seems, all GaAs samples we studied were fabricated

in a very clean atmosphere.

Although we have presented a brief survey report here on deep states obtaining in the samples of our studies, we do not offer any suggestion how they got into, and nor we suggest the nature of their structure. For the proper identification, one has to continue the work with other method of investigation including EPR, Hall effect and DLTS.

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b. A. K. Roy, "DLTS study of e-irradiated Si-$p^{+}n$ junctions", unpublished work.

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